Electrical characteristics of MIS structures with ALD Al_2O_3, HfO_2 and Nanolaminates on different silicon substrates

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In this work the electrical characteristics of different atomic layer deposited (ALD) high-permittivity dielectric films (Al_2O_3, HfO_2 and a nanolaminate of them), with a physical thickness about 10 nm, are evaluated. An extensive capacitance-voltage (C-V) and current-voltage (I-V) characterization at room temperature is carried out on metal-insulator-semiconductor (MIS) structures fabricated on different p-type and n-type silicon substrates and with Al as metal gate. HfO_2 layers are found to exhibit the higher dielectric constant, but they suffer from the largest hysteresis and leakage currents and the lowest breakdown voltages. The nanolaminate stacks, with an intermediate dielectric constant, are found to exhibit more similarities to the Al_2O_3 layers, withstanding the largest voltages of all the studied dielectric films. The electrical degradation of the layers is evaluated by means of consecutive current-voltage ramps and with constant voltage stress

experiments. Results on n-type Si, with electron injection from the substrate, indicate a dominant negative charge trapping on all the studied layers, leading to a decrease in the leakage current levels. On the other hand, the results on p-type Si, with electron injection from the metal gate, suggest that not only charge trapping but also creation of new traps, particularly under the higher stress voltages, are responsible for the observed degradation.

I. INTRODUCTION

The continuous miniaturization of complementary metal-oxide-semiconductor (CMOS) technologies has lead to unacceptable tunnelling current leakage levels for conventional thermally grown SiO_2 gate dielectrics[1,2]. During the last years, a lot of efforts have been devoted to investigate alternative high permittivity (high-k) dielectrics that could allow replacing SiO_2 and SiON as gate insulators in MOS transistors[3]. The higher dielectric constant provides higher gate capacitances with moderated thickness layers; however, other requirements such as lower leakage currents, high breakdown fields, prevention of dopant diffusion and good thermodynamic stability must be also fulfilled. A number of high-k materials have been investigated as candidates to replace the SiO_2 as gate dielectric. In this way, Al_2O_3, ZrO_2 and HfO_2, as well as their silicates, are amongst the most studied ones[3,4].

Apart from CMOS technologies, high-k dielectrics are also of important interest for a wide range of micro/nanoelectronics applications, such as dynamic random access memories (DRAM)[5],emerging nanodevices[6,7], organic light emitting devices[8],silicon solar cells[9], or microelectromechanical systems[10]. For all these applications, it becomes necessary to have also a deposition technique capable of producing high-quality films

with good dielectric properties, large area uniformity and conformality and accurate control of thickness. To this respect, atomic layer deposition (ALD) has been shown to meet most of these demands[11,12]. Moreover, taking advantage of ALD unique properties, a few works have also studied the possibility to deposit alternate layers of different high-k materials (nanolaminates). This can be useful to tailor the dielectric properties of the stack, reduce leakage currents in the presence of possible crystallization processes or improve the interface in contact with the semiconductor, by introducing an intermediate permittivity dielectric with better properties in contact with silicon[13,14].

It is known that the electrical properties of ALD-deposited layers can be strongly affected by deposition and post-deposition conditions[3,4]. Whereas some of the post-deposition treatments can have a deleterious effect, others may be useful to improve the characteristics of the as-deposited layers[15,16]. The integration of such new high-k dielectrics requires important efforts in characterization to optimize process parameters[17,18]. In recent years, a lot of work has been devoted to the electrical characterization and reliability issues of alternative high-k dielectrics stacks[19,20], where the role of different aspects like the presence of a SiO_2 interface layer with the silicon substrate, the material of the gate electrode or the chemistry precursors used for the ALD process have been under study.

In this work, we evaluate the electrical characteristics of ALD-deposited high-k dielectric layers of Al_2O_3, HfO_2 and a nanolaminate of them without any high temperature annealing, so that a comparison of the as-deposited layers can be carried out. The study has been made by means of the measurement of the electrical properties of MIS structures fabricated with a dielectric physical thickness of about 10 nm on different

p-type and n-type silicon substrates and Al as the metal gate. The capacitance-voltage and current-voltage characteristics of the different layers have been measured and analyzed and the electrical degradation phenomena due to consecutive current-voltage ramps as well as to constant voltage stress experiments are reported.

II. EXPERIMENTAL DETAILS

A. Atomic Layer Deposition Processes

Three high-k dielectric layers are considered in this study: Al_2O_3, HfO_2 and a nanolaminate of them. These layers were grown by Atomic Layer Deposition in a Cambridge NanoTech Savannah 200 system, equipped with Trimethylaluminium (TMA), Tetrakis(Dimethylamido)-Hafnium (TDMAH) and H_2O as precursors, and N_2 as carrier and purge gas. In the case of Al_2O_3, the ALD process was done at 200ºC with 95 cycles, one ALD cycle being the sequence of the following: a H_2O pulse of 15 ms, a purge in N_2 for 5 s, followed by a TMA pulse of 50 ms and a purge in N_2 for 5 s. For HfO_2, the deposition was at 225ºC and the process has also 100 cycles, each ALD cycle being: a H_2O pulse of 30 ms, a N_2 purge for 6 s, a TDMAH pulse of 150 ms and a purge for 5 s. In the case of the nanolaminate of the two materials, a 5-layer stack ($Al_2O_3/HfO_2/Al_2O_3/HfO_2/Al_2O_3$) was grown at 225ºC, using 20 ALD-cycles for each layer. The ALD reactor pressure for this nanolaminate process is shown in Figure 1.

The film thickness of the as-deposited dielectric was obtained on layers deposited on p-type silicon substrates by a Rudolph Research Auto EL ellipsometer, using an index of refraction of 1.64 in the case of Al_2O_3, and 2.07 in the case of HfO_2. Under these conditions the physical thickness of the as-deposited layers is 11.6 nm and 10.9 nm,

respectively. In the case of the nanolaminate, a first estimation of the layer thickness can be made using the growth-per-cycle obtained for each dielectric[17]. According to the ALD process used to grow the nanolaminate stack, a thickness of ~ 10 nm was expected, that has been confirmed by cross-sectional TEM analysis[21].

B. MIS structure fabrication

In order to electrically characterize the deposited high-k layers, MIS structures were fabricated. The test devices were made on 100 mm-diameter, (100)-oriented CZ-grown silicon wafers. Three types of silicon substrates were used: one is n-type, Phosphorus-doped and resistivity 1-12 Ω·cm, and two are Boron-doped with resistivity 4-40 Ω·cm and 0.1-1.4 Ω·cm, which will be referred to as Si(p) and Si(p^+), respectively.

The fabrication process started with standard wafer cleaning followed by a wet thermal oxidation process at 1100ºC leading to a 400 nm-thick SiO_2 layer. Next, this field oxide was patterned by photolithography and wet etching. Immediately after cleaning in H_2O_2/H_2SO_4 and a dip in HF(5%), the deposition of the high-k dielectric layer by ALD was carried out and a 500 nm-thick Al/0.5%Cu layer was deposited that constitutes the metal gate of the MIS structure. After patterning the metal layer by photolithography and wet etching, the back of the wafers were also metalized with aluminum for electrically contacting the silicon substrate. Finally, the wafers underwent a forming gas ($N_2/(10\%)H_2$) annealing step at 350ºC for 20 min. The fabricated MIS structures are square-shaped with five different surface areas ranging from 9.604×10^{-3} cm^2 to 6.4×10^{-5} cm^2. A cross-sectional view of the structure is shown in Fig. 2.

C. Electrical characterization

The study of the electrical characteristics of the different MIS structures has been carried out through the measurement of capacitance-voltage (C-V) and current-voltage (I-V) characteristics. All measurements were performed at room temperature in a light-proof, electrically shielded probe station.

C-V curves were recorded using a HP4192-A Impedance Analyzer in the parallel configuration. The stair sweep voltage was 0.05 V and the a.c signal voltage was 0.03 V. Since the Si(n) and Si(p) substrates have a significant spreading resistance as compared to the impedance of the high-k structure, an a.c. signal frequency of 30 kHz was selected for all substrates and dielectric layers, so that correction for series resistance effects was not needed. In this way, the capacitance of the structure at the maximum gate voltage in accumulation was used to extract the Capacitance Equivalent Thickness (CET). The hysteresis was measured by sweeping the voltage from inversion to accumulation and then sweeping back from accumulation to inversion. For p-type silicon substrates, the voltage was swept from 2 V to -3 V and back to 2 V, whereas for n-type silicon the voltage sweep went from -2 V to 3 V and back to -2V. From this measurement, the hysteresis voltage, V_h, was obtained from the voltage separation of the curves at the flat band condition.

Current-voltage curves were recorded using a HP 4155B Semiconductor Parameter Analyzer, with Long Integration Time configuration. The MIS structures were biased in accumulation, i.e., applying negative voltages to the metal gate with respect to the p-type substrates and positive voltages in the case of the n-type silicon. In this way, current injection from the metal gate for p-type, and injection from the silicon substrate for n-type, can be analyzed.

III. RESULTS AND DISCUSSION

The capacitance-voltage (C-V) measurements were done on 104 MIS structures with a surface area of 2.304×10^{-3} cm^2, for each wafer. Figure 3 shows an example of the C-V curves obtained for the three dielectric layers on the three silicon substrates. From each C-V curve, the CET, flat-band voltage, V_{fb}, and hysteresis, V_h, were extracted. The statistical results are summarized in Table I, where the mean values of each parameter are given together with the standard deviation of V_{fb} and V_h.

As for CET, excellent uniformity across the wafer is obtained, with a standard deviation less than 0.1 nm in the worst case. As expected, CET for HfO_2 layers is lower than for Al_2O_3, in accordance with a higher dielectric constant for HfO_2 than for Al_2O_3. In the case of the nanolaminate, intermediate CET values are obtained which would correspond to an intermediate k, as already reported for nanolaminate stacks[22].

With respect to the flat-band voltages, the measured values indicate that a rather large negative fixed charge exists in the dielectric. In order to estimate the density of fixed charge located at the insulator-silicon interface, the experimental values are compared to those corresponding to an ideal MIS structure. This simplified analysis gives charge densities ranging from 3×10^{11} cm^{-2} for Al_2O_3 on Si(n) up to 7×10^{12} cm^{-2} for the nanolaminate stack on Si(p^+).

As shown, all dielectrics exhibit counter-clockwise hysteresis on p-type silicon, and clockwise hysteresis on n-type silicon, although its magnitude is significantly different depending on the type of the silicon substrate and the dielectric material. In the case of Si(n), all dielectric layers exhibit large hysteresis indicating significant charge

trapping. For Si(p) and Si(p^+), large hysteresis is also observed in the case of HfO_2, whereas for Al_2O_3 the hysteresis is small. A rather different behavior is shown by the nanolaminate, since the hysteresis is rather small in the case of Si(p) substrates as compared to the behavior shown by the same stack on Si(p^+). Although the observed hysteresis in the C-V characteristics indicates charge trapping, these results cannot be used to measure the trapping since the magnitude of the voltage shift is dependent on the sweep rate relative to the trapping-detrapping time constants[23]. In addition, it also depends on the magnitude of the endpoints of the voltage sweep[24] and when making repeated C-V measurements on the same sample a decrease of the hysteresis width is obtained. As a consequence, a further and deeper investigation is needed to understand the different behavior observed.

With respect to electrical conduction through the dielectric layers, in Figure 4 the experimental results obtained for each type of substrate are shown for MIS structures with a surface area of 6.4×10^{-5} cm^2. It should be noted that no perimeter effects exist, i.e., identical J-V characteristics are obtained for the 5 capacitor surface areas available, except in the case of the silicon substrates with low doping level, in which a series resistance effect is observed at high current levels and large capacitor area. J-V curves of different samples across each wafer were also identical, as a consequence of the excellent insulator thickness uniformity.

Comparison of the conduction behavior of the different dielectrics shows some general trends: HfO_2 layers exhibit higher leakage current than Al_2O_3 or nanolaminates, for all types of substrates, i.e., either for injection from the metal electrode or from the silicon substrate, with breakdown voltages much lower than those of the other insulators.

When comparing Al_2O_3 with the nanolaminate , two regions are distinguished: for low voltages lower leakage is obtained for Al_2O_3 than for the nanolaminate, and the contrary occurs for large voltages, giving rise to higher breakdown voltages for the nanolaminate than for Al_2O_3.

As for the predominant conduction mechanism, the experimental results indicate that for HfO_2 and nanolaminate there is only one mechanism that determines the leakage current, being the J-V dependence similar in both cases so indicating that most probably the same conduction mechanism is predominant for the two types of dielectric layer.

In the case of Al_2O_3, however, two distinct laws along the J-V curve are observed depending on the gate voltage, for both biasing conditions. When injection is from the metal electrode, a change in the log J- V slope occurs at applied voltages around -5.8V and when injection is from the silicon substrate the change in the slope is at applied voltages around 4.5 V. If the J-V characteristics for Si(n) and Si(p) are compared, it is interesting to note that for voltages below the ones that correspond to the changing in slope, the log J-V slope is the same for both substrates, i.e., for injection from the metal electrode and from the substrate, but for voltages above the transition voltages the slopes for both biasing conditions are different, being the law the same as in the case of the other dielectric layers, as is clearly seen in Figure 4(b).

In view of the charge trapping observed from the hysteresis of the C-V curves, we have investigated what effect the electrical stress has on the J-V characteristics. For this purpose two types of measurements have been carried out. First, consecutive ramped J-V measurements have been made on the same sample increasing the endpoint of the voltage sweep, V_s, so that comparison of two consecutive J-V curves would indicate the effect of

the application of a voltage ramp up to the endpoint of the first of the two measurements. Next constant voltage stress experiments on fresh samples have been performed in order to gain a deeper insight of the different behavior of the three dielectric layers.

The results obtained from consecutive ramped J-V show that after applying a voltage ramp up to $(V_s)_i$, the endpoint of the i^{th} sweep, the next measurement with a sweep up to the same endpoint gives a gate current different from the one previously measured, either smaller or larger. If at this point another measurement is made up to the same $(V_s)_i$ no further variation in the gate current is recorded. But when increasing the V_s of the following sweep, again a different gate current is measured. In view of this behavior, the measurement procedure consisted in increasing V_s of each consecutive ramp.

In Figure 5 the results obtained for MIS structures with Si(n) substrates are shown. For all dielectrics, after an electrical stress with a voltage ramp a lower gate current density is measured in the voltage range of the previously applied voltage sweep but, for larger voltages the gate current follows the J-V characteristic of a fresh device. This behavior indicates that negative charge trapping occurs when applying a voltage ramp, being the magnitude of the trapping dependent on the maximum voltage of the sweep. It should be noted that for all V_s the current decrease is observed, i.e., there are not traps created contributing to trap-assisted tunneling[25]. In order to evaluate the effect of constant voltage stresses the recorded time evolution of the gate current on stress time is studied normalizing the current measured during the stress to the gate current level of the J-V characteristics at the stress voltage. The obtained results are shown in the insets of Figure 5. The general trends of the normalized current vs. stress time are: results are

independent of the stress voltage, after an overshoot at t=0 the current decays fast to the value that was measured in the J-V characteristics ($J_g(t)/J_o = 1$) and then continues to very slowly decay. Although this behavior is observed by the three dielectric layers under study, in the case of Al_2O_3 the normalized current decays to 0.1 after 600 s of stressing whereas in the other dielectrics it decays to 0.7.

In contrast to the very similar results obtained when injection is done from the silicon substrate, injection from the metal electrode gives rise to different results depending on the dielectric. The results are shown in Figure 6, and clearly indicate that the effect of consecutive ramped J-V measurements gives rise to different current changes. In this way, for HfO_2 a lower decrease in gate current is obtained as compared to the one for Al_2O_3, whereas in the case of the nanolaminate, the current increases. These differences are further confirmed by the constant voltage stress results, shown in the insets of Figure 6. For HfO_2 a similar result is obtained as compared for injection from the silicon substrate, the gate current decreasing irrespective of the voltage applied. This is not the case for Al_2O_3 and the nanolaminate in which only for low stressing voltages there is a continuous current decrease but when larger voltages are applied a current increase is recorded indicating the creation of new traps inside the dielectric.

IV. CONCLUSIONS

The comparison of the electrical characteristics of as-deposited 10 nm-thick dielectric layers grown by ALD, have shown that HfO_2 has a higher dielectric constant than Al_2O_3, but exhibit larger hysteresis and leakage current and lower breakdown voltages, for all types of silicon substrates. As for the nanolaminate stack of these

dielectric materials, an intermediate dielectric constant is obtained, with hysteresis widths in C-V characteristics similar to Al_2O_3. In addition, the nanolaminate withstands the largest voltages of the layers studied, although it exhibits larger leakage currents at low voltages, as compared to Al_2O_3.

With respect to the effect of electrical stress on the characteristics of the studied dielectric layers, negative charge trapping has been shown for all layers when injection is from the silicon substrate whereas for injection from the metal electrode different effects are observed depending on the high-k dielectric, since HfO_2 exhibits only negative charge trapping but Al_2O_3 and nanolaminates show this effect only for low stress voltages, an effect that leads to lower leakage currents. Instead, for larger stress voltages, creation of traps is observed that lead to an increase in current which can be associated to trap-assisted tunneling.

As a conclusion, the reported measurements and results indicate that the nanolaminate stack concept may lead to better electrical performance than each material alone, depending on the required characteristics for a particular application. It should be pointed out, however, that these results correspond to as-deposited layers, without high temperature anneal, so that they give information on the material properties obtained from the ALD technique.

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TABLE and FIGURE CAPTIONS

Table I. Parameters extracted from the C-V curves at 30 kHz.

Figure 1. ALD reactor pressure in the case of the nanolaminate deposition process.

Figure 2. Cross-sectional sketch of the fabricated MIS structure.

Figure 3. Capacitance-Voltage characteristics of Al_2O_3, HfO_2 and nanolaminate dielectrics for MIS structures with (a) p-type and n-type and (b) p^+-type silicon substrates, at 30 kHz. Capacitor area is 2.304×10^{-3} cm^2. Arrows indicate the double voltage sweep direction.

Figure 4. Current-Voltage characteristics of Al_2O_3, HfO_2 and nanolaminate dielectrics for MIS structures for (a) injection from the gate electrode (p-type silicon substrate) and (b) injection from the silicon substrate (n-type silicon substrate). Capacitor area is 6.4×10^{-5} cm^2.

Figure 5. Consecutive ramped Current-Voltage characteristics for Si(n) substrate MIS capacitors with increasing endpoint sweep voltage V_s for (a) Al_2O_3, (b) HfO_2 and (c) nanolaminate dielectrics. The J-V curves labeled Fresh, correspond to the result obtained with a unique and continuous ramp voltage up to breakdown The inset shows the normalized gate current density, J_g/J_o, vs stress time under constant voltage stress, where J_o is the gate current density at the stress voltage in the J-V characteristics.

Figure 6. Consecutive ramped Current-Voltage characteristics for Si(p) substrate MIS capacitors with increasing endpoint sweep voltage V_s for (a) Al_2O_3, (b) HfO_2 and (c) nanolaminate dielectrics. The J-V curves labeled Fresh, correspond to the result obtained

with a unique and continuous ramp voltage up to breakdown The inset shows the normalized gate current density, J_g/J_o, vs stress time under constant voltage stress, where J_o is the gate current density at the stress voltage in the ramped J-V characteristics.

Table I

Dielectric		Substrate		
		Si(p+)	Si(p)	Si(n)
HfO_2	CET (nm)	3.4	3.2	3.4
	V_{fb} (V)	-0.68±0.07	-0.37±0.05	0.21±0.02
	V_h (V)	1.28±0.07	1.31±0.04	0.92±0.09
Al_2O_3	CET (nm)	5.8	6.3	6.2
	V_{fb} (V)	-0.21±0.02	0.01±0.06	0.44±0.01
	V_h (V)	0.08±0.03	0.09±0.01	0.47±0.01
Nanolaminate	CET (nm)	4.3	4.8	5.0
	V_{fb} (V)	0.16±0.04	-0.09±0.02	0.43±0.03
	V_h (V)	0.76±0.04	0.08±0.03	1.28±0.04

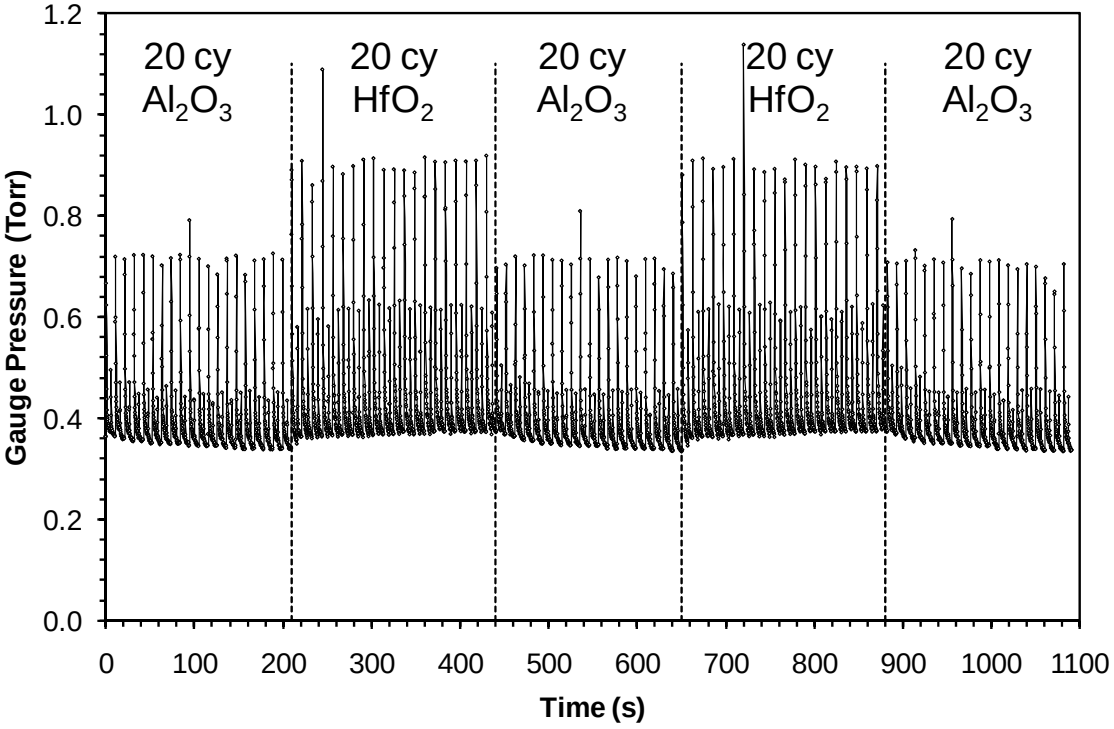

20 cy
Al2O3
20 cy
HfO2
20 cy
Al2O3
20 cy
HfO2
20 cy
Al2O3
Gauge Pressure (Torr)
Time (s)
0.0
0.2
0.4
0.6
0.8
1.0
1.2
0
100
200
300
400
500
600
700
800
900
1000
1100

Figure 1

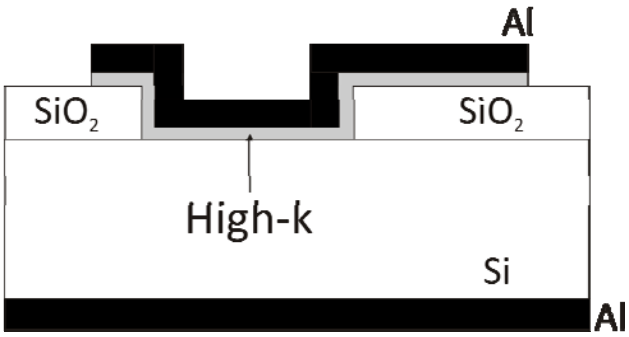
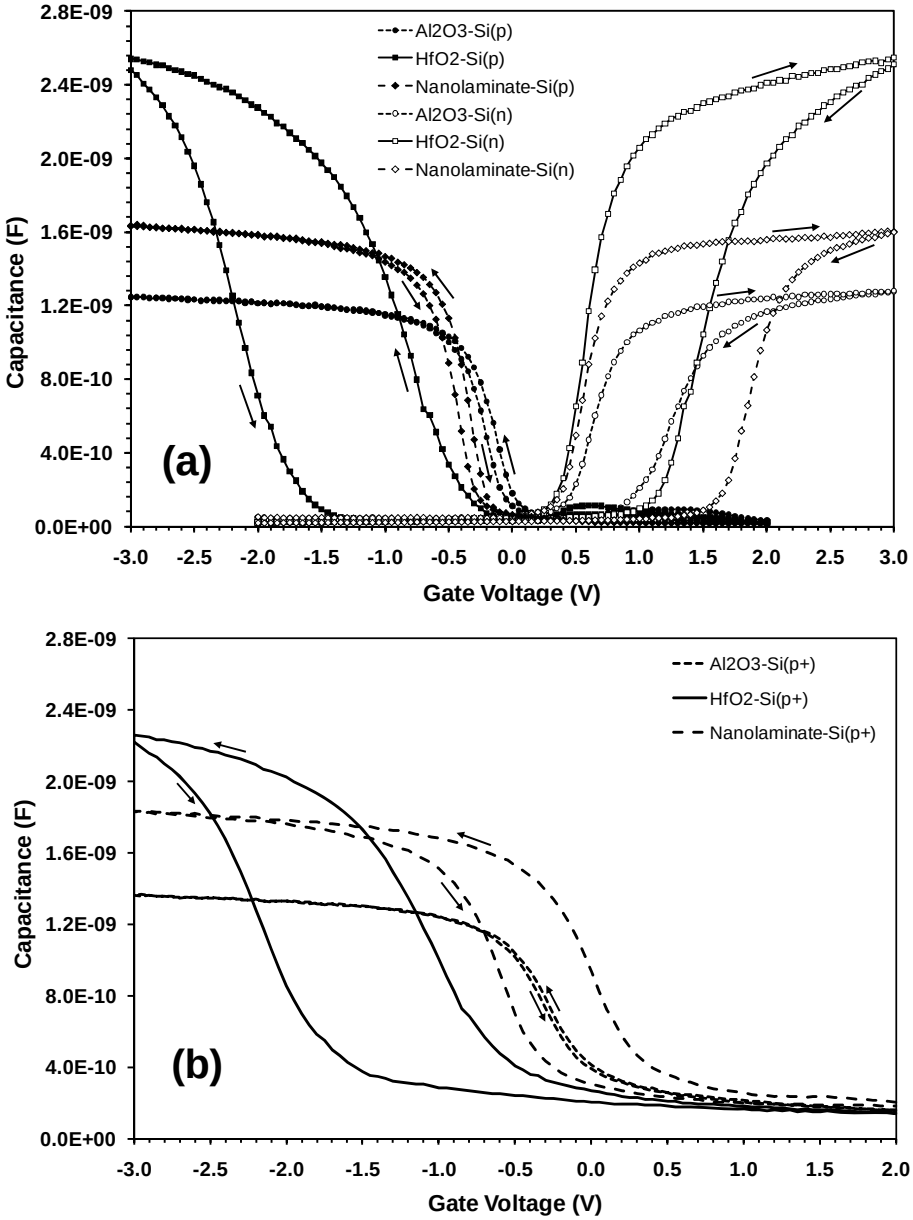


Figure 2


Al2O3-Si(p)
HfO2-Si(p)
Nanolaminate-Si(p)
Al2O3-Si(n)
HfO2-Si(n)
Nanolaminate-Si(n)
(a)
Capacitance (F)
Gate Voltage (V)
2.8E-09
2.4E-09
2.0E-09
1.6E-09
1.2E-09
8.0E-10
4.0E-10
0.0E+00
-3.0
-2.5
-2.0
-1.5
-1.0
-0.5
0.0
0.5
1.0
1.5
2.0
2.5
3.0
Al2O3-Si(p+)
HfO2-Si(p+)
Nanolaminate-Si(p+)
(b)
Capacitance (F)
Gate Voltage (V)
2.8E-09
2.4E-09
2.0E-09
1.6E-09
1.2E-09
8.0E-10
4.0E-10
0.0E+00
-3.0
-2.5
-2.0
-1.5
-1.0
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0.0
0.5
1.0
1.5
2.0

Figure 3

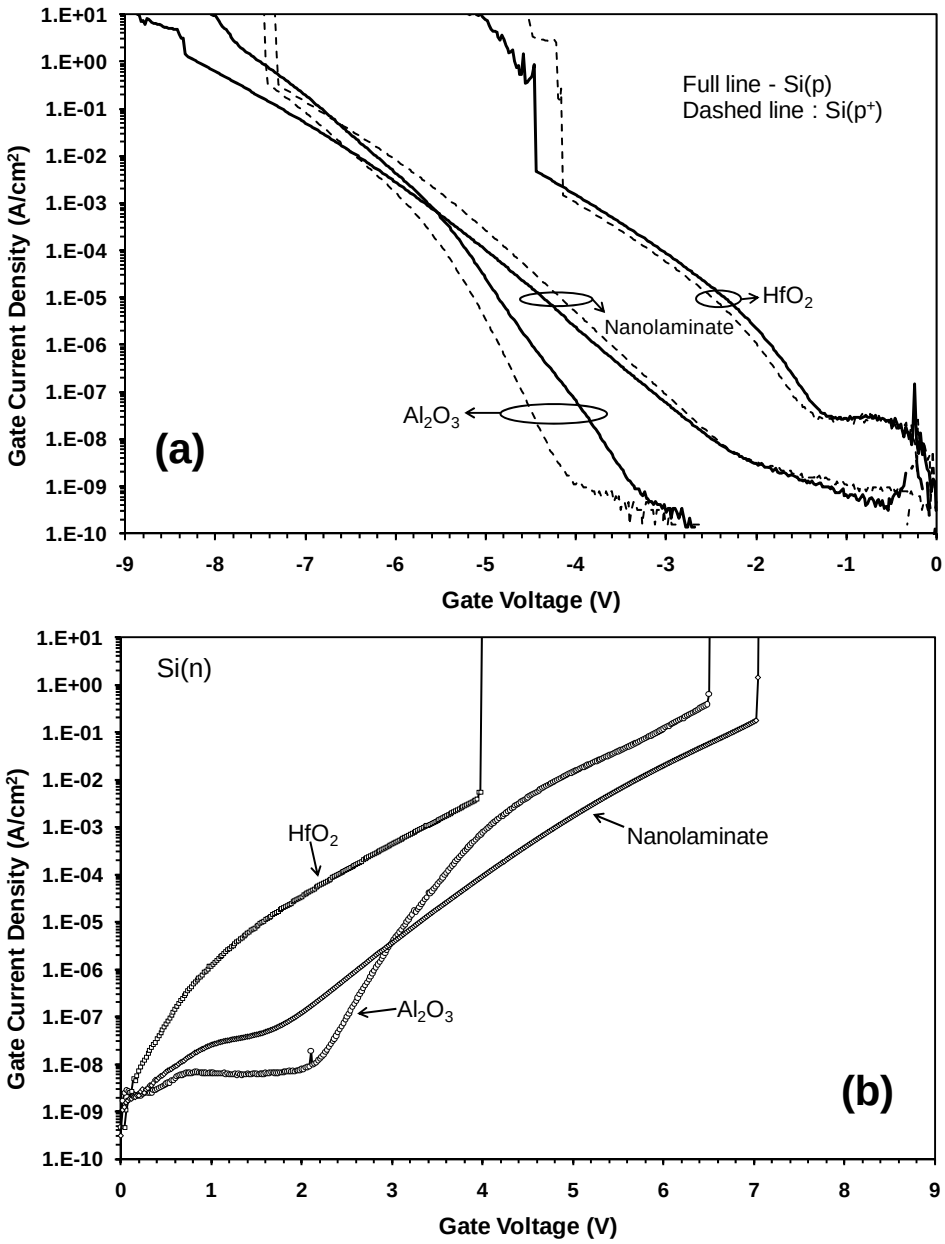
Full line - Si(p)
Dashed line : Si(p+)
HfO2
Nanolaminate
Al2O3
(a)
Gate Current Density (A/cm2)
Gate Voltage (V)
Si(n)
HfO2
Nanolaminate
Al2O3
(b)
Gate Current Density (A/cm2)
Gate Voltage (V)

Figure 4

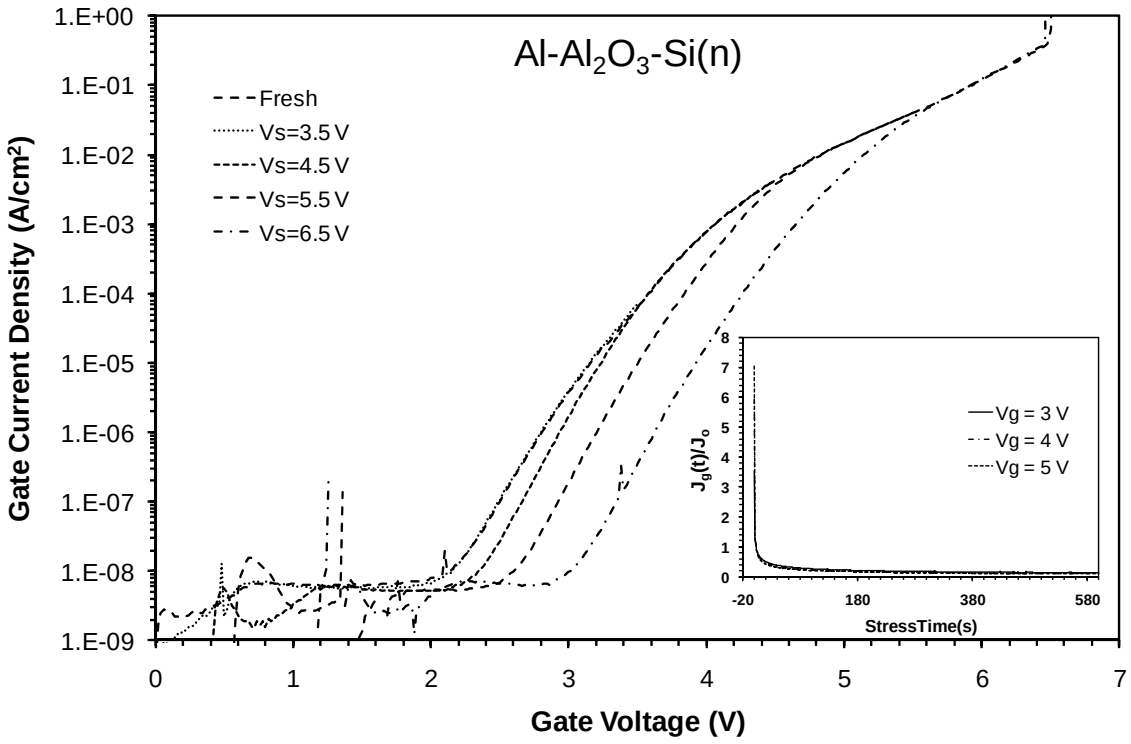
Al-Al2O3-Si(n)
Fresh
Vs=3.5 V
Vs=4.5 V
Vs=5.5 V
Vs=6.5 V
Gate Current Density (A/cm²)
Gate Voltage (V)
1.E+00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
1.E-06
1.E-07
1.E-08
1.E-09
0
1
2
3
4
5
6
7
Vg = 3 V
Vg = 4 V
Vg = 5 V
Jg(t)/Jo
StressTime(s)
-20
180
380
580

Figure 5 (a)

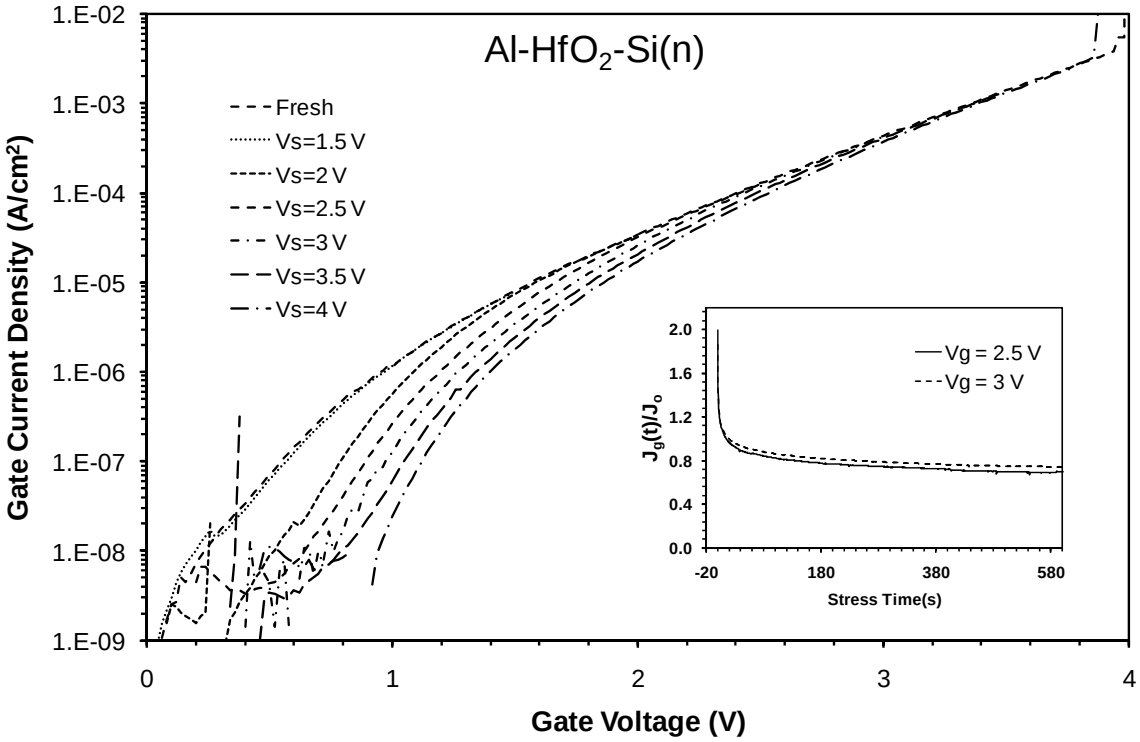
Al-HfO2-Si(n)
Fresh
Vs=1.5 V
Vs=2 V
Vs=2.5 V
Vs=3 V
Vs=3.5 V
Vs=4 V
Gate Current Density (A/cm²)
Gate Voltage (V)
1.E-02
1.E-03
1.E-04
1.E-05
1.E-06
1.E-07
1.E-08
1.E-09
0
1
2
3
4
Vg = 2.5 V
Vg = 3 V
Jg(t)/Jo
Stress Time(s)
2.0
1.6
1.2
0.8
0.4
0.0
-20
180
380
580

Figure 5(b)

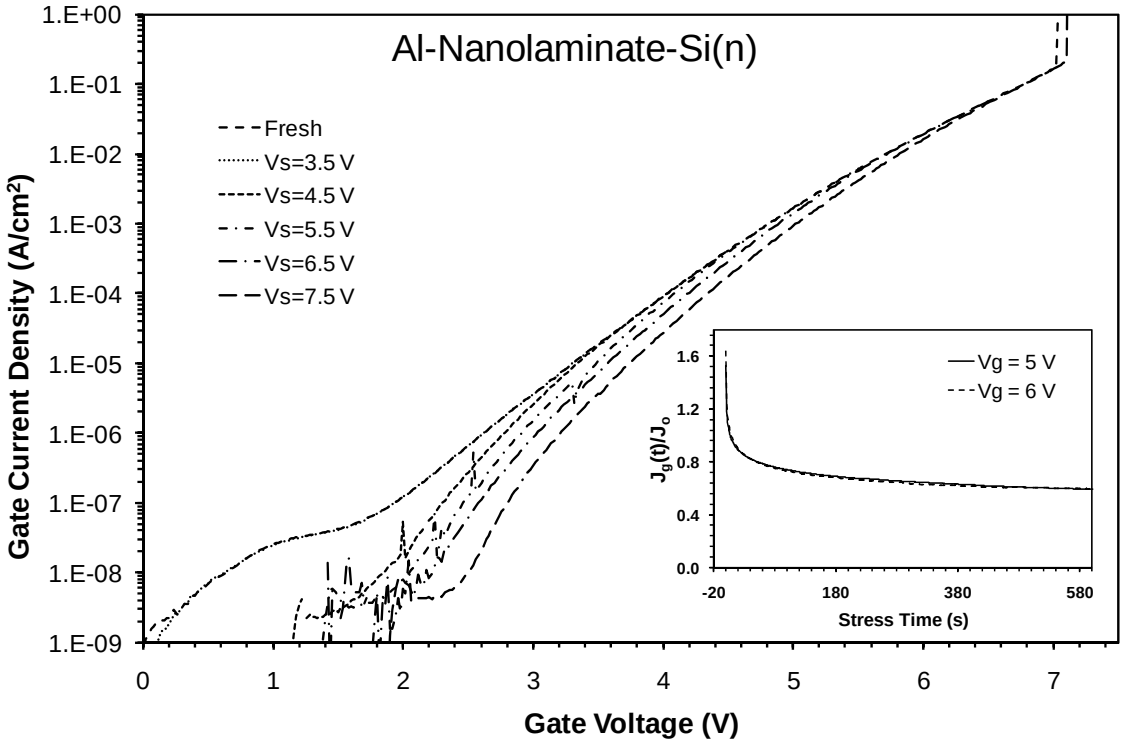
Al-Nanolaminate-Si(n)
Fresh
Vs=3.5 V
Vs=4.5 V
Vs=5.5 V
Vs=6.5 V
Vs=7.5 V
Gate Current Density (A/cm²)
Gate Voltage (V)
1.E+00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
1.E-06
1.E-07
1.E-08
1.E-09
0
1
2
3
4
5
6
7
Vg = 5 V
Vg = 6 V
Jg(t)/Jo
Stress Time (s)
1.6
1.2
0.8
0.4
0.0
-20
180
380
580

Figure 5(c)

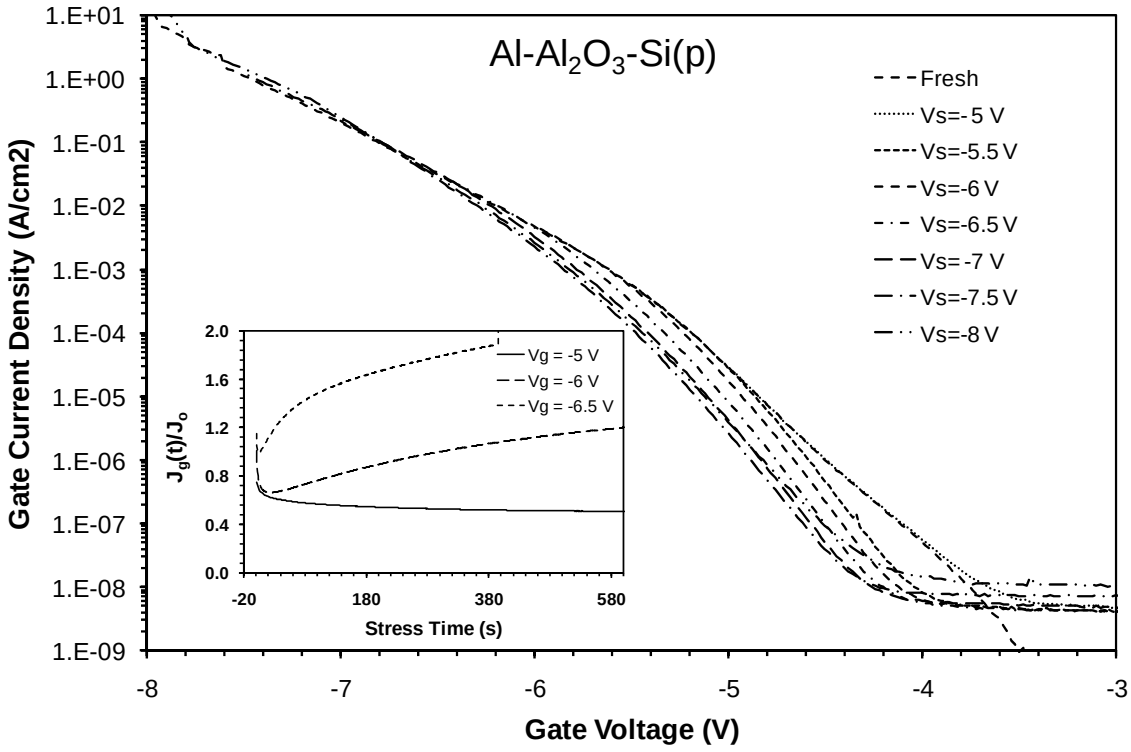
Al-Al2O3-Si(p)
Fresh
Vs=- 5 V
Vs=-5.5 V
Vs=-6 V
Vs=-6.5 V
Vs= -7 V
Vs=-7.5 V
Vs=-8 V
Gate Current Density (A/cm2)
1.E+01
1.E+00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
1.E-06
1.E-07
1.E-08
1.E-09
-8
-7
-6
-5
-4
-3
Gate Voltage (V)
Vg = -5 V
Vg = -6 V
Vg = -6.5 V
Jg(t)/Jo
2.0
1.6
1.2
0.8
0.4
0.0
-20
180
380
580
Stress Time (s)

Figure 6(a)

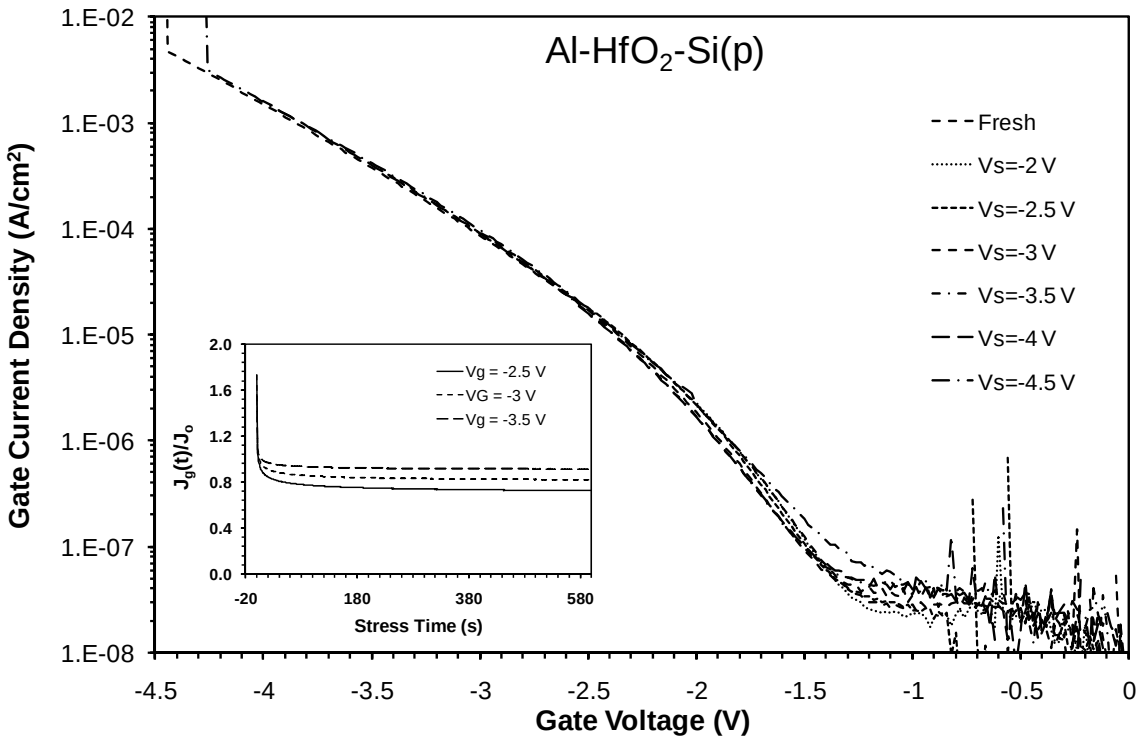
Al-HfO2-Si(p)
Gate Current Density (A/cm2)
Gate Voltage (V)
1.E-02
1.E-03
1.E-04
1.E-05
1.E-06
1.E-07
1.E-08
-4.5
-4
-3.5
-3
-2.5
-2
-1.5
-1
-0.5
0
Fresh
Vs=-2 V
Vs=-2.5 V
Vs=-3 V
Vs=-3.5 V
Vs=-4 V
Vs=-4.5 V
Vg = -2.5 V
VG = -3 V
Vg = -3.5 V
Jg(t)/Jo
Stress Time (s)
2.0
1.6
1.2
0.8
0.4
0.0
-20
180
380
580

Figure 6(b)

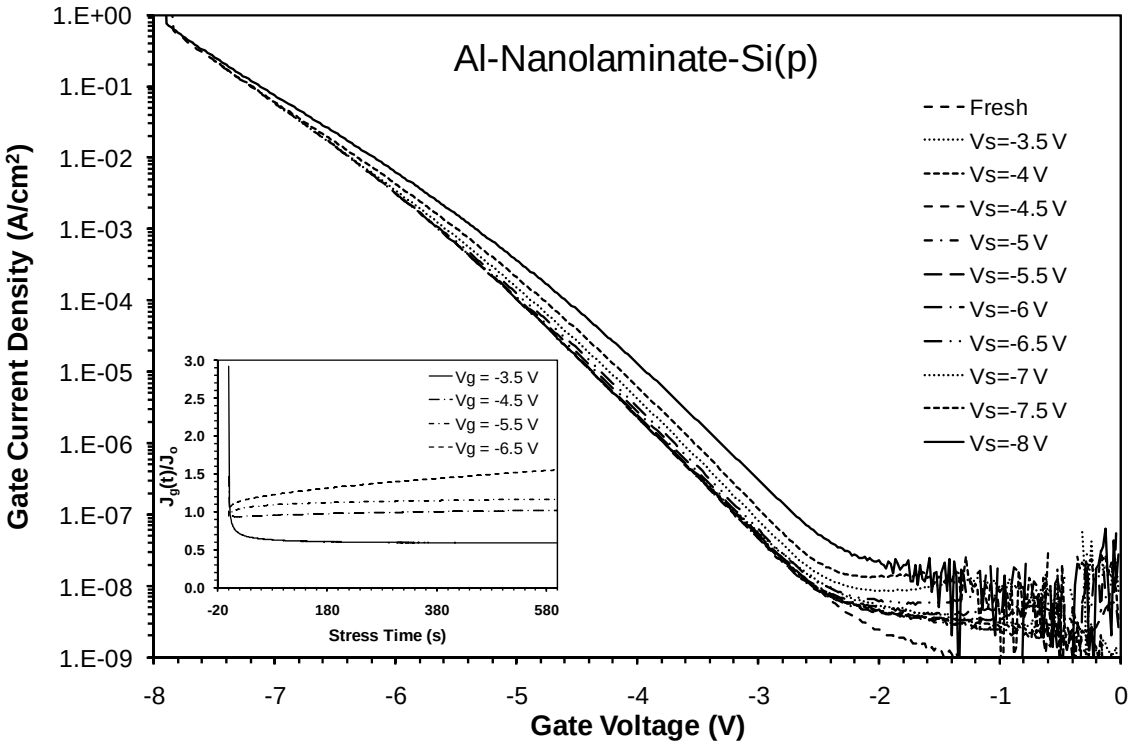
Al-Nanolaminate-Si(p)
Gate Current Density (A/cm²)
Gate Voltage (V)
1.E+00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
1.E-06
1.E-07
1.E-08
1.E-09
-8
-7
-6
-5
-4
-3
-2
-1
0
Fresh
Vs=-3.5 V
Vs=-4 V
Vs=-4.5 V
Vs=-5 V
Vs=-5.5 V
Vs=-6 V
Vs=-6.5 V
Vs=-7 V
Vs=-7.5 V
Vs=-8 V
Vg = -3.5 V
Vg = -4.5 V
Vg = -5.5 V
Vg = -6.5 V
J_g(t)/J_o
Stress Time (s)
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-20
180
380
580

Figure 6(c)