Radiation Tolerance of NROM Embedded Products

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***Abstract*—Radiation tolerance of NROM memories is demonstrated at the level of industrial 4 Mbit memory embedded modules, specifically not designed for operation in radiation harsh environments. The memory fabricated in 0.18 um technology remains fully functional after total ionization doses exceeding 100 krad. The tests were performed by irradiating with γ-rays (^{60}Co source) and 10 MeV ^{11}B ions in active (during programming/erase and read-out) and passive (no bias) modes. Comprehensive statistics were obtained by using large memory arrays and comparison of the data with the parameters of irradiated single cells allowed deep understanding of the physical phenomena in the irradiated NROM devices for both moderate (<1 Mrad) and large (>1 Mrad) TID. The obtained data is currently employed in the design of the new generation of NROM memories, having improved radiation tolerance**

***Index Terms*—Floating gate memories, ONO, radiation effects, radiation hardening.**

I. Introduction

RADIATION effects in MOS devices are mostly manifested as charge trapping in the dielectric layers and at the interfaces. Charges are captured by the initially existing or generated in the same irradiation process defects. MOSFET parameters are degraded, sometimes resulting in total failure of logic gates or analog elements [1]–[3]. The nonvolatile memories based on the polysilicon floating gate (FG) principle are especially sensitive to the ionizing radiation. The radiation induced defects in the gate silicon dioxide may result in the formation of percolation paths responsible for the gate leakage current [4]. Even one high resistance leakage path is a principal endanger of the retention capability of the Flash memory with a conductive FG. This strongly limits the ability to scale down the thickness of the FG memory bottom oxide since the probability of the leakage path creation strongly increases with the oxide thickness (TOX) decrease. Most FG memories in strongly scaled down technologies work with the bottom oxides of 80–85 Å minimum thickness.

Nitride based memory are free from the aforementioned limitation. They were reported to have better radiation immunity compared with EEPROM polysilicon FG devices due to storage of information charge at traps in the nitride layer [5]. Even if a leakage channel is created, this results only in a small decrease of the charge in the silicon nitride layer. Silicon-nitride-oxide-silicon (SNOS) and silicon-oxide-nitride-oxide-silicon (SONOS) structures have been widely used in the non-volatile memories (NVM) intended for operation in the radiation hardened military and space systems [5], [6], [20]. Some of the SNOS transistors could be programmed and remained functional after irradiation to a total ionization dose (TID) of more than 1000 Mrad [5].

The dominant SONOS-like technology at the NVM market is NROM (nitride read-only memory) [7]. It features significant memory density increase compared with classical SONOS by storing information as charge packages in silicon nitride at both transistor channel edges. Programming of NROM (by channel hot electrons-CHE) and the read operation are performed in opposite directions. The memory array has a field less cross-wise organization. Unlike other nitride NVM, the bottom oxide of NROM (BOX) is relatively thick ($\sim$ 70 Å), thus ensuring excellent retention, suppressed read disturb and much easier scaling compared with the polysilicon FG memories [8]. Recently, results on NROM single cells and SONOS capacitors with thick BOX subjected to irradiation were reported [9]. Radiation tolerance exceeding 500 krad was demonstrated for SOI single memory cells [10]. Little is known about NROM product radiation hardness. A limited characterization of some commercial NROM products from different technology nodes in heavy ion environment (with focus on periphery performance) was reported in [11].

This paper reports a systematic study of both NROM products and single cells subjected to different types of radiation and reflects the major trend of space and military system designers to accommodate the existing commercial products to the needs of harsh-environment applications [12]. We report the results of radiation immunity testing for Tower Semiconductor's 0.18 um *micro*FLASH NROM technology. In contrast to the previous publications, we place emphasis on the changes happening under irradiation in the NROM memory arrays and report the correlation of the array performance with the characteristics of irradiated single cells. The peculiarities of the NROM

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technology that define the TID immunity of this memory type are discussed. The study had the following main goals:

(i) To select the NROM technology flavors that guarantee optimal radiation immunity of NVM products

(ii) To evaluate radiation tolerance and qualify the optimized products for special applications

(iii) To reveal the dominant physical mechanisms responsible for the functionality and reliability of NROM products in radiation environments.

II. EXPERIMENTAL

Two sources of radiation were used in the laboratory modeling of a space environment. Most of the experiments were performed by irradiating the NROM products with γ-rays in the range of absorbed doses (Si) 10–100 krad and monitoring their functionality in the course of and after irradiation. A part of the memory devices was subjected to high radiation doses ($\geq$1 Mrad) to examine the functional limits of the technology. γ-irradiations were performed in Ben Gurion University, Israel and CNEA-Buenos Aires, Argentina using ^{60}Co sources with a dose rate of the order of 200 rad/min.

The experiments emulating other radiation environments were performed using high-energy Boron ions. Ion irradiations were performed in the IMM-CNR Catania, Italy using 10 MeV $^{11}\mathrm{B}$ ions (3.9 $\mathrm{MeVcm^2/mg}$ LET) with the fluence of $10^8 - 5 \times 10^{11}\ \mathrm{cm}^{-2}$ (flux $\sim 10^6\ \mathrm{cm^{-2}s^{-1}}$) perpendicularly to the specimen surface. The Boron doping effects of the silicon substrate were negligible even for the highest doses. All irradiations were performed at room temperature. NROM single cells (mini-arrays) and *micro*FLASH 4 Mbit embedded memory product (Topaz) fabricated in 0.18 $\mu\mathrm{m}$ technology were examined.

The total volume of the 4 Mbit embedded Flash memory is divided into 16 equal sectors. A sector includes a contactless array with the orthogonal systems of word and bit lines (256 $\times$ 1032, respectively) and CMOS periphery. The last contains bit line (BL) and word line (WL) drivers, power switches and charge pumps, sense amplifiers and reference cells. Each sector is controlled separately. It can be programmed/erased or readout independently of other sectors. Such internal structure of the product significantly widens its testability in radiation environments.

The single cell with typical dimensions $\mathrm{W} \times \mathrm{L} = 0.18 \times 0.42\ \mu\mathrm{m}^2$ is the basic element of the full-sized product. The unique design allows storage of two bits of information in one memory cell, thus allowing it to double the memory density (8 Mbit instead of 4 Mbit). The dielectric properties of the ONO stack prevent charge loss from silicon nitride and assure bit separation and high endurance/retention of the memory cells. Unlike the traditional SONOS with Fowler-Nordheim injection, program/erase operations in NROM are performed using CHE for electrons and Band to Band Tunneling (BBT) for holes.

To emulate the features of a real NROM cell in a product, each single cell in the test chips was placed in the middle of a 3 $\times$ 3 miniarray. In order to control the possible effects of lateral charge spread in the nitride layer, single bit programmed pattern (AAAA-hexadecimal code) was taken as a base (4 Mbit Topaz NVM modules). Devices were programmed and measured before and after each irradiation. Array threshold voltage distribution (in a case of array $\mathrm{V_t}$ is the gate voltage at which the cell current equals the current of the reference cell) or currents of programmed/erased cells in full-sized arrays were monitored using a MOSAID tester. In single cell measurements, the threshold voltage shift $(\Delta \mathrm{V_t})$ and leakage currents were measured in forward and reverse directions. At least ten identical cells were measured to obtain statistically significant results when irradiating in the studied range of absorbed doses and ion fluences.

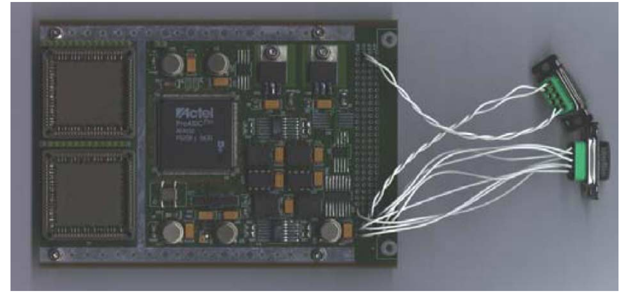

Fig. 1. A view of the autodiagnostic board developed for NROM product qualification. The board exists in two versions that use standard and rad-hard components (the latter is intended for tests in space missions and special qualifications). Lead shielding box is used in earth experiments, allowing the access of γ-radiation and ions only to the investigated NROM chips.

ONO capacitors with the area of $200 \times 200\ \mu\mathrm{m}^2$ (effective ONO stack thickness $\sim$ 190 Å) were used to distinguish the effects connected with radiation stimulated charge trapping in the ONO stack itself and at the memory cell edges (spaces between the WLs). Capacitors were also used for testing of ONO stack radiation immunity for doses above 1 Mrad. To study the influence of radiation on memory retention parameters and investigate the annealing of radiation induced charging in CMOS periphery [13], bakes at 150–250°C were performed. The degradation of the silicon/ONO stack interface was monitored by a charge pumping technique (control of the density of traps generated at $\mathrm{Si - SiO^2}$ interface and in the bottom oxide of ONO, see comments in Fig. 7).

TID tests of electronic components were performed in active (with bias) and passive (no bias) modes. A special autodiagnostic board operated in the remote control regime (Fig. 1) was used in the active mode measurements. The board and specially developed software allowed irradiation and measurements to be performed in a real-time regime and supported data readout, program/erase, registration, analysis of failures, etc. Two chips were exposed to irradiation on a board. One of them was addressed inside the $^{60}\mathrm{Co}$ γ-setup, while the other was irradiated in a passive mode and used as a reference (for comparison of device degradation in active and passive modes). It was revealed that the charge loss of the programmed cells in the radiation environment was similar in active and passive testing. Thus, passive mode was widely used for the express radiation immunity testing. This allowed collection of the necessary statistics of radiation damage in the wide range of doses and radiation conditions.

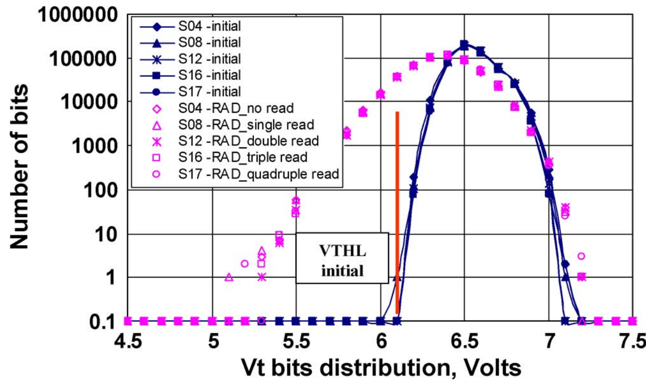

Fig. 2. Initial V_t cells distribution of 5 large Topaz sectors programmed in 0000 pattern: initial (dark blue symbols), and immediately after γ-irradiation with a dose of 60 krad (magenta symbols). Different readout regimes were provided for different sectors. A solid vertical line shows the edge of initial programmed cells V_t distribution (VTHL is the lowest V_t in the programmed part of the array).

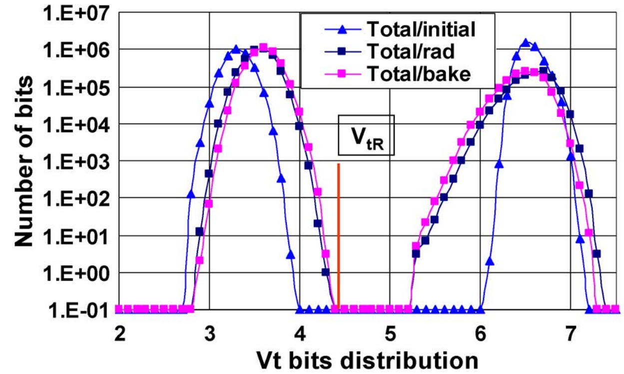

Fig. 3. V_t distribution of Topaz: i) initial (dark blue symbols); ii) immediately after irradiation with a TID 80 krad (black symbols); iii) after a post radiation retention bake 250°C for 1 hour (magenta symbols). The shift of the erased part of the V_t distribution is connected with the charge loss in the reference cell. A solid vertical line shows the position of reference cell V_{tR}.

III. Experimental Results

The initial irradiation experiments were performed both with the 0.18 μm NROM memory products and older 0.5 μm NROM technology devices. The radiation immunity of 0.18 μm memories appeared to be significantly higher. The difference could be attributed to higher quality of dielectrics filling the gaps between the WLs in the cross-wise memory arrays (spacer dielectrics and a part of the pre-metal dielectric). Different types of WL gap filling dielectrics in 0.18 μm NROM also resulted in different radiation immunity. The best gap filling dielectric combination was chosen. The reported results are for the optimized NROM memories.

Experiments with different irradiation sources (γ-rays and ^{11}B ions) revealed similar changes of device parameters. We divided all the obtained data into two groups:

- Radiation effects at tolerant fluence and TID ($\leq$100 krad) when the products remain fully functional (Section III-A).
- Radiation damage at "extended" fluence and TID ($\geq$1 Mrad) when NROM memory product is strongly damaged due to CMOS periphery failures. In this case, NROM characteristics were examined mostly on single cells and capacitors (Section III-B).

It will be shown below that NROM products can potentially withstand TID above 100 krad but require specially designed transistors in the CMOS periphery.

A. Irradiation With Tolerant Fluence and TID ($\leq$100 krad)

Fig. 2 shows the initial V_t distribution in five separate sectors programmed in 0000 (hexadecimal code) pattern (all cells are programmed) before and after 60 krad γ-irradiation. Irradiation was performed in the active mode. A special recurring readout regime was employed during irradiation (sequential addressing of the sector resulted in differed times of read-outs: single, double...). Thus, the memory cells in different sectors experienced the read-out voltages for different times.

- No readout—sector S04 (actually, passive regime)
- Single readout—sector S08
- Double readout—sector S12
- Triple readout—sector S16
- Quadruple readout—sector S17

As mentioned above, the test board allowed irradiating of two chips simultaneously (one in the active mode and the other in passive mode). The following conclusions were done from the evolution of V_t distributions of both chips:

Radiation impacts the program margin (~1.0 V margin loss after 60 krad).

The margin loss does not depend on the regime of the readout. It means that most of the programmed cells lose their charge (or positive charge is trapped), but the mechanism of radiation induced charge loss is not sensitive to the bias applied to the cell terminals (the readout gate and drain voltages are ~4.4 V and 1.8 V, respectively).

No difference in margin loss was found in sectors irradiated in passive and active modes (for instance, compare sectors S04 and S12 in Fig. 2). However, active mode results in a significant increase of standby current (about one and a half orders of magnitude) in the CMOS periphery. The following anneal at 150°C for 24 hours returns the standby currents to their initial values.

Fig. 3 demonstrates the V_t cell distributions of the whole memory array programmed in an AAAA (CKB-checkerboard) pattern and measured prior and after the irradiation with the dose of 80 krad. In the CKB pattern, the number of cells in programmed and erased states is equal. Under irradiation, the distribution curves of both states shift towards each other, thus decreasing the window margin (the discussion of this behavior is provided later). The post irradiation retention bake additionally decreases the program margin (~0.1 V) and erase margin (~0.05 V). The observed shifts correspond to additional charge loss or redistribution of charges in the ONO stack or at the periphery (edges) of the memory cells. In particular, the low V_t increase can be in part attributed to the "rebound" effect when the hole charge is annealed while the remaining negative charge trapped in ONO at $\mathrm{Si-SiO^2}$ interface and the edges of the cell results in the V_t increase [14]. Nevertheless, no degradation of memory retention was observed even after 80 krad irradiation. The NROM memory remains fully functional: no readout mistakes were observed, and the array could be reprogrammed in the standard regime. After the flash erase and bake (to recover

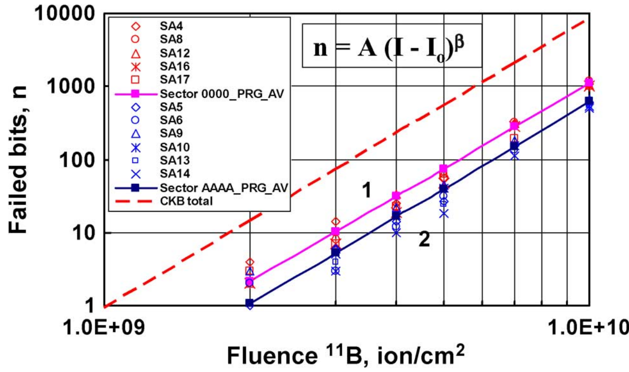

Fig. 4. The rate of failed bits generation versus the fluence of $^{11}\mathrm{B}$ ions with the energy of 10 MeV. Curves 1 and 2 demonstrate the dose dependence of faults in sectors programmed in 0000 and AAAA patterns, respectively. Curves are obtained by fittings through the averaged points. The dash line manifests the predicted dose dependence of a product.

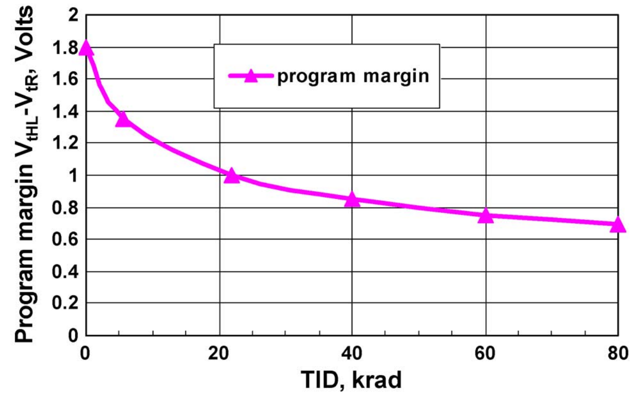

Fig. 5. The dependence of the program margin loss $(\mathrm{V_{tHL}} - \mathrm{V_{tR}})$ versus the dose of γ-irradiation (here $\mathrm{V_{tHL}}$ and $\mathrm{V_{tR}}$ are defined in Figs. 2 and 3).

the standby current) the irradiated array behaved as the specimen before irradiation.

The analysis of cells that form the tail of $\mathrm{V_t}$ distribution (Fig. 3) shows that these cells are scattered uniformly over all sectors of the memory product and their location does not depend on the position of a cell in the memory array (center, or periphery).

As it was revealed in $^{11}\mathrm{B}$ irradiation tests, the number of failed words grows proportionally with the number of programmed cells. Curves 1 and 2 in Fig. 4 demonstrate the number of fails in sectors with 0000 and AAAA patterns, respectively, versus the ion fluence. The 0000 pattern doubles the number of programmed cells compared with AAAA. The probability of failures also increases twice (curve 1). This is consistent with the fact that radiation induced positive charge accumulation is a random process having a spatial statistical character. The number of fails $\mathbf{n}$ depends on the ion fluence $\mathbf{I}$ as a power low:

$$\mathbf{n} = \mathbf{A}(\mathbf{I} - \mathbf{I_O})^{\beta}$$

where $\mathbf{A}$ is a constant specific for the cell and the type of irradiation; $\mathbf{I_o}$ manifests the threshold fluence resulting in the first bit error; β is a power index ≈4.

Taking into account the specifics of failed bit generation, we can predict the threshold fluence for a product programmed in a typical AAAA (CKB) pattern. The threshold fluence for a whole memory array programmed in AAAA pattern (red dashed line in Fig. 4) is equal to $\sim 1 \times 10^9\ \mathrm{ions/cm^2}$ and this corresponds to the bit error cross section $\sim 5 * 10^{-16}\ \mathrm{cm^2/bit}$ (approximately three orders of magnitude better than for heavy ion testing with the same LET on 220 nm technology [11]). It is clear that the radiation tolerance can be strongly increased in a case where redundancy or error correction codes are used in the product design. These features are absent in Topaz. Otherwise, the amount of failures depends on the number of programmed bits, so it is clear that the threshold fluence $\mathrm{I_o}$ is higher for smaller arrays.

In the case of γ-irradiation, the threshold TID for readout is above 100 krad. This follows from Fig. 5 which shows the decrease of the memory window (program margin) versus the dose of γ-exposure. The margin decrease starts to saturate for >40 krad. At 80 krad, there is still ∼0.7 V window (Figs. 3 and 5). The TID tolerance of *micro*FLASH exceeds the data presented in [11] (including 90 nm NROM array). The 100 krad γ-irradiation results in the NROM product margin loss similar to the influence of $\sim 1 \times 10^9\ \mathrm{cm^{-2}}$ of 10 MeV Boron ions.

An additional manifestation of the radiation damage is the increase of the offset (drain leakage) current in the programmed/erased memory cells. Both drain and source currents were measured. They were equal, thus showing that the leakage was between source and drain (Fig. 6). This phenomenon is observed both in programmed and erased single cells and memory arrays (bit line to bit line leakage is measured in NROM cross-wise arrays) and can not be explained by charge trapping in the ONO stack since leakages increase also in the programmed cells. The leakage is partially annealed during the post radiation bake at 150–250°C. We attribute the effect to positive charge trapped at the sides of the memory cell (between the word lines). This is consistent with no leakage effect in SOI single cells even at significantly higher TID ∼500 krad [10]. The effect is similar to generation of positive charge in the low quality isolation silicon oxides (field oxide-FOX or shallow trench isolation-STI), known as one of the main degradation mechanisms in the irradiated CMOS circuits with standard MOS transistor design [3], [13]. For large fluences of $^{11}\mathrm{B}$ and high TID (>500 krad) the leakages sometimes become irreversible and probably additional degradation mechanisms are added to charge trapping effects (see Section IV).

The charge pumping (CP) measurements (Fig. 7) performed on single cells irradiated with γ-rays up to the TID of 100 krad did not reveal pronounced changes of the surface state density (within the accuracy of CP measurements $\sim 10^{10}\ \mathrm{cm^{-2}eV^{-1}}$). The peak connected with the surface states at Si-bottom oxide interface of ONO [15] is shown in the inset of Fig. 7 (this example is for 30 krad TID).

Similar to the Topaz product measurements, the decrease of the $\mathrm{V_t}$ of the programmed state after irradiation was observed for NROM single cells. This shift increases with the Si absorbed dose and corresponds to the decrease of the electron charge or trapping of positive charge in the memory bit location (Fig. 8).

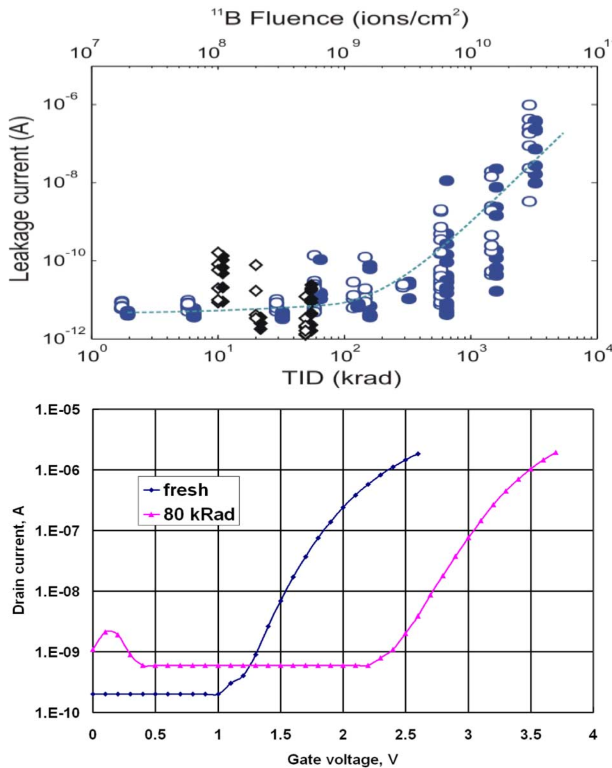

Fig. 6. The change of the leakage current (I_{off}) in the irradiated memory cells (one-bit programmed NROM cells are considered): a) Single cells exposed to γ-rays and Boron ions—black♦and blue ● symbols, respectively; source-drain leakage current was measured as a function of the total absorbed dose and ^{11}B fluence in two directions, forward (open symbols) and reverse (closed symbols); b) Bit line to Bit line leakage in the memory array: (1)—fresh selected cell, (2) after programming and 80 krad γ-irradiation.

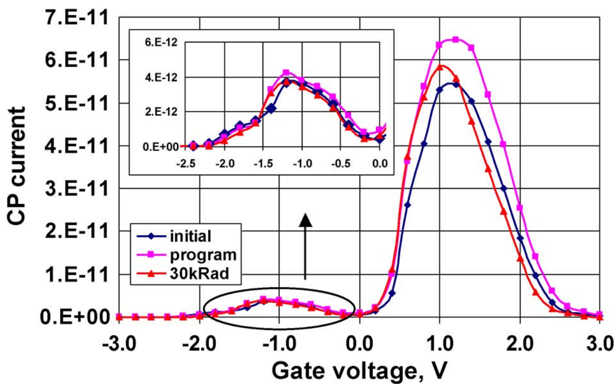

Fig. 7. Charge pumping measurements of a typical single cell: fresh cell (1-blue), after programming (2-red) and after 30 krad γ-irradiation (3-violet). CP was performed with a constant amplitude of 3 V while the pulse base varied from 6 to 3 V. Trapezoidal pulses with the frequency of $f = 1$ MHz were applied to the gate of the memory cell. Bulk current of the fresh and irradiated NVM transistors were measured. The signal is proportional to the density of the surface states.

The observed phenomenon is consistent with the data reported in [11].

It follows from Fig. 8 that the V_t decrease effect for programmed bits is much higher in the reverse readout (standard for NROM). This indicates that the trapped charge in ONO interacts electrostatically with electrons and holes created in the irradiation process procedure. Such interaction explains the changes of

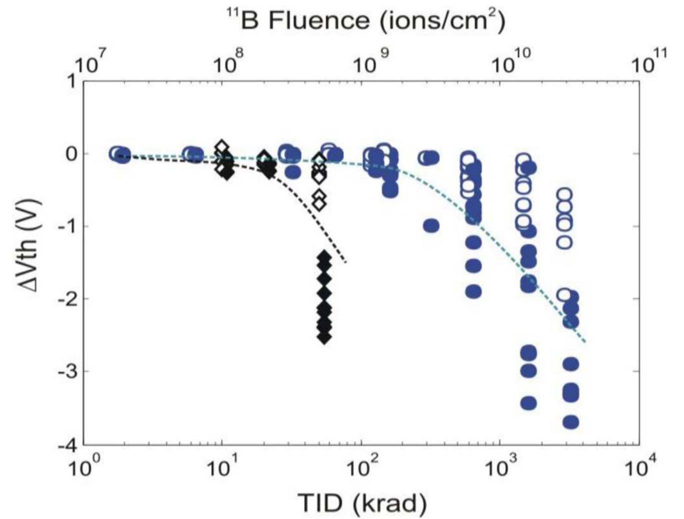

Fig. 8. V_t decrease as a function of the TID (in krad) and ^{11}B fluence for programmed cells: γ-rays (black♦) and ^{11}B ions (blue ●) for forward (open circles) and reverse (closed circles) readout conditions.

V_t distribution in the array during irradiation (Fig. 3). The rate of V_t shift is different for cells in a programmed state, erased state and partially (intermediate) programmed reference cells. The negative charge loss is higher for cells having higher V_t before the irradiation. This fact gives a plausible explanation for the observed decrease of both program and erase margins shown in Fig. 3.

The V_t decrease (both in reverse and forward read-out) indicates trapping of positive charge in ONO and/or in the dielectric between the WLs. To distinguish the cell periphery (edge) effects, measurements of large area ONO capacitors were performed. Fig. 9(a) shows the C-V characteristics of $200 \times 200\ \mu m^2$ NMOS capacitors irradiated to TID of 5 Mrad (γ-rays). Unlike the NROM single cells, the capacitors had no gate protection against the in-process plasma charging. Thus, prior to the irradiation they were already strongly "programmed"- charged negatively (curve 1). After 5 Mrad, the effective ONO-Si interface charge was slightly positive-curve 2 ($\Delta V_{fb} \sim 0.5$ V). The positive charge did not completely disappear after 250°C bake for 2 h (compare curves 2, 3 respectively). Nevertheless, the capacitors could be programmed (negative charge in ONO) by applying negative bias of ~18 V to the control gate (curve 4). A consequent 250°C bake for 1 hour (curve 5) shows that excellent charge retention is preserved even after very high TID. No pronounced degradation of SiO_2-Si interface was manifested since the slope of C-V characteristics (curves 1–5) did not change. This is consistent with the results of CP measurements (Fig. 7). I-V characteristics also did not show any signs of ONO stack degradation (Fig. 9(b), curves 1 and 2).

Summarizing the results observed in irradiated ONO area capacitors, it can be concluded:

1) No significant change in programmability, i.e. in trap concentration of nitride layer, was found after very high TID.
2) Integrity and retention parameters of ONO stack did not show signs of degradation; the parameters of ONO interfaces with poly and substrate were also not changed.

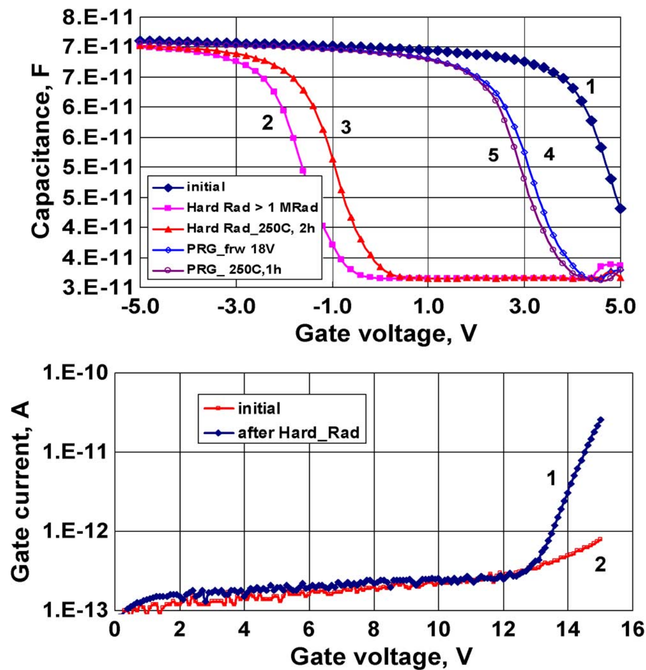

Fig. 9. Characteristics of the ONO capacitor $(200 \times 200\ \mu\mathrm{m}^2)$ after 5 Mrad γ-irradiation: (a) C-V characteristics of the fresh capacitor (1); after 5 Mrad γ-irradiation (2); bake at 250°C for 2 hour (3); electron injection by a −18 V/10 ms gate pulse (4); the following 250°C bake for 1 h (5); (b) I-V characteristics of the fresh capacitor and after its irradiation (curves 1 and 2, respectively).

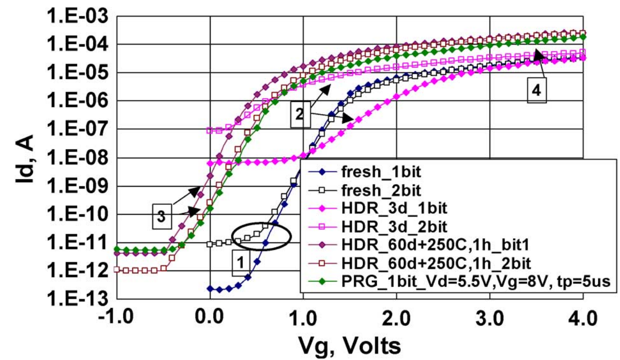

Fig. 10. Evolution of the initial (1) $\mathrm{I_D - V_G}$ characteristics of the memory cell; (2)-after γ-irradiation with a dose of ∼5 Mrad; (3)-after room temperature storage and 250°C bake for 1 h; (4) after an attempt to program in standard for a typical cell conditions. Fig. 11 Source/drain characteristics of the NROM cell exposed to γ-dose of 5 Mrad: BVDss characteristics ($\mathrm{I_D}$ vs. $\mathrm{V_D}$ at $\mathrm{V_G} = 0$) measured in forward (bit 1) and reverse (bit 2) directions prior (curves 1, 2) and after (curves 3, 4) irradiation; reverse current of source/drain diodes to bulk measured in fresh cell (curve 5) and after irradiation (curve 6).

3) After 5 Mrad, ONO stack completely loses the negative charge and is charged positively. The accumulated positive charge only partly disappears after the bake. Since a periphery effect in large ONO capacitors is negligible, this is evidence of hole trapping in the silicon nitride layer. A plausible explanation of hole trapping mechanism was proposed in [5] and will be discussed in Section IV.

A) Irradiation With High Ion Fluences and γ-Ray ≥1 Mrad TID: At high radiation doses (TID $\geq$ 1 Mrad, or fluence $\sim 10^{11}\ \mathrm{ions/cm^2}$) the functionality of memory products was severely degraded. Though the readout operation of some chips still could be performed after the device anneal at 250°C, the stored information was corrupted and re-programming of the memory cells was impossible. Thus, most of the studies at high radiation doses were done using single memory cells and capacitors. Some of the results obtained with large area ONO capacitors were reported in Section III-A. In the case of single memory cells, there is a significant spread of characteristics. However, several observations are statistically significant and the following conclusions can be made (illustrated by Fig. 10):

1) After 5 Mrad TID, the values of $\mathrm{V_t}$ for single cells (curves 2) show large scattering around the initial $\mathrm{V_t}$ (curves 1). The shifts may be different for two bits of the same memory transistor. The $\mathrm{I_{off}}$ values for most cells were strongly increased. A long-term storage at room temperature or/and bake at 250°C for 1 hour reduce $\mathrm{V_t}$ values to 0.5–1.0 V (curves 3). This is less than for regular NMOS transistors with the identical TOX. The studies of ONO capacitors irradiated in the same regime showed that the ONO interface with the substrate, charge trapping in silicon nitride and retention parameters were not degraded significantly. Similar to ONO capacitors, the programmed memory cells lost their information and were charged slightly positive after the irradiation. Radiation induced loss of charge is accompanied by the dramatic increase of the leakage current, $\mathrm{I_{off}}$, that almost disappears after the bake (curves 2 and 3). The last peculiarity of $\mathrm{I_D - V_G}$ characteristics after irradiation and bake are attributed to charging/discharging at the NROM cell side edges (similar to <100 krad doses, but the leakage effect at high doses is much more pronounced). Actually, this may be considered as connecting a parasitic device in parallel with the channel of the main transistor

2) Annealing at 250°C results in an increase (3–4 times) of the saturation drain current $\mathrm{I_{dsat}}$ of the memory transistors. The effect does not depend on the initial charge state of the memory bit and $\mathrm{I_D - V_G}$ curve position after irradiation (curves 2 and 3). This phenomenon is discussed in Section IV.

3) Programming of the irradiated cell (after the bake) is strongly degraded (curve 4). Negligible $\mathrm{V_t}$ shift is observed in the conditions leading to the strong programming of a fresh cell ($\mathrm{V_D} = 5.5$ V, $\mathrm{V_G} = 8$ V, $\mathrm{t_p} = 5\ \mu$s). Taking into account the radiation tolerance of ONO stack, this degradation suggests changes of electrical fields in the CHE injection areas. It is necessary to note that memory cells could still be programmed in a SONOS regime (F-N injection) by applying high voltage (above 18 V) to the polysilicon gate (devices without gate protection limiting the applied voltage).

4) Connected in parallel, source/drain reverse currents decrease after irradiation (Fig. 11, curves 5 and 6). At the same time, a strong degradation of BVDss characteristics ($\mathrm{I_D}$ vs. $\mathrm{V_D}$ at $\mathrm{V_G} = 0$) was observed in several cells (the punch through effect). Fig. 11 (curves 1, 2 and curves 3, 4) presents the $\mathrm{I_D - V_D}$ characteristics measured in both directions in a fresh cell and after its post-radiation bake, respectively. The effects can be attributed to effective channel length decrease in the irradiated transistors.

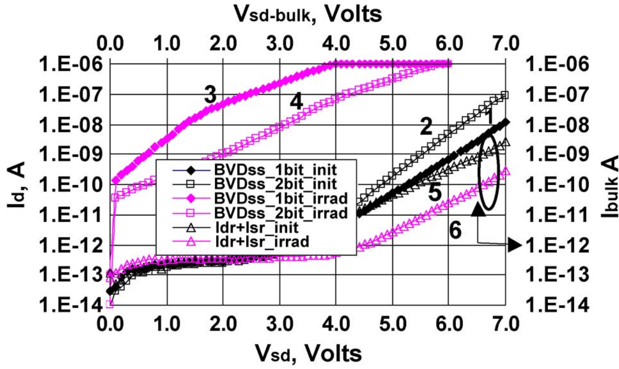

Fig. 11. Source/drain characteristics of the NROM cell exposed to γ-dose of 5 Mrad: BVDss characteristics (I_D vs. V_D at $V_G = 0$) measured in forward (bit 1) and reverse (bit 2) directions prior (curves 1, 2) and after (curves 3, 4) irradiation; reverse current of source/drain diodes to bulk measured in fresh cell (curve 5) and after irradiation (curve 6).

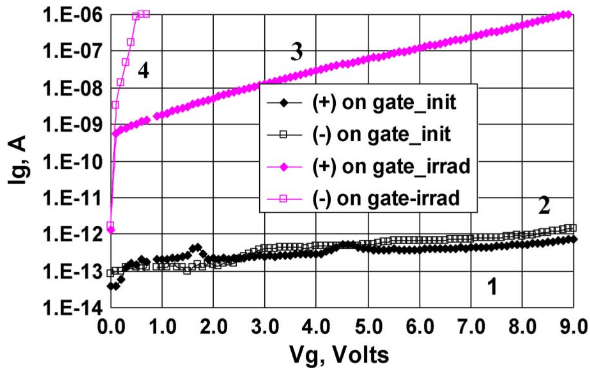

Fig. 12. Reverse currents of the protection diodes measured in a fresh single cell (curves 1 and 2) and after 5 Mrad γ irradiation (curve 3 and 4).

5) In addition to the channel area, irradiation degrades the rectifying properties of the protection diodes (Fig. 12). One of them lost its rectifying properties (curve 4), while the reverse current of the other one dramatically increased (compare curves 3, 4 with the curves 1, 2 of the fresh cells). Nevertheless, the protection diode still allows the positive 9 V bias on the NROM transistor gate needed for programming. The leakage may be attributed to the charge trapped in the passivation layer.

Summarizing the results, we can conclude that the high dose $(\mathrm{TID} > 1\ \mathrm{Mrad})$ radiation damage has irreversible character and results in the loss of NROM cell programmability. The irreversible damage is accompanied by the strong leakage degradation. As in the case of CMOS degradation, this leakage is at least partially recovered by long-term room temperature annealing or short-term bakes at 250°C [16].

IV. Discussion. Mechanisms of Radiation Damage at Low and High Doses

In the case of doses <100 krad (Section III-A), the dominant effect of radiation on programmed cells is manifested as the decrease or compensation of the negative charge trapped in the nitride layer of the ONO stack. It was emphasized that the charge loss is higher for larger V_t of the cell prior to irradiation. Two possible mechanisms working together or being dominant one over another could be proposed to explain the observed phenomena:

1) Interaction of electron-hole pairs created in the ONO stack by the ionizing radiation with the trapped charge
2) Lateral spreading of the locally trapped charge in the nitride layer

The first mechanism is similar to the one proposed in [5] to explain the charge loss in SNOS structures. It is typical for all SONOS devices. The other mechanism is specific for NROM cells and arrays where information is stored as localized charge packages in the source and drain regions of ONO transistors.

According to the first mechanism, the electron-hole pairs generated in the ONO or diffused into ONO from the surrounding materials are separated by the electric field in the ONO under the WL. The electric field of the negatively charged ONO in the programmed cell stimulates separation of generated carriers (suppresses recombination) and pulls the holes into nitride. The holes are accumulated in the nitride layer and compensate the negative charge. The difference from the traditional SONOS consists in the influence of the locally stored negative charge on hole trapping.

The role of lateral charge spread (mechanism 2) was investigated by monitoring $I_D - V_G$ characteristics of memory array cells in both directions. Spreading of locally trapped negative charge inside the channel would decrease the V_t of one (programmed) bit and increase the V_t of the neighbor bit in the same memory transistor. It means that in the patterned AAAA (CKB) one bit per cell mode and then irradiated memory array, the currents in the non-programmed cells with two "1" bits will change stronger compared with the "1" bit pattern (readout in the direction of programming). Fig. 13 shows the result of the performed experiment. One can see that an opposite situation is registered. It is the result of the known in NROM "second bit effect": an increase of the V_t of the erased bit as a result of its neighbor programming. Thus, if the spreading of local charge does exist under the irradiation, it is not the dominant effect.

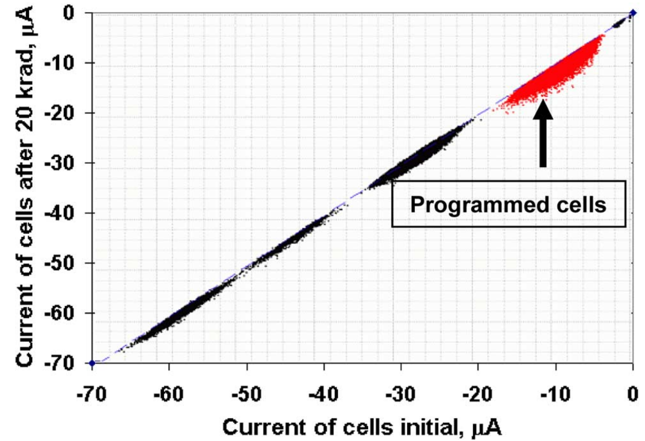

Fig. 13. Dependence of the readout current ($V_r = 4.4$ V) of cells after irradiation (20 Krad) vs. the initial readout current in the erased cells (black spots), and programmed cells (red spots). The readout is in forward direction (erased bits tested). The graph shows the data for a whole sector (~0.5 Mbit) patterned in AAAA (CKB) mode.

Both low (<100 krad) and high (>1 Mrad) dose irradiation show reversible leakage current effects. The leakage increase can be annealed by long-term room temperature or short-term high temperature bakes. As mentioned above, increased leakages could be attributed to detrapping of positive charge at the edges of the irradiated NROM cells. Ionizing factor has a dominant role in this group of phenomena (trapping of generated electrons/holes by the existing and radiation induced defects).

The high dose radiation results in a more severe damage of single cells and NROM products. The cell ability to be programmed is deteriorated. There are several mechanisms that could explain the radiation stimulated changes in the heavily irradiated NROM devices: (i) ionization stimulated release of hydrogen atoms from dielectrics with subsequent passivation of boron in the substrate by hydrogen (B-H) complexes [17]; (ii) generation of intrinsic defects and impurity complexes due to displacement of atoms in interstitial positions (Frenkel defects) [2], [18], [19]; (iii) purely electrostatic effects connected with local redistribution of holes in ONO.

The first option was excluded on the basis of the following experimental facts:

(i) No changes in silicon nitride layer, which is the main supplier of hydrogen in the investigated systems (silicon nitride is known to have up to 10–20% of hydrogen in its chemical microstructure)

(ii) It is known that bakes at temperatures above 200°C destroy the B-H complexes [17]. In our case, bakes at 250°C did not lead to the recovery of the memory cells.

In the second scenario, Radiation Induced Diffusion (RID) of Boron and Phosphorous is considered. Created defects are the root course of enhanced low temperature diffusion of implants in Silicon. Radiation enhanced diffusion was reported, for example, in [18], [19] and references therein. Post radiation bake (at 250°C) stimulates RID of P and B atoms in $n-p$ junctions making these junctions less abrupt. As a consequence the cell programming efficiency by hot carriers is suppressed. Since the concentration of Phosphorus (source/drain) is much higher than Boron (channel), the $n-p$ metallurgical junction shifts inside the channel. The effective length of channel decreases resulting in the punch-through effect. Lower channel length is one of the reasons of the increased drain saturation current (Fig. 10). The other reason for the Id increase is the ~1 V V_t shift of the memory cell (positive charge accumulation).

In the third scenario, the charges trapped in ONO over the 700 A Bit Line oxide (BLO) move in the direction of the channel during the 250°C bake. Lateral migration of holes is the result of potential difference between the BLO and channel areas (the same density of trapped holes over the BLO and the channel area is supposed after irradiation). The increase of hole concentration at the channel edges leads to inversion regions connected with source and drain (Fig. 14). As a result, the effective channel length decreases. At present, we can not conclude which of the scenarios, (ii) or (iii) dominate in channel length decrease. Both significantly change the field in the areas where CHE are generated and thus decrease the programming efficiency.

The reported high dose effect is significant for the functionality (mostly programmability) of the memory transistors only.

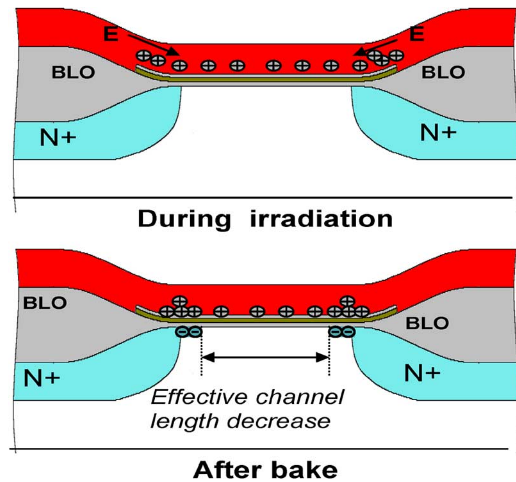

Fig. 14. Lateral hole shift in the irradiated NROM. The holes trapped in ONO over the Bit Line oxide (BLO) migrate in the direction of the NROM transistor channel.

In CMOS transistors these changes are not critical and masked by charge trapping at the STI edges.

In order to achieve NROM radiation hardness exceeding 100 krad, the CMOS periphery must be redesigned. MOS transistors having high radiation immunity compared with standard devices with FOX or STI edges must be used, e.g., MOS transistors having a fieldless (e.g., donut) geometry.

The issues of high LET required for IC qualification in some of the radiation hard environments were not addressed in the reported studies. High LETs are achieved in NROM memories by the appropriate designs and layouts (CMOS periphery) using the approaches developed for other integrated circuits.

V. Conclusion

1) Tolerant radiation immunity ($\mathrm{TID} > 100\ \mathrm{krad}$) was demonstrated for Tower Semiconductor NROM products (*micro*Flash) specifically not engineered for operation in radiation hard environments and fabricated in a conventional CMOS Fab. The only optimization consisted in the selection of the WL space filling oxide using the available in the Fab dielectric recipes. We show that by minimum changes in the process flow the NROM product is converted into NVM with promising radiation tolerance, significantly exceeding the parameters of analogous commercial products [11].
2) The results obtained for the irradiated with different sources single cells are consistent with the 4 Mbit product data.
3) Comprehensive statistics obtained due to the use of large memory arrays allowed deep understanding of the physical phenomena in the irradiated NROM devices. This data is currently employed for the development of a new generation of NROM memories having improved radiation tolerance.

4) A methodology of radiation testing, special test boards, and programs were developed that allowed the on-the-board radiation tests for memory products operated in the real bias conditions.

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REFERENCES

[1] T. R. Oldham and F. B. McLean, "Total ionizing dose effects in MOS oxides and devices," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 483–499, Jun. 2003.

[2] J. R. Stour, C. J. Marshall, and P. W. Marshall, "Review of displacement damage effects in silicon devices," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 653–670, Jun. 2003.

[3] T. R. Oldham, *Ionizing Radiation Effects in MOS Oxides*. Singapore: World Scientific, 1999.

[4] A. Gasperin, G. Ghidini, A. Cester, and A. Paccagnella, "Oxide-nitride-oxide capacitor reliability under heavy-ion irradiation," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 1898–1905, Dec. 2007.

[5] P. J. McWhorter, S. L. Miller, and T. A. Dellin, "Radiation response of SNOS nonvolatile transistors," *IEEE Trans. Nucl. Sci.*, vol. NS-33, no. 6, pp. 1414–1419, Dec. 1986.

[6] M. H. White, D. A. Adams, and J. Bu, "On the go with SONOS," *IEEE Circuits Devices Mag.*, vol. 16, pp. 22–31, Jul. 2000.

[7] B. Eitan, P. Pavan, I. Bloom, E. Aloni, A. Frommer, and D. Finzi, "NROM: A novel localized trapping 2-bit nonvolatile memory cell," *IEEE Electron Device Lett.*, vol. 21, pp. 543–545, Nov. 2000.

[8] Y. Roizin, R. Daniel, S. Greenberg, M. Gutman, M. Lisiansky, V. Kairys, E. Pikhay, and P. Zisman, "Interface traps and reliability performance of microFlash memory," in *Proc. IEEE Non-Volatile Semiconductor Memory Workshop*, 2004, pp. 85–87.

[9] D. Corso, A. Palermo, F. Palumbo, S. Libertino, S. Lombardo, M. Lisiansky, and Y. Roizin, "Radiation effects in programmed NROM cell," in *Proc. 23rd Symp. Microelectronics Technology and Devices*, Aug. 2008, vol. 14.

[10] B. Draper, R. Dockerty, M. Shaneyfelt, S. Habermehl, and J. Murray, "Total dose radiation response of NROM-style SOI non-volatile memory elements," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 3202–3205, Dec. 2008.

[11] J. Tausch, S. Tyson, and T. Fairbanks, "Multigenerational radiation response trends in SONOS-based NROM flash memories with neutron latch-up mitigation," in *Proc. IEEE Radiation Effects Data Workshop*, Jul. 2007, pp. 189–193.

[12] H. I. Hudges and J. M. Benedetto, "Radiation effects and hardening of MOS technology: Devices and circuits," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 500–521, Jun. 2003.

[13] M. R. Shaneyfelt, P. E. Dodd, B. L. Draper, and R. S. Flores, "Challenges in hardening technologies using shallow-trench isolation," *IEEE Trans. Nucl. Sci.*, vol. 45, no. 6, pp. 2584–2491, Dec. 1998.

[14] T. P. Ma and P. V. Dressendorfer, *Ionizing Radiation Effects in MOS Devices and Circuits*. New York: Wiley, 1989, pp. 222–227.

[15] R. Daniel, Y. Shacham-Diamand, and Y. Roizin, "Interface states in cycled hot electron injection program/hot hole erase silicon-oxide-nitride-oxide-silicon memories," *Appl. Phys. Lett.*, vol. 85, pp. 6266–6270, Dec. 2004.

[16] Y. Takahashi, K. Ohnishi, T. Fujimaki, and M. Yoshikawa, "Radiation-induced trapped charge in metal-nitride-oxide semiconductor structure," *IEEE Trans. Nucl. Sci.*, vol. 46, no. 6, pp. 1578–1585, Dec. 1999.

[17] J. I. Pankove, "Temperature dependence of boron neutralization in silicon by atomic hydrogen," *J. Appl. Phys.*, vol. 68, pp. 6532–6534, Dec. 1990.

[18] D. G. Nelson, J. F. Gibbons, and W. S. Johnson, "Radiation-enhanced diffusion of boron in silicon," *Appl. Phys. Lett.*, vol. 15, pp. 246–248, Jan. 1969.

[19] S. Z. Karazhanov, "Effect of radiation-induced defects on silicon solar cells," *J. Appl. Phys.*, vol. 88, pp. 3941–3947, Oct. 2000.

[20] D. Adams, P. Farfell, M. Jacunski, D. Williams, J. Jakubczak, M. Knoll, and J. Murray, "SONOS technology for commercial and military nonvolatile memory application," in *Proc. 5th Biennial Nonvolatile Memory Technology Rev.*, Jul. 1993, pp. 96–99.