Analysis of integrated STATCOM-SMES based on three-phase three-level multi-pulse voltage source inverter for high power utility applications ☆

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Abstract

This paper is aimed to investigate the operating characteristics of a static synchronous compensator (STATCOM) integrated with superconducting magnetic energy storage (SMES) for high power applications in the transmission network level. The STATCOM controller topology comprises multi-level multi-pulse neutral-point clamped-type (NPC) voltage source inverters (VSIs) using the harmonics cancellation technique, and incorporates a SMES coil. An innovative two-quadrant multi-level dc–dc converter is proposed to effectively interface the STATCOM with the superconducting coil using a buck-boost topology with neutral point voltage control capabilities; thus enabling to simultaneously control both active and reactive power exchange with the high voltage power system. A detailed analysis of major system variables is presented, including analytical results and digital simulations using the MATLAB/Simulink environment. Moreover, a three-level control scheme is designed, including a full decoupled current control strategy in the d–q reference frame with a novel controller to prevent the STATCOM dc bus capacitors voltage drift/imbalance and an enhanced power system frequency controller.

1. Introduction

In recent years, it has been gradually seen that energy storage systems (ESS) advanced solutions such as superconducting magnetic energy storage (SMES), have received significant interest for high power applications in the transmission network level. The rapid advances in superconductive technology have permitted such devices of reasonable size to be designed and commissioned successfully. In this way, SMES coils main features, such as rapid response (ms), high power (hundred MW), high efficiency, and four-quadrant control can be effectively used for influencing the operation of the power system (PS), and consequently its dynamic security [1].

By combining the technology of superconduction with a recent type of power electronic equipments, such as flexible alternating current transmission systems (FACTS) [2], the PS can take advantage of the flexibility benefits provided by SMES coils and the high controllability provided by power electronics aiming at controlling and optimizing the performance of the high voltage power system.

The application of FACTS controllers based on voltage source converters (VSCs) or specifically inverters (VSIs) has been settled world-wide as the next generation of fast reactive power compensators for improving both transient and dynamic stabilities [3,4]. In this sense, shunt compensation provided by STATCOM controllers has already proved its benefits on existing transmission systems. A STATCOM can only exchange reactive power with the electric grid. This feature limits its degrees of freedom and therefore its impact on the power system operation [5]. As demonstrated by various previous studies, simultaneous active and reactive power compensation has more valuable effects on counteracting PS disturbances. In this way, a STATCOM integrated with a SMES coil (also known simply as SMES system) through an appropriate interface, provides additional benefits and improvements to the PS, since it allows to simultaneously and independently control both active and reactive power exchange with the electric network [6]. These benefits include enhancement of reliability, dynamic stability, power quality, and area protection.

As detailed in [7], various STATCOM-SMES topologies have been studied in the literature for high power and high voltage utility applications. They mostly include STATCOMs with 24- and 48-pulse gate turn-off (GTO) thyristor inverter designs among the most adequate for the transmission network level. However, all the proposed configurations use a conventional two-level dc/dc converter to interface the SMES coil with the STATCOM. This largely restricts the possibility of employing multi-level converters in the STATCOM and therefore avoids taking advantage of its benefits for both the STATCOM-SMES system and the electric network.

This paper presents a novel high performance STATCOM-SMES device based on multi-level converters for high power utility applications and its control system. Major characteristics and the analysis of the operation of the integrated STATCOM-SMES controller is presented, including analytical results and digital simulations of main ac and dc system variables using SimPowerSystems of MATLAB/Simulink. To this aim, a detailed modelling approach and a three-level control scheme are firstly proposed, including a full decoupled current control strategy in the d–q reference frame with a unique controller to prevent the STATCOM dc bus capacitors voltage drift/imbalance. Then, the dynamic performance of the control algorithms is evaluated using digital simulation on a test power system in case of a three-phase-to-ground fault.

2. Modelling and analysis of the STATCOM-SMES controller

Fig. 1 summarizes the proposed detailed model of the STATCOM-SMES controller for dynamic performance studies in high power applications in the transmission network level. This model mainly consists of the STATCOM controller, the SMES coil with the corresponding filtering and protection system and the interface between the STATCOM and the SMES, represented by the dc–dc converter.

2.1. Three-level multi-pulse VSI-based STATCOM

The STATCOM essentially comprises the static power inverter, the dc bus capacitors and the step-up coupling transformers. Since the SMES coil is basically a stiff current source, the use of a current source inverter (CSI) would emerge as the natural selection. However, the wide range of variation of the coil current and voltage would cause the device to exceed its rating, which makes impractical the use of conventional CSIs. On this basis, an analyses were performed to evaluate hybrid current source inverters (HCSI) and voltage source inverters (VSI); concluding that the later ones are a more cost-effective solution for this application.

High efficiency voltage source inverters with reduced harmonics distortion can be implemented essentially through three feasible solutions: the conventional full bridge inverter employing pulse width modulation (PWM), the multi-level inverter, and the multi-pulse inverter.

In practice, conventional PWM switching techniques are regarded uneconomic for high power applications since the VSI have to withstand many commutations of the power
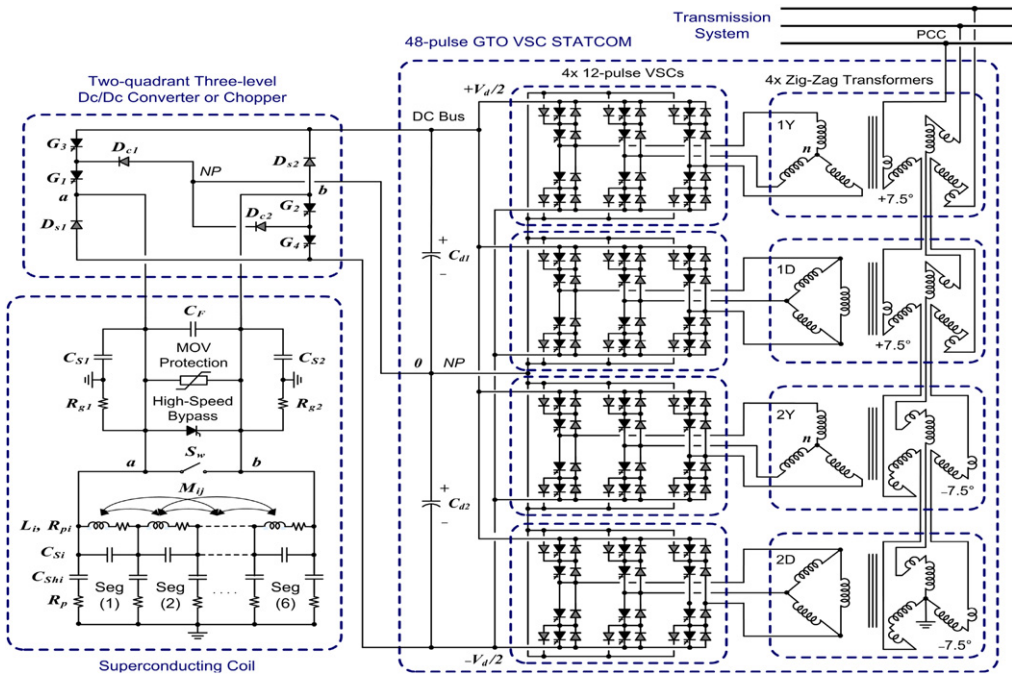

Fig. 1. Detailed model of the proposed 48-pulse VSC STATCOM-SMES controller.

semiconductors in one period of the fundamental output voltage in order to synthesize the output voltage waveforms and thus produce very high switching losses [8]. This feature and the unavailability of fast GTOs mostly limit their development in high-voltage high-power levels.

The multi-level inverter synthesizes the staircase output voltage waveform from dc capacitor voltages by splitting its dc voltage into several levels. The most relevant topologies of multi-level inverter are diode-clamped (neutral-point clamped), capacitor-clamped (flying capacitors), and cascaded multi-cell with separate dc sources [9,10]. By increasing the number of levels in the inverter, the output voltages waveforms have more steps generating a staircase approximation of a sinusoidal waveform, which has a reduced harmonics distortion. In theory, ideal output sinusoidal waveform could be obtained by an infinite number of levels. However, a high number of levels increases the control complexity and introduces voltage imbalance problems, voltage clamping requirements, circuit layout, and packaging constraints [11]. In practice, for the case of high-voltage high-power applications including active power exchange, the number of feasible voltage levels with adequate results is restricted to five.

The traditional magnetic coupled multi-pulse inverter using the harmonics cancellation technique have two or more bridges and synthesizes the staircase output voltage waveform by varying transformer turns ratio with zigzag connections. The magnetic transformer coupled inverter is bulky, heavy, and lossy. Furthermore, the VSI should have a large number of bridges and transformers in order to increase the pulses number for minimizing the harmonics distortion produced [10]. Nevertheless, practical high-voltage high-power applications in the transmission level demonstrate the adequacy of this topology, especially for simultaneous active and reactive power exchange with the electric power system.

On the basis of these facts, this work proposes the use of the multi-pulse inverter for building a STATCOM that interfaces a high-power high-energy SMES coil with the transmission utility grid. In order to avoid the use of ac capacitor banks for harmonics filtering and to meet the voltage total harmonics distortion requirements for transmission level applications, a 48-pulse inverter composed of eight magnetic coupled conventional 6-pulse GTO full bridges would appear as the most appropriate topology [12]. However, since the eight transformers required for the 48-pulse VSI are quite lossy, the proposal in this paper is to combine magnetically three-level 12-pulse full bridges instead of two-level ones. In this way, the number of transformers required is reduced to a half with a pseudo-48-pulse VSI topology and having the advantages of multi-level inverters [13]. This topology can be applied to reactive power generation almost without voltage imbalance problems. But when active power exchange is included, the inverter could not have balanced voltages without sacrificing output voltage performance and auxiliary converters would be needed in order to provide a compensating power flow between the capacitors of the dc link [14]. For this reason, the use of a two-quadrant three-level dc–dc converter as interface between the STATCOM and the SMES is proposed here, instead of a standard two-level one. This converter makes use of the extra level to solve the above-mentioned possible voltage imbalance problems. As a result, the proposed three-level pseudo-48-pulse inverter reduces the excessively large number of bulky transformers and decreases the harmonics produced as much in the ac as in the dc side of the STATCOM while permits simultaneous active and reactive power exchange between the SMES coil and the electric grid.

The proposed three-level VSI structure makes use of the neutral-point clamped (NPC) topology and employs a line-frequency switching modulation method with selective

harmonics elimination in order to build the pseudo-48-pulse inverter [7]. This multi-level inverter topology attempts to address some of the limitations of the standard two-level inverter such as the difficulty to extend the power capability of the inverter beyond the ratings of an individual switching device and the need of PWM or pulse-dropping techniques to improve the poor harmonic performance of the inverter. The three-level structure offers one degree of freedom through the additional flexibility of the zero level in the output voltage. This level can be controlled in duration, either to vary the fundamental output voltage, or to assist in the output waveform construction as is the case proposed in this work.

2.1.1. Switching functions for the elementary 6-pulse VSI

By considering that the basic three-level 6-pulse voltage source inverter is modulated with a line-frequency square-wave switching, each phase can be connected to the positive dc terminal, the midpoint (NP) or the negative dc terminal, as shown in Fig. 2a for phase 'a'. From this, the switching function expression can be derived as follows:

$$h_a^6 = \sum_{h=1}^{\infty} \left[\frac{4}{h\pi} \cos(h\beta) \sin[(h\omega t + h\beta)] \right] \tag{1}$$

being, $h = 2m - 1$ any positive integer, that is, $h = 1, 3, 5\dots$ for all $m = 1, 2, 3\dots$; β the dead angle (period) during which the VSI output voltage is zero.
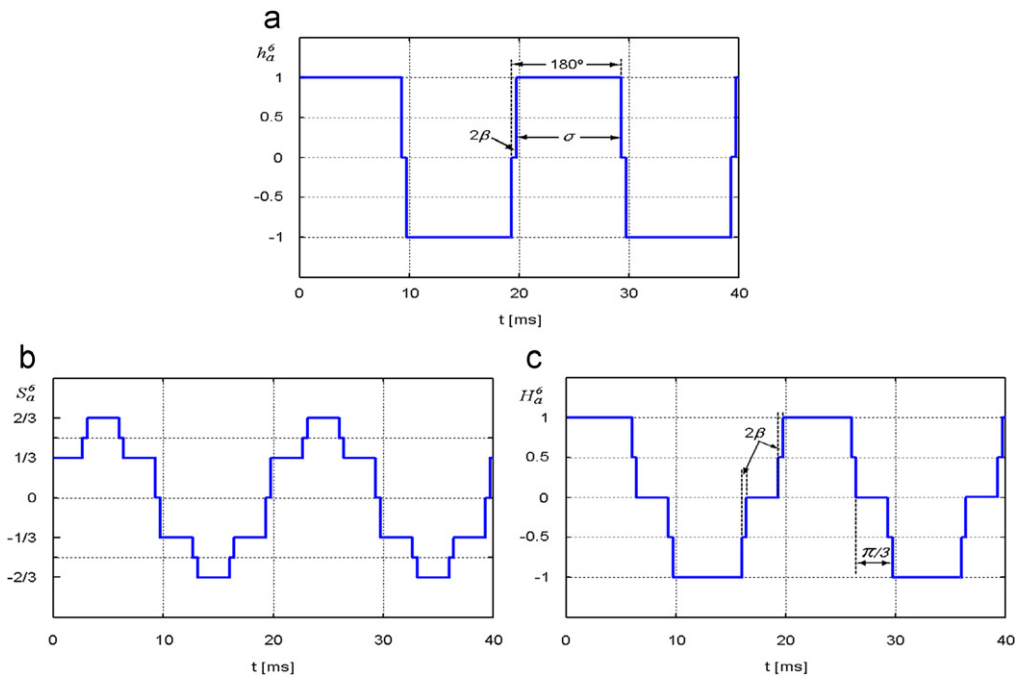

Fig. 2. Switching functions for an elementary three-level 6-pulse voltage source inverter (phase a): (a) phase-to-dc-neutral (NP) switching function, (b) phase-to-ac-neutral (n) switching function, and (c) phase-to-phase switching function.

The switching functions for phases 'b' and 'c' are similar but phase-shifted $120°$ and $240°$, respectively. Assuming that the dc capacitors voltages are balanced and equal to $V_d/2$, the VSI instantaneous terminal voltages with respect to the neutral point (NP) of the dc bus can be obtained as

$$
\begin{bmatrix} v_{inv,a0} \\ v_{inv,b0} \\ v_{inv,c0} \end{bmatrix} = \begin{bmatrix} h_a^6 \\ h_b^6 \\ h_c^6 \end{bmatrix} \frac{V_d}{2}
\tag{2}
$$

In the same way, the instantaneous 6-pulse inverter output voltages with respect to the neutral (n) of the transformer '1Y' can be expressed as

$$
\begin{bmatrix} v_{inv,an} \\ v_{inv,bn} \\ v_{inv,cn} \end{bmatrix} = \begin{bmatrix} S_a^6 \\ S_b^6 \\ S_c^6 \end{bmatrix} V_d
\tag{3}
$$

where

$$
S_a^6 = \frac{1}{2}\left(h_a^6 - \left(\frac{h_a^6 + h_b^6 + h_c^6}{3} \right) \right)
\tag{4}
$$

Substitution of Eq. (1) into Eq. (4) yields the expression of the switching function for phase 'a' with respect to the neutral of the transformers (see Fig. 2b), as follows:

$$
S_a^6 = \sum_{h=1}^{\infty} \left[\frac{2}{h\pi} \cos(h\beta)\sin(h\omega t + h\beta) \right]
\tag{5}
$$

being, $h = 6m \pm 1$ any positive integer, that is, $h = 1, 5, 7\ldots$ for all $m = 0, 1, 2\ldots$

In the same manner, the phase-to-phase instantaneous VSI output voltages can be written as

$$
\begin{bmatrix} v_{inv,ab} \\ v_{inv,bc} \\ v_{inv,ca} \end{bmatrix} = \begin{bmatrix} H_a^6 \\ H_b^6 \\ H_c^6 \end{bmatrix} V_d
\tag{6}
$$

where

$$
H_a^6 = \frac{1}{2}(h_a^6 - h_b^6)
\tag{7}
$$

Eq. (7) can be re-written using Eq. (1) as follows (see Fig. 2c):

$$
H_a^6 = \sum_{h=1}^{\infty} \left[\frac{4}{h\pi} \sin\left(\frac{h\pi}{3} \right) \cos(h\beta)\cos\left(h\omega t + h\beta - \frac{h\pi}{3} \right) \right]
\tag{8}
$$

being, $h = 6m \pm 1$ any positive integer, that is, $h = 1, 5, 7\ldots$ for all $m = 0, 1, 2\ldots$

It is significant to observe the relationship between the fundamental and harmonic components of the phase-to-phase and phase-to-neutral VSI output voltages, derived from Eqs. (5) and (8). The amplitude of the phase-to-phase voltages is $\sqrt{3}$ times the phase-to-neutral values, whereas the phase-shift is $30°$. Harmonic components different from $h = 6m \pm 1$ are present although with phase opposition and therefore neutralized in the elementary three-level inverter.

2.1.2. Switching functions for the proposed equivalent 48-pulse VSI

By applying Fourier analysis to the inverter phase output voltages expressed by Eq. (3), as can be directly derived from Eq. (5), the peak value of the fundamental and harmonics components can be found as follows:

$$v_{inv}^6 = \frac{2}{h\pi}\cos(h\beta)V_d \qquad (9)$$

with $h=6m\pm1$ ($h=1, 5, 7, 11, 13\ldots$) and $m=0, 1, 2\ldots$.

The harmonics content of the output voltage waveform, measured through the total harmonic distortion (THD) of the basic 6-pulse VSI, is higher than 14%. In order to reduce the voltage THD and thus to fulfill with standards for power electronics equipments applied to high voltage power systems (IEEE, CIGRÉ, and UIE), an equivalent 48-pulse VSI topology is used as shown in Fig. 1. Thus, using zigzag phase-shifting transformers and the appropriate valves switching phase, the principle of harmonic neutralization can be applied.

The combination of two three-level 6-pulse basic inverters (couples 1Y-1D and 2Y-2D) through the appropriate magnetic coupling creates a three-level 12-pulse converter. The 30° phase-shift between the primary and secondary of transformers 1 D and 2 D permits to cancel harmonics $5+12r$ (i.e., $h=5, 17, 29, 41\ldots$) and $7+12r$ (7, 19, 31, 43…), where $r=0,1,2,\ldots$ In the same way, by combining two three-level 12-pulse VSIs, phase-shifted 7.5° from each other, a three-level 24-pulse inverter is build. This structure is able to behave like an equivalent standard two-level 48-pulse inverter for an optimum setting of β. The 15° phase shift between the two groups of transformers (1Y-1D leading by 7.5° and 2Y-2D lagging by 7.5°) allows cancellation of harmonics $11+24r$ (11, 35,…) and $13+24r$ (13, 37,…). As all $3r$ harmonics are not transmitted by the Y and D transformers' secondaries, the first harmonics which are not cancelled by the transformers are 23rd, 25th, 47th, and 49th.

A particular harmonic h reaches zero when Eq. (10) is satisfied:

$$2\beta = \frac{180^\circ}{h} \qquad (10)$$

Thus, by choosing an appropriate conduction angle σ for the three-level inverters ($\sigma=180^\circ-2\beta$), that is, $\sigma_{optimum}=172.5^\circ$ ($\beta_{optimum}=3.75^\circ$), the 23rd and 25th harmonics can be minimized, as can be observed from harmonic content shown in Fig. 3a. As a result, the first significant harmonics are the 47th and 49th, so that the inverter acts as a 48-pulse conventional VSI. This topology permits to generate an almost sinusoidal voltage waveform consisting of 48-steps, as shown in Fig. 3b for a capacitive operation mode (generating
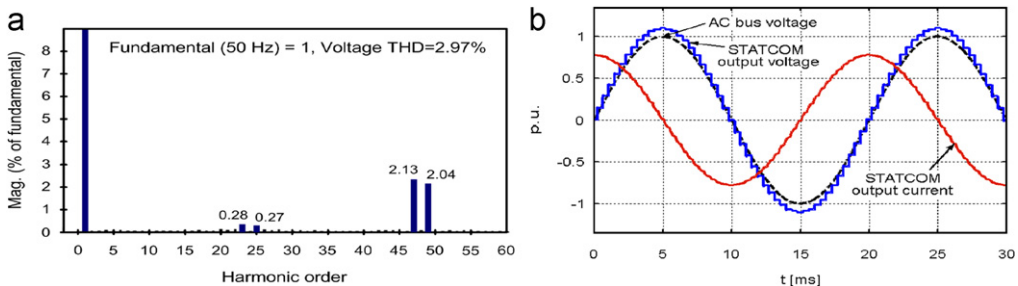

Fig. 3. Equivalent 48-pulse VSI-based STATCOM voltage THD and output waveforms for optimum conduction angle operation: (a) voltage harmonic content and (b) voltage and current output waveforms.

reactive power). The low harmonic rate of the proposed 48-pulse VSI device is expressed through the reduced voltage THD, which is less than 3%. Consequently, this equipment can be used in high power applications without ac filters. Even more, this controller supplies at the point of common coupling (PCC) to the electric grid an almost sinusoidal current; the current being smoothed by the leakage inductance of the step-up coupling transformers which act as a natural first-order low-pass filter.

The switching function for the equivalent 48-pulse voltage source inverter can be estimated for phase 'a' by Eq. (11):

$$S_a^{e48} \approx \sum_{h=1}^{\infty} \left[\frac{2}{h\pi} k_T \cos(h\beta)\sin(h\omega t) \right] \tag{11}$$

with $h = 48m \pm 1$ ($h = 1, 47, 49\ldots$) and $m = 0, 1, 2\ldots$; $k_T = 4(n_2/n_1)$ the total voltage ratio of the zigzag phase-shifting transformers.

If the switching functions are averaged, approximating by their fundamental components (neglecting harmonics), the peak value of the phase-to-neutral output voltage for the equivalent 48-pulse VSI can be expressed through Eq. (12):

$$V_{inv} = S_{av}^{e48} V_d \tag{12}$$

being, $S_{av}^{e48} = (2/\pi)k_T \cos\beta$ is the average switching function for the equivalent 48-pulse VSI.

The current exchange between the VSI and the ac system is straight determined by the voltage across the tie reactance provided by the leakage inductance of the coupling transformers. In this way, by varying the amplitude of the output voltages produced by the STATCOM respect to the ac system voltage (PCC), the current flow can be controlled and thus the reactive power exchange. The magnitude of the STATCOM fundamental current component can be derived in the following fashion:

$$I_m = \frac{1}{\omega L} \left(V_m - \left(\frac{2}{\pi} k_T \cos\beta V_d \right) \right) \tag{13}$$

where V_m is the maximum level of the ac system voltage at PCC and L the equivalent leakage inductance of the four coupling step-up transformers.

It is to be noted that if the amplitude of the inverter fundamental output voltage is increased above that of the ac system (V_p), that is $V_p < 0.6663 k_T \cos\beta V_d$, then the inverter generates reactive (capacitive) power. In a similar way, if the amplitude of the inverter fundamental output voltage is decreased below that of the ac system, that is $V_p > 0.6663 k_T \cos\beta V_d$, then the VSI generates reactive (inductive) power. The active power generation (or absorption) in turns, is accomplished by phase-shifting (leading or lagging) the output VSI voltage, v_{inv} by an angle α in relation to the ac system voltage.

The total dc bus current expression can be derived from the contribution of each ac line current through the switching functions. Thus, by considering a pure sinusoidal current waveform, as expressed by Eq. (14) for phase 'a':

$$i_a = I_m \sin(\omega t + \varphi) \tag{14}$$

being i_b and i_c phase-shifted successively by 120°. φ the phase-shift between the output line current and the voltage generated by the STATCOM VSI.

The angle φ is near equal to $\pm \pi/2$ depending upon whether the STATCOM exchanges capacitive or inductive reactive power, respectively.
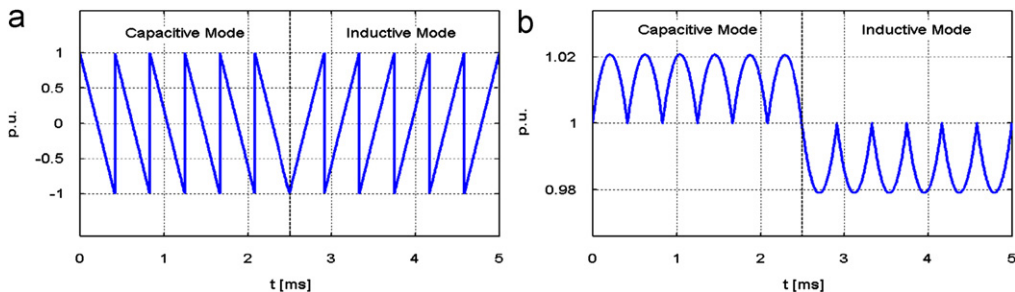
Fig. 4. Instantaneous dc bus current and voltage for the equivalent 48-pulse inverter in capacitive and inductive mode: (a) dc bus current and (b) dc bus voltage.

The total dc bus current can be described by Eq. (15):

$$I_{dc} = \begin{bmatrix} S_a^{e48} & S_b^{e48} & S_c^{e48} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{15}$$

This current waveform is shown in Fig. 4a for the inverter generating (capacitive mode) and absorbing (inductive mode) reactive power and neglecting losses. The switching functions can be expressed in Fourier series form, so that Eq. (15) can be re-written as

$$I_{dc} = I_d + \sum_{h=1}^{\infty} \left[\frac{3I_m}{48h} \sin(48h\omega t) \right] \tag{16}$$

In case that active power is also exchanged, φ will differ from $\pm\pi/2$ in Eq. (14), being reduced its absolute value. This feature also becomes evident in Eq. (16) by the appearance of a constant dc current offset which produces a dc power. This dc current component I_d, accounts for the total actual switching VSI losses and capacitors power losses, as well as the current provided by the SMES coil linked to the dc bus. On the other hand, the infinite summation of Eq. (16) describes the reactive power exchanged with the utility system. It can be noted the presence of harmonic components of order $48h$ on the capacitors current, so that the first significant harmonic is the 48th. This feature meets the harmonics transfer condition from ac-side to dc-side and vice versa. A harmonic on the dc-side is transferred to the ac-side as two side-bands of order $(48h\pm1)$ with positive and negative sequence components, respectively. In the same way, a given sequence harmonic on the ac-side transferred to the dc-side gives only one of the side-bands, being the lower order for a positive sequence and the higher order for a negative sequence.

The previous study supposes a constant dc voltage provided by an infinite capacitor. If a finite capacitor is considered, a dc ripple appears which depends on the capacitor value and the current flow. Considering this case, as can be seen from Fig. 4b, the dc bus voltage can be expressed in a similar way than for the dc bus current as follows:

$$V_{dc} = \frac{2}{C_d} \int_0^t I_{dc}\, d\tau + V_{d0} \tag{17}$$

being V_{d0} an initial condition at $t=0$.

Substituting Eq. (16) into Eq. (17) permits to obtain the dc bus voltage expression as

$$V_{dc} = V_d - \sum_{h=1}^{\infty} \left[\frac{6I_m}{48h} Z_d(h) \cos(48h\omega t) \right] \tag{18}$$

where $Z_d(h) = (1/48h\omega C_d)$ is the dc side impedance at harmonic components $48h$, neglecting losses.

The dc voltage component, V_d involves initial voltage condition (according to capacitors initial state of charge) and active power exchanged with the utility system including the action of the SMES coil. In contrast, the infinite summation describes the reactive power exchanged with the ac system.

2.2. Two-quadrant three-level dc–dc converter

The inclusion of a SMES coil into the dc bus of the STATCOM demands the use of an interface to adapt the wide range of variation in voltage and current levels between both devices. Controlling the SMES coil rate of charge/discharge requires varying as much the coil voltage magnitude as the polarity according to the coil state-of-charge, while keeping essentially constant the STATCOM dc bus voltage. To this aim, a two-quadrant three-level dc–dc converter or chopper is proposed to be employed. This converter (top left-hand side of Fig. 1) allows decreasing the ratings of the overall power devices by regulating the current flowing from the SMES coil to the inverter of the STATCOM and vice versa. In addition, it allows varying the amplitude of the output voltage of the VSI, keeping constant the conduction angle σ of the inverter valves. Thus, the harmonic distortion of the STATCOM output voltage can be maintained at the lowest level, independently of the voltage required at the PCC ($\sigma_{optimum}$ seen in Section 2.1.2).

Major advantages of three-level chopper topologies compared to traditional two-level ones include reduction of voltage stress of each thyristor by half, permitting to increase the chopper power ratings maintaining high dynamic performance and decreasing the harmonics distortion produced. Furthermore, the availability of redundant switching states, which allow generating the same output voltage vector through various states. This last feature is very significant in order to reduce switching losses and dc current ripple, but mainly to maintain the charge balance of the dc capacitors. This condition of NP voltage balancing is crucial for avoiding contributing additional distortion to the three-level equivalent 48-pulse VSI output voltage.

Table 1
Three-level chopper output voltage vectors and their corresponding GTO switching states.

States	G_1	G_2	G_3	G_4	V_{ab}
1	1	1	1	1	$+V_d$
2	0	0	0	0	$-V_d$
3	0	1	0	1	0
4	1	0	1	0	0
5	1	1	0	0	0
6	1	1	0	1	$+V_d/2$
7	1	1	1	0	$+V_d/2$
8	1	0	0	0	$-V_d/2$
9	0	1	0	0	$-V_d/2$

Table 1 shows all possible combinations of the chopper output voltage vectors, V_{ab} (defining the SMES side of the circuit as the output side) and their corresponding GTO switching states. The addition of an extra level to the dc–dc chopper allows enlarging its degrees of freedom. As a result, the charge balance of the dc bus capacitors can be controlled using the extra switching states, at the same time acting as a conventional dc–dc converter. The output voltage vectors can be selected based on the required SMES coil voltage and dc bus NP voltage. In this way, multiple subtopologies can be used in order to obtain output voltage vectors of magnitude 0 and $V_d/2$, in such a way that different vectors of magnitude $V_d/2$ produce opposite currents flowing from/to the neutral point. This condition causes a fluctuation in the NP potential which permits to maintain the charge balance of the dc-link capacitors. By properly selecting the duration of the different output voltage vectors, an efficient dc–dc controller with NP voltage control capabilities is obtained.

The dc–dc chopper has basically three modes of operation, namely the buck or charge mode, the boost or discharge mode and the stand-by mode. These modes are obtained in this work using a buck-boost topology control mode in opposition to a bang–bang control mode [15] that is much simpler yet produces higher ac losses in the SMES coil.

2.2.1. Switching functions for the chopper operating in buck mode (charge)

In the charge mode, the chopper works as a step-down (buck) converter. This topology makes use of switching states 1, 5, 6 and 7, in order to produce output voltage vectors $+V_d$, 0, and $+V_d/2$ with separate contribution of charge at the NP from capacitors C_{d1} and C_{d2}. In this mode, thyristors G_1 and G_2 are always kept on, while thyristors G_3 and G_4 are modulated to obtain the appropriate output voltage, V_{ab}, across the SMES coil. In this way, only subtopologies closest to the state 1 are used. In consequence, only one semiconductor device is switched per switching cycle T_s; this reducing the switching losses compared to the standard two-level converter and thus also reducing the current ripple.

Fig. 5a shows the switching function of the three-level chopper operating in buck mode. This function, which is stated in Eq. (19), shows an attribute of immutability associated to the switching states utilized for maintaining the charge balance of the dc capacitors (states 6 or 7):

$$S_{ch} = D_1 + D_2 + \sum_{h=1}^{\infty} \left[2\frac{\sin(h\pi D_2)}{h\pi} \cos\left[h\omega(t-\gamma_2-2\gamma_1)\right] \right] + \sum_{h=1}^{\infty} \left[\frac{\sin(2h\pi D_1)}{h\pi} \cos\left[h\omega(t-\gamma_1)\right] \right]$$
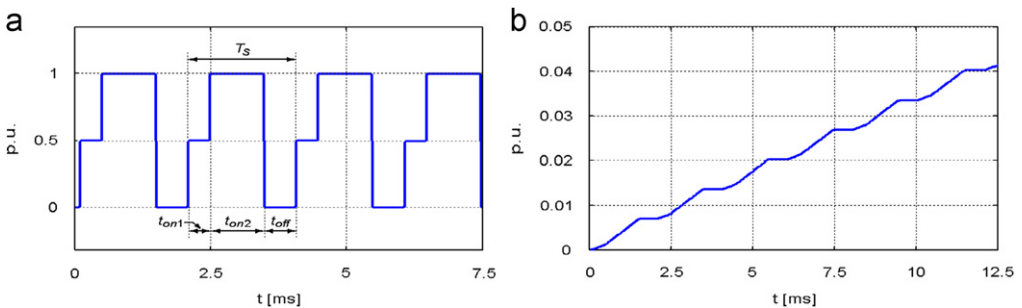
(19)

Fig. 5. Chopper switching function and output current for buck mode (charge): (a) chopper switching function and (b) SMES current.

where $h = 1, 2, 3 \ldots$; $D_1 = (t_{on1}/2T_s)$ the duty cycle for switching states 6 or 7; $D_2 = (t_{on2}/T_s)$ the duty cycle for switching state 1; $\gamma_1 = (D_1/f)$ the harmonic phase angle due to D_1; $\gamma_2 = (D_2/2f)$ the harmonic phase angle due to D_2.

It can be inferred from Eq. (19) the presence of voltage ripples generated by the three-level dc–dc chopper output. Even though this chopper has an improved harmonic quality of the output voltage relative to the two-level converter, especially at low frequencies, it is necessary to provide the SMES coil with a capacitive filter to prevent an excessive stress of the superconducting coil insulation caused by resonances at certain frequencies.

The relationship between the chopper output voltage V_{ab}, and the VSI dc bus voltage V_d can be derived from Eq. (19), as follows:

$$V_{ab} = S_{ch} V_d \tag{20}$$

In the same fashion, the chopper output current I_{sc}, i.e., the current flowing to the SMES coil, can be estimated as described by Eq. (21):

$$I_{sc} = \frac{1}{L} \int_0^t V_{ab} \, d\tau \tag{21}$$

Fig. 5b allows observing the existence of ripple also in the SMES coil current, although being lower than the case of the output voltage.

Once completed the charging of the SMES coil, the operating mode of the converter is changed to the stand-by mode, for which only the state 5 is used. In this condition, thyristors G_3 and G_4 are switched off, while thyristors G_1 and G_2 are kept on all the time. During periods when the SMES coil is charged but it is expected not to use such stored energy for a relatively long time, the coil should be shorted by a mechanical switch (S_w) in order to avoid power dissipation on semiconductors.

2.2.2. Switching functions for the chopper operating in boost mode (discharge)

In the discharge mode, the chopper operates as a step-up (boost) converter in collaboration with the dc bus capacitors. This topology employs switching states 2, 5, 8, and 9, in order to produce at terminals ab, vectors $-V_d$, 0, and $-V_d/2$ with independent contribution of charge at the NP from capacitors C_{d1} and C_{d2}. In this mode, thyristors G_3 and G_4 are constantly kept off while thyristors G_1 and G_2 are controlled to obtain the suitable voltage V_{ab}, across the SMES coil. In this way, only subtopologies closest to state 2 are utilized.

Fig. 6a shows the switching function of the three-level chopper operating in discharge or boost mode. From this, the switching function expression can be derived as stated in Eq. (22).
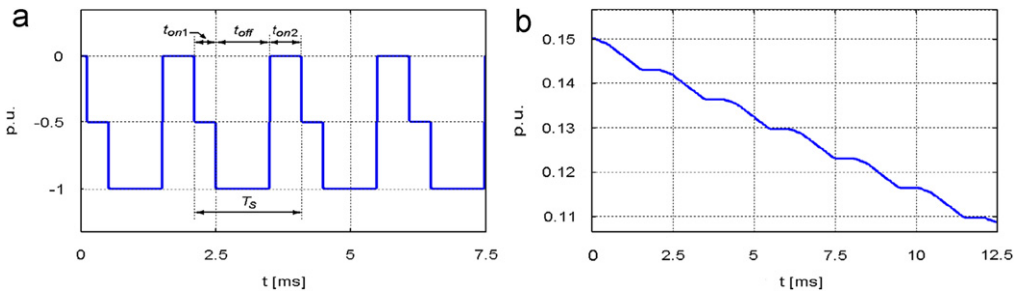

Fig. 6. Chopper switching function and output current for boost mode (discharge): (a) chopper switching function and (b) SMES current.

This function exhibits an analogous feature of immutability respect to the switching states utilized for generating vectors $-V_d/2$ (states 8 or 9), as in the case of the buck mode:

$$S_{dch} = 1 - D_1 - D_2 + \sum_{h=1}^{\infty} \left[2 \frac{\sin(h\pi(1-D_2))}{h\pi} \cos[h\omega(t - \zeta_2 - 2\zeta_1)] \right] + \sum_{h=1}^{\infty} \left[\frac{\sin(2h\pi(1-D_1))}{h\pi} \cos[h\omega(t - \zeta_1)] \right]$$

(22)

where $h = 1, 2, 3 \ldots$; $\zeta_1 = ((1-D_1)/f)$ is the harmonic phase angle due to D_1; $\zeta_2 = ((1-D_2)/2f)$ the harmonic phase angle due to D_2.

As in the case of the chopper working in buck mode, the relationship between the chopper voltage V_{ab}, and the VSI dc bus voltage V_d can be derived from Eq. (22), as stated in Eq. (23):

$$V_{ab} = S_{dch} V_d$$

(23)

In the same manner, the SMES coil current I_{sc} can be estimated as described by Eq. (21) for charge mode, but substituting V_{ab} from Eq. (23) into Eq. (21).

As can be inferred from previous equations, there exists also voltage and current ripples generated by the three-level dc–dc chopper output in the boost mode. Fig. 6b shows the SMES coil current in the discharge or boost mode.

By averaging the switching functions S_{ch} and S_{dch}, which results analogous to neglecting harmonics, a general expression relating the chopper average output voltage V_{ab}, to the VSI average dc bus voltage V_d, can be derived through Eq. (24):

$$V_{ab} = m V_d$$

(24)

being m, the modulation index expressed as $m = (D_1 + D_2)$ the chopper buck mode (charge); $m = -(1 - D_1 - D_2)$ the chopper boost mode (discharge).

2.3. Multi-segment SMES coil

The equivalent circuit of the SMES coil depicted at the bottom left-hand side of Fig. 1 makes use of a lumped parameters network represented by a six-segment model comprising self-inductances (L_i), mutual couplings between segments (i and j, M_{ij}), ac loss resistances (R_{si}), skin effect-related resistances (R_{pi}), turn-ground (shunt—C_{Shi}), and turn–turn capacitances (series—C_{Si}). This model is based on the ones previously proposed in [16,17], and is reasonably accurate for electric systems transients studies, over a frequency range from dc to several thousand Hertz.
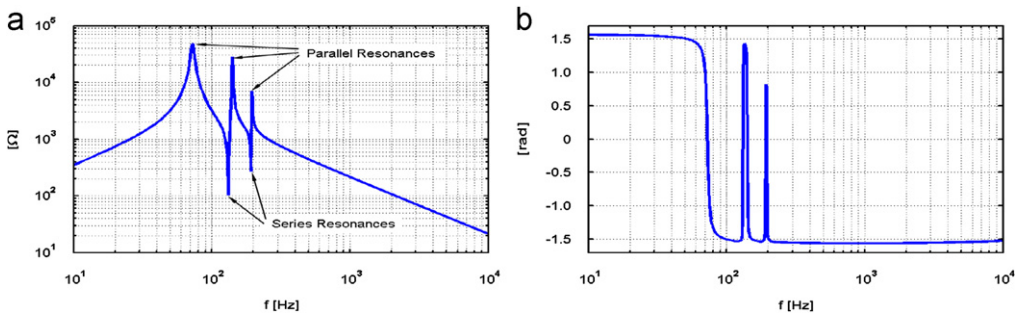

Fig. 7. SMES coil terminal impedance Z_{ab} versus frequency: (a) magnitude of SMES coil impedance and (b) phase angle of SMES coil impedance.

Fig. 7 shows the frequency domain analysis of the six-segment SMES model (for the coil detailed in Appendix B), measuring the impedance of the superconducting coil across its terminals (Z_{ab}). As can be seen from the magnitude of the terminal impedance, the coil has parallel resonance frequencies at around 70, 120, and 200 Hz and series resonance frequencies at about 110 and 190 Hz. As expressed in Section 2.2, the Fourier series of the chopper output voltage V_{ab}, contains both even and odd harmonics of the switching frequency, which may excite coil resonances and cause significant voltage amplification of transients with the consequent addition of insulation stress within the coil. Since the SMES coil has a rather high inductance, these resonance frequencies become lower, turning this phenomena an issue for selecting the chopper operating frequency. In addition, high power dc–dc converters utilize low operating frequencies in order to minimize losses, being significant in consequence to take into consideration the coil resonance phenomena for choosing a safety frequency band of operation for the chopper.

Fortunately, the negative effects of the harmonic decrease faster than the inverse of the harmonic order due to the skin effect occurring in the superconductor. Furthermore, the inclusion of surge capacitors (C_{s1} and C_{s2}) in parallel with grounding-balance resistors (R_{g1} and R_{g2}) allows reducing the effect of resonances. However, in order to decrease even more this phenomenon, a filter capacitor C_F is proposed to be connected at the SMES coil terminals. Thus, a reduction of harmonics content of V_{ab} is obtained, also strongly decreasing the magnitude of the terminal SMES coil impedance at secondary series and parallel resonances, maintaining constant their frequencies and becoming lower the frequency of the first parallel resonance, as shown in Fig. 8. In this way, for the case presented here, the chopper operating frequency can be set as low as 500 Hz without producing severe voltage amplification inside the SMES coil.

3. Multi-level control scheme of the STATCOM-SMES

The proposed three-level control scheme of the integrated STATCOM-SMES controller is based on the steady-state average model of the device. This hierarchical control system, consisting of an external, middle and internal level, is based on concepts of instantaneous power on the synchronous-rotating d–q reference frame [18], as shown in Fig. 9.
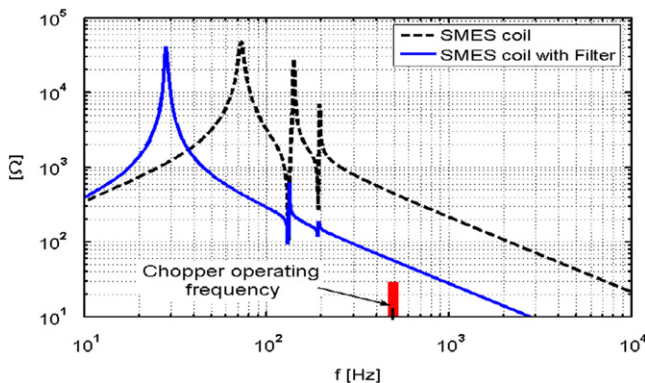

Fig. 8. SMES coil terminal impedance versus frequency with and without input filter.
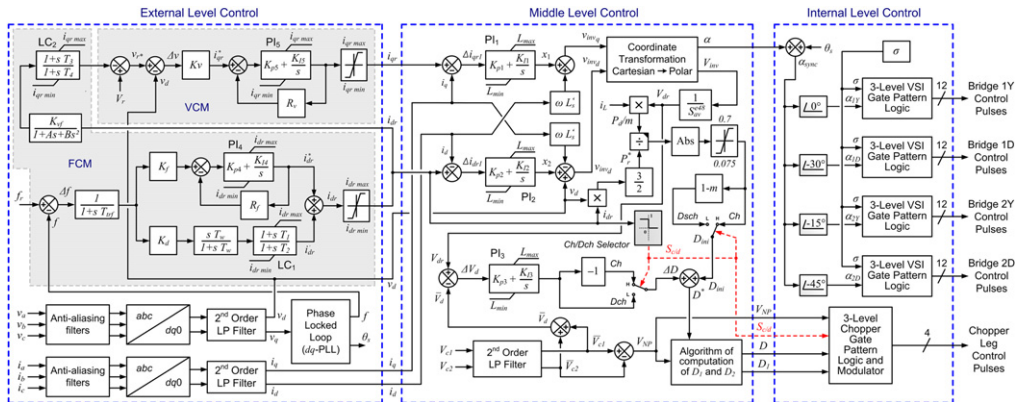
Fig. 9. Proposed three-level control scheme of the STATCOM-SMES device.

3.1. External level control design

The external level control, which is outlined in Fig. 9 (left-hand side), is responsible for determining the active and reactive power exchange between the STATCOM-SMES device and the utility system in order to reduce the change of determined operating conditions of the power system in case of large disturbances. This control strategy is designed for performing two major objectives (control modes) with dissimilar priorities:

- Frequency control mode (FCM). Case of a STATCOM-SMES controller with active and reactive power exchange capabilities.
- Voltage control mode (VCM). Case of a traditional STATCOM with only reactive power compensation capabilities.

3.1.1. Frequency control mode

This highest-priority control mode accomplished by the middle blocks of the external level aims at controlling the PS frequency through the modulation of both, the reactive component of the output current i_q (case of a conventional STATCOM) and the active component i_d (case of a STATCOM-SMES). In the case of controlling i_q, the set-point of the VCM, i.e., the voltage reference signal V_r, is varied with a stabilizing voltage signal proportional to the PS frequency deviation Δf (defined as the difference between the set reference frequency f_r and the actual frequency f) which directly represents the power oscillation of the PS. This added signal causes the output quadrature current of the STATCOM, i_q to vary around the operating point defined by V_r, the purpose of this variation being to improve the damping of the power oscillations. In this way, the voltage at the PCC is forced to decrease when the frequency deviation Δf is positive aiming at reducing the transmitted power through the transmission system and thus providing an effective fast-acting voltage reduction reserve which opposes the deceleration of generators in the PS. This action is performed in the opposite way when the frequency deviation Δf is negative, and then generators accelerate. Two transfer functions, including a lag-compensator (LC$_2$), are used to assist in shaping the gain and phase characteristics of the frequency stabilizer for the case of modulating the output quadrature current of the STATCOM.

Although the power oscillation damping technique of the standard STATCOM is rather effective, the most effective compensation action for power oscillations (or swings) damping and thus for primary frequency control (PFC) is carried out by rapidly exchanging active power with the utility system, that is to say by controlling the output direct current of the STATCOM-SMES, i_d. Considering this case, as in the previous case, the reference of the STATCOM-SMES output direct current is directly derived from Δf, representing the power oscillation of the system. The frequency transducer transfer function is designed to eliminate any dc component that may be present on the signal Δf, by proper setting of the constant T_{trf} of the low-pass filter. Since a robust and efficient frequency control scheme requires the effective damping of a wide range of generators power oscillations, ranging from less than 0.2 Hz for global oscillations to 4 Hz for local oscillations of units, a decoupled two-loop control approach with differential bands of damping is proposed in this work. Thus, a loop is dedicated to low and intermediate frequency modes of oscillations while the other one covers the high frequency mode.

The first loop is composed of a proportional-integral (PI) controller (PI$_4$) with output restriction including an anti-windup system to enhance the dynamic performance of the PFC system. A speed-droop R_f (typically 3%) is also included in order to obtain a stable load division among several fast-response devices operating in parallel. This characteristic is analogous to the one included in generators speed governors. Thus, the rapid active power exchange between the STATCOM-SMES and the PS is controlled, forcing the SMES coil to absorb active power when generators accelerate (charge mode), or to inject active power when they decelerate (discharge mode). The PI controller including a droop feedback acts as an overall first-order lag-compensator. This first loop ensures an excellent performance in damping power oscillations at low and intermediate frequency modes and then for large-signal stability, but its response is very poor for the high frequency mode. To this end, a supplementary signal proportional to the rate of change of the system frequency has been included via the second loop in order to speed-up the transient response of the controller for managing high frequency modes of oscillations. A differential signal of the frequency error with restricted high frequency gain is obtained using a first-order washout filter. A lag-compensator (LC$_1$) is also included into the loop in order to improve the dynamic response of the controller and to ensure the robust global damping provided by the proposed PFC mode. This second loop provides an excellent performance in damping power oscillations at high frequency modes and then for small-signal stability. Therefore, both loops act independently, so that their effects add up to provide effective damping of all modes of interest. In this way steady state and transient objectives are fulfilled by this control strategy almost uniformly. The stabilizer signal composed from both loops is passed through a final limiter for setting the reference i_{dr}.

In all cases, the frequency signal is derived from the positive sequence components of the ac voltage vector measured at the PCC of the STATCOM-SMES, through a phase locked loop (PLL). The design of the PLL is developed in the *dq* reference frame and incorporates an adaptive control using a neural network for increasing its capture range [19]. This device also synchronizes, by providing the phase θ, the coordinate transformations from *abc* to *dq* components in the voltage and current measurement system. These signals are then filtered using second-order low-pass filters in order to obtain the fundamental components employed in the control system.

3.1.2. Voltage control mode

This subordinate control mode has the goal of controlling (supporting and regulating) the voltage at the PCC to the electric grid. It has proved very good performance in

conventional STATCOM controllers through the modulation of the reactive component of the output current i_{qr}. To this end, in this work the instantaneous voltage at the PCC is computed using a synchronous-rotating reference frame. In consequence, by applying Park's transformation, the instantaneous values of the three-phase ac bus voltages are transformed into d–q components, v_d and v_q, respectively. By defining the d-axis always coincident with the instantaneous voltage vector v, then v_d results equal to $|v|$ while v_q is set at zero. Consequently, only v_d is used for computing the voltage error vector which is introduced to a proportional-integral (PI) controller with output restriction including an anti-windup system to enhance the dynamic performance of the VCM system. A voltage regulation droop R_d (typically 5%) is included in order to allow a higher operation stability of the STATCOM-SMES device in cases that more high-speed voltage compensators are operating in the area. This characteristic is comparable to the one included in generators voltage regulators [20]. As a result, the PI controller including a droop feedback acts as an overall first-order lag-compensator.

3.2. Middle level control design

The middle level control makes the expected output, particularly the actual active and reactive power exchange between the STATCOM-SMES and the ac system, to dynamically track the reference values set by the external level. The middle level control design, which is depicted in Fig. 9 (middle side), is based on a linearization of the state-space averaged mathematical model of the STATCOM VSC in the d–q reference frame described in depth in [7], as follows:

$$s\begin{bmatrix} i_d \\ i_q \\ \hline V_d \end{bmatrix} = \begin{bmatrix} \dfrac{-R_s}{L'_s} & \omega & \dfrac{S_d^{e48}}{L'_s} \\ -\omega & \dfrac{-R_s}{L'_s} & \dfrac{S_q^{e48}}{L'_s} \\ \hline -\dfrac{3}{C_d}S_d^{e48} & -\dfrac{3}{C_d}S_q^{e48} & -\dfrac{2}{R_p C_d} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ \hline V_d \end{bmatrix} - \begin{bmatrix} \dfrac{|v|}{L'_s} \\ 0 \\ \hline 0 \end{bmatrix}, \tag{25}$$

where R_s is the equivalent resistance accounting for transformers winding resistance and VSI semiconductors conduction losses, L_s' the equivalent leakage inductance in the d–q reference frame for the four VSI step-up transformers, C_d the equivalent capacitance of the dc bus capacitors, and ω the synchronous angular speed of the network voltage at the fundamental system frequency f.

As reported by Acha et al. [21], modeling of static inverters using a synchronous-rotating orthogonal d–q reference frame offers higher accuracy than employing stationary coordinates. Moreover, this operation allows designing a simpler control system than using a–c or α–β stationary components.

The average switching functions for the equivalent 48-pulse voltage source inverter, transformed into the d–q reference frame, can be defined as

$$S_d^{e48} = S_{av}^{e48}\cos\alpha \tag{26}$$

$$S_q^{e48} = S_{av}^{e48}\sin\alpha \tag{27}$$

with α is the phase-shift of the VSI output voltage from the reference position, set by the instantaneous voltage vector measured at the PCC.

The new coordinate system is defined where the d-axis is always coincident with the instantaneous voltage vector at the PCC ($v_d = |v|$, $v_q = 0$). Consequently, the d-axis current component contributes to the instantaneous active power p- and the q-axis current component represents the instantaneous reactive power q, as stated in Eqs. (28) and (29). In this way, in order to achieve a decoupled active and reactive power control, it is required to provide a full decoupled control strategy for i_d and i_q:

$$p = \tfrac{3}{2}(v_d i_d + v_q i_q) = \tfrac{3}{2}|v|i_d \tag{28}$$

$$q = \tfrac{3}{2}(v_d i_q - v_q i_d) = \tfrac{3}{2}|v|i_q \tag{29}$$

Inspection of Eq. (25) shows a cross-coupling of both components of the STATCOM-SMES controller output current through ω. Therefore, in order to decouple the control of i_d and i_q, appropriate control signals have to be generated. To this aim, it is proposed the use of two control signals x_1 and x_2, which are derived from assumption of zero derivatives of currents (si_d and si_q) in the upper part (ac side) of Eq. (25). In this way, the cross-coupling effect in steady state can be eliminated. This upper part of Eq. (25) can be re-written using the relation stated in Eq. (12), transformed into the synchronous rotating d–q reference frame through Eqs. (26) and (27), as follows:

$$s\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} = \begin{bmatrix} \dfrac{-R_s}{L'_s} & \omega \\ -\omega & \dfrac{-R_s}{L'_s} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{1}{L'_s} \begin{bmatrix} v_{inv_d} - |v| \\ v_{inv_q} \end{bmatrix} \tag{30}$$

From Eq. (30), the peak value of the phase-to-neutral output voltage of the pseudo-48-pulse VSI, transformed into the d-q reference frame, can be directly derived as stated in Eqs. (31) and (32):

$$v_{inv_d} = L'_s \left(\frac{R_s}{L'_s} i_d - \omega i_q \right) + |v| \tag{31}$$

$$v_{inv_q} = L'_s \left(\frac{R_s}{L'_s} i_q + \omega i_d \right) \tag{32}$$

Assigning the proposed control signals x_1 and x_2 in order to replace the output current components i_q and i_d, respectively, in such a way that only the cross-coupling of both components are left in Eqs. (31) and (32), it is obtained:

$$v_{inv_d} = L'_s(x_2 - \omega i_q) + |v| \tag{33}$$
$$v_{inv_q} = L'_s(x_1 + \omega i_d) \tag{34}$$

Eventually, substituting Eqs. (33) and (34) into the upper part (ac side) of Eq. (25), yields the expression of Eq. (35) as follows:

$$s\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \dfrac{-R_s}{L'_s} & 0 \\ 0 & \dfrac{-R_s}{L'_s} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} - \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \tag{35}$$

As can be noticed, i_d and i_q respond to x_1 and x_2, respectively, with no crosscoupling. Thus, with the introduction of these new variables this control approach allows to obtain a quite effective decoupled control with the model (ac side) reduced to first-order functions. In order to guarantee the decoupled control condition of i_d and i_q in steady state, two conventional PI controllers with proper feedback of the STATCOM-SMES output current components are introduced in order to generate the proposed control signals x_1 and x_2, as shown in Fig. 9 (middle side).

Even though the STATCOM-SMES and the power system are inherently nonlinear, practical phase-shift ratings α of the VSI output voltage from the reference position are small enough (typically within $\pm 3°$) to consider the linearization of average switching functions as valid. Consequently, linear methods of control yield satisfactory results for a wide range of disturbances in the PS.

Fig. 9 (middle side) shows the full implementation of the middle level control. The coordinate transformation from Cartesian to Polar yields the required magnitude of the output voltage vector produced by the VSI (V_{inv}) and the phase-shift rating α of this vector from the reference position, represented by the voltage vector measured at the PCC of the STATCOM-SMES. From V_{inv}, the required voltage at the dc bus (V_{dr}) is derived and the duty cycle of the chopper thyristors (D^*) is estimated through a balance of dc power in the chopper, taking into consideration the active power injection/absorption ratings required from the STATCOM-SMES and the actual current of the SMES coil i_L. The duty cycle of the chopper GTO thyristors is then derived by relying on the mode of operation of the dc/dc chopper (charge/discharge), so that an initial value D_{ini} is determined for the thyristors duty cycle. This mode of operation is determined assessing the sign of the required positive sequence component of i_d (i_{dr1}) via a charge/discharge selection block and producing a signal of mode $S_{c/d}$ that is also required by the internal level control. A corrective action of integral-type (PI controller) is needed for an accurate tracking of the actual duty cycle D^*, being D^* the total duty ratio of the three-level chopper. Therefore, dc bus voltage deviations ΔV_d caused by actual VSC switching losses and capacitors power losses can be quickly counteracted. Finally, duty cycles D_1 and D_2 are computed from D^* through a novel controller for balancing the dc link capacitors. This novel extra dc voltage control block provides the availability of managing the redundant switching states of the chopper according to the capacitors charge unbalance measured through the neutral point voltage, $V_{PN} = \overline{V}_{c1} - \overline{V}_{c2}$. This specific loop modifying the modulating waveforms of the internal level control is also proposed for reducing instability problems caused by harmonics as much in the STATCOM-SMES device as in the electric system [22].

3.3. Internal level control design

The internal level provides dynamic control of input signals for the dc–dc and ac–dc converters. This level is responsible for generating the triggering and blocking control signals for the different valves of the pseudo-48-pulse three-level VSI and the three-level dc–dc chopper, according to the control mode and types of valves used. Fig. 9 (right-hand side) shows a basic scheme of the internal level control of the STATCOM-SMES compensator. This level is mainly composed of a line synchronization module and a firing pulses generator for both the STATCOM VSI and the dc–dc chopper. The line synchronization module simply synchronizes the STATCOM-SMES device switching pulses with the

positive sequence components of the ac voltage vector at the PCC through the PLL phase signal, θ_s.

4. Computational implementation of the STATCOM-SMES model in MATLAB/Simulink

The full detailed model of the proposed STATCOM-SMES device is implemented in the MATLAB/Simulink software package [23] and uses the SimPowerSystems (SPS) as shown in Fig. 10. Since this detailed model contains many states and non-linear blocks such as power electronics switches, the discretization of the electrical system with fixed-step is required so as to allow much faster simulation than using continuous variable time-step methods. Two sample times are employed in order to enhance the simulation, Ts_Power = 5 μs for the simulation of the power system, the multi-pulse VSI and the dc–dc converter, and Ts_Control = 100 μs for the simulation of the multi-level control blocks.

The Simulink/SPS libraries offer a variety of models, such as machines, power electronic devices and control blocks, which make it feasible to straightforwardly develop the proposed technical models. Thus, the equivalent 48-pulse GTOs voltage source inverter is basically made out of three-level bridge blocks linked through zigzag phase-shifting transformer blocks and series branches of RC linear elements, all being ready-built blocks and elements of SPS. The three-level GTOs dc–dc converter is wisely developed using an original proposal. The conventional three-level bridge block with just one branch activated is employed in such a way that simply the required semiconductors are switched while the others are kept off at all times. In this way, the dc–dc converter implementation is optimizely achieved for discrete simulations, since the turn-on and turn-off times (fall time and tail time) of the power switching device are not modelled. This results in a faster simulation when compared to a single GTO mask because
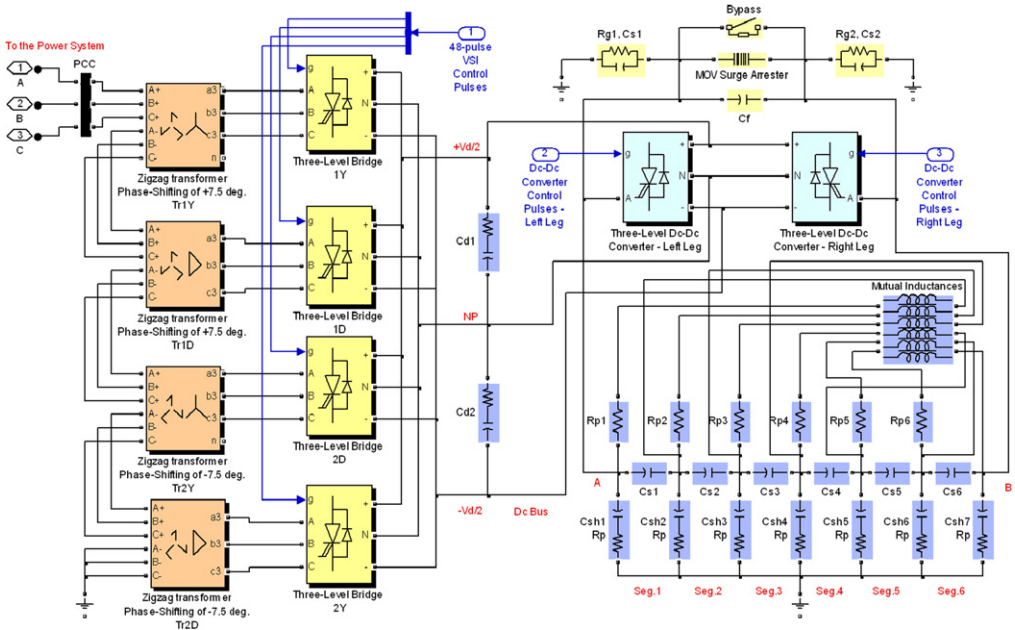

Fig. 10. MATLAB/Simulink implementation of the proposed STATCOM-SMES detailed model.

of the later increased state-space model. Thus, the conventional solution with individual semiconductors would not be feasible when the power system is also included into the simulation. The six-segment SMES coil is developed using series branches of RC linear elements and the generalized model of mutual inductances block existing is SPS, specifying the inductance matrices that define the mutual coupling relationship between the six windings (balanced for this application). Protection elements, such as the metal-oxide varistors (MOVs) are developed via the metal-oxide surge arrester modelled through a highly nonlinear *V–I* characteristic. In the same way, the bypass switch is made out of a circuit breaker controlled from an external Simulink signal.

5. Digital simulation results

5.1. Test system

The test power system used to study the dynamic performance of the STATCOM-SMES is shown in Fig. 11 as a single-line diagram. This 7-bus transmission system operates at 230 kV/50 Hz, and implements a dynamically-modelled single generator-type small utility linked to a bulk power system represented by a machine-infinite bus-type used for studies of FACTS devices. The generator is powered by a steam turbine represented through non-linear models and the controls of the unit include a dc type-1a standard IEEE voltage regulator and a speed governor. All loads are modelled by constant impedances and are grouped at buses 6, 4, and 7. The major test system data are summarized in Appendix A.

The performance of the proposed STATCOM-SMES controller is analyzed through digital simulation carried out using SPS of MATLAB/Simulink during 40 s. To this aim, a three-phase-to-ground fault is applied at bus 2 in the bulk power system at $t=0.1$ s, and cleared 5 cycles later (100 ms) by tripping the tie line with the opening of the circuit breaker placed between buses 3 and 4. A load shedding scheme (LS) is included in order to prevent the system frequency collapse during the disturbance, but also to make use of the activated load shedding steps as a performance comparison index for various scenarios including the STATCOM-SMES. This integrated controller is placed at bus 4 aiming at enhancing the dynamic security, in cases that severe disturbances occur.
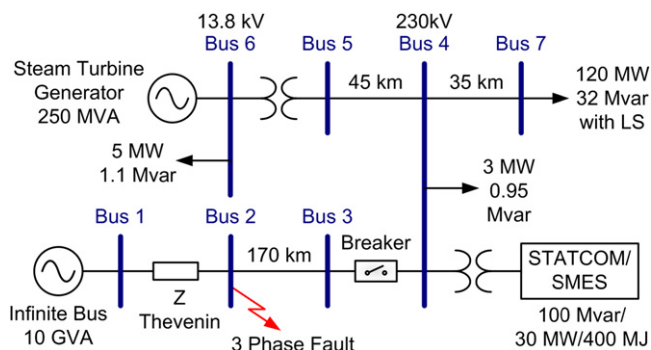

Fig. 11. Test system.

5.2. Base case study

For the topology presented in the test case without the inclusion of the STATCOM-SMES, also called as base case, in the steady state previous to the fault the utility system must import about 20 MW from the bulk power system. In this interconnected operation the system frequency is at its rated value of 1 p.u. After the fault, the tie line is tripped and the generator operates in island conditions. Under these conditions, only the generator is able to provide all the power demanded by loads. As can be seen from the simulation results of Fig. 12, presented the base case using dash-dotted lines, the spinning reserve of the unit is neither sufficiently large nor fast enough for supporting the system frequency through the primary frequency control (PFC) and thus avoiding the frequency drop which causes the system collapse. In this case, the implementation of the automatic LS scheme with the activation of four (of ten) frequency steps is required in order to recover the system frequency to its scheduled value. Despite this fact, the generating unit have to ramp up quickly to decrease the amount of load rejected. Load rejection also permits to improve the voltage profile at bus 4 in each LS activation step. A transient overvoltage occurs until unit's voltage regulators stabilize the bus voltage.

Consider the inclusion at bus 4 of a 100 Mvar STATCOM controller combined with a 30 MW/400 MJ SMES coil. In this condition, two external control modes are studied, namely the voltage control mode, or VCM (case of a traditional STATCOM without energy storage) and the frequency control mode, or FCM (case of an integrated STATCOM-SMES controller).

5.3. STATCOM in voltage control mode

The impact of the inclusion of a traditional STATCOM controller at bus 4 operating in VCM can be analyzed by simulation results of Fig. 12, portrayed this case through dashed lines. The good performance of the voltage regulator of the STATCOM device is evidently depicted by the compensation of reactive power, which is shown in Fig. 13 in dash-dotted line. PI controller gains of the external level control scheme in VCM were determined to give the power system the fastest possible Bus 4 voltage regulation (the shortest settling time, and therefore rise time) while keeping the maximum overshoot less than 15%. However, this control objective (VCM) of the standard STATCOM device comes into conflict with the primary frequency control of the PS. Thus, by controlling the voltage at bus 4, an augment of the active power demanded of the generator is obtained which causes an increase of the system frequency drop and its rate of change. In this way, an extra LS frequency step needs to be activated respect to the base case
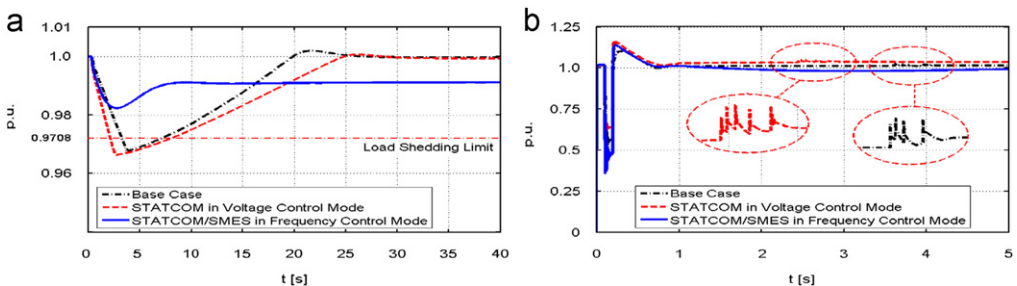

Fig. 12. Fault results for the proposed case studies: (a) power system frequency and (b) bus 4 voltage.
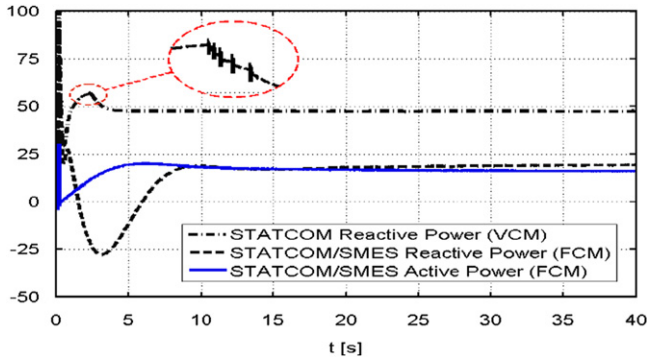
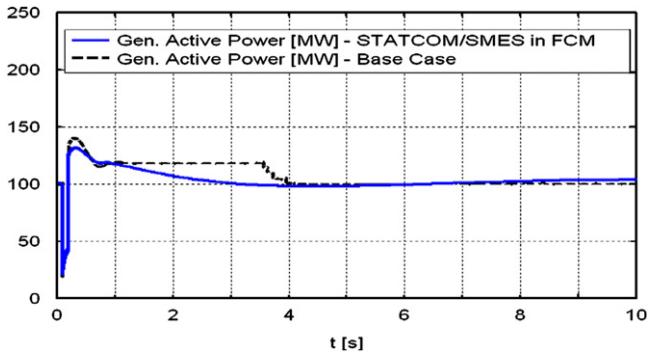Fig. 13. STATCOM-SMES active and reactive power for VCM and FCM.

Fig. 14. Generator active power for the base case and STATCOM-SMES in FCM.

(five of ten steps) by the PFC in order to recover the system frequency during the disturbance effect. In the post-fault steady-state, the voltage level at bus 4 is enhanced by the STATCOM providing a compensation of 47.5 Mvar (Fig. 13).

5.4. STATCOM-SMES in frequency control mode

The effect of incorporating a 30 MW/400 MJ SMES coil into the dc bus of the conventional 100 Mvar STATCOM device, yielding an enhanced integrated STATCOM-SMES controller, can be studied through the simulation results of Fig. 12, depicted this case through solid lines. These results clearly show the outstanding dynamic performance of the frequency control mode of the STATCOM-SMES system. After the fault, when the frequency deviation exceeds the controller dead-band limits, the SMES device is activated. The rapid active power supply added to the conventional reactive power compensation, which are shown in Fig. 13 in solid and dashed lines, respectively, absorbs the sudden power lost occurred after the tie-line tripping. Thus, the generator is able to find the balance with the load at a lower speed than in the previous test cases without producing a significant frequency deviation, as can be derived from the generator active power flow of Fig. 14, for the base case (dashed lines) compared to the case with the STATCOM-SMES in FCM (solid lines). This condition permits to greatly decrease the power strain of the generating unit and also the spinning reserve required from this machine.

In this case, the effects of the disturbance are totally mitigated in a shorter time than in the base case without being necessary to activate the load shedding scheme. In fact, the frequency drop is drastically reduced and maintained far away from the load shedding limit. Furthermore, the maximum reactive power required from the STATCOM-SMES is reduced respect to the conventional STATCOM device and the voltage profile at bus 4 is preserved without rejecting load. The improvement of the PFC is obtained by the action of the SMES coil, which provides active power for about 20 s (approximately 315 MJ of energy). Automatic generation control (AGC) action has not been shown in order to focusing the study on the primary frequency control performance.

6. Conclusions

In this paper, the operating characteristics of a static synchronous compensator (STATCOM) integrated with superconducting magnetic energy storage (SMES) for high power applications in the transmission network level have been investigated. A detailed full dynamic model of the integrated STATCOM-SMES device has been proposed, including a three-level pseudo-48-pulse voltage source inverter and a two-quadrant three-level dc–dc converter as interface between both devices. Based on the state-space averaging method a three-level control scheme has been designed, comprising an enhanced frequency control scheme, a full decoupled current control strategy in the synchronous-rotating *d-q* reference frame with an effective control approach to balancing the STATCOM dc bus capacitors voltage. The proposed STATCOM-SMES controller has been implemented and fully validated by digital simulation carried out using SimPowerSystems of MATLAB/ Simulink. The descriptive digital models proposed have been deeply examined, including analytical results and digital simulations of main ac and dc system variables.

Appendix A

A.1. Test system data

Transmission lines are modelled as distributed parameters with lumped losses. Major lines data are given in Table A1, using p.u. quantities on 220 kV and 100 MVA base. Table A2 shows the most important transformer data. In this case, all p.u. quantities are on 220 kV and the generating unit nominal MVA base. Major generating unit data and the active and reactive power quantities used in the base-case load flow are shown in Table A3. In addition, main parameters related to synchronous machines, voltage regulator and prime mover systems are shown in Tables A4 and A5. Finally, in Table A6 the most important load data are shown.

An underfrequency load shedding scheme is utilized. The scheme is composed of ten frequency steps, each one rejecting 5 MW and 2 Mvar. Consequently up to 50 MW of

Table A1
Line data.

ID#	From Bus	To Bus	L (km)	R (pu)	X (pu)	B (pu)
L1	2	3	170	0.0223	0.1227	0.2948
L2	5	4	45	0.0149	0.0818	0.1966
L3	4	7	35	0.0062	0.0341	0.0819

ID#=component identifier; R, X, and B=total positive sequence resistance, reactance and susceptance of transmission lines.

Table A2
Transformer data.

ID#	From Bus	To bus	R (pu)	X (pu)	G (pu × 10^{-3})	B (pu × 10^{-3})	S_N (MVA)	N_p/N_s (kV/kV)
T1	6	5	0.00413	0.1653	0.653	3.0976	250	230/18

R and X=winding resistance and reactance.
G and B=magnetizing conductance and susceptance.
N_p/N_s=voltage transformation ratio.

Table A3
Generating unit data.

ID#	Bus	Unit Type	Unit Size (MW)	P_G (MW)	Q_G (Mvar)	S_N (MVA)	V_N (kV)	V_S (pu)
G1	6	ST	170	100	15	250	18	1.03

Unit type=ST—fossil-fuelled steam turbine with tandem compound single mass generator.
P_G and Q_G=generating unit active and reactive power output.
V_S=generating unit voltage output.

Table A4
Generating unit data (cont.).

ID#	H (MW/MJ)	R_S (pu)	X_l (pu)	X_d (pu)	X_q (pu)	X'_d (pu)	X'_q (pu)	T'_{d0}(s)	T'_{q0}(s)
G1	5.5	0.001	0.14	1.569	1.548	0.324	0.918	5.140	1.5

H=inertia constant.
R_s and X_l=stator resistance and leakage inductance X_d, X'_d, X_q, and X'_q=direct and quadrature axis synchronous and transient reactances T'_{d0} and T'_{q0}=direct and quadrature axis open-circuit transient and subtransient time constants.

Table A5
Generating unit data (cont. 1).

ID#	R (%)	DB (mHz)	T_{SR} (ms)	T_{SM} (ms)	K_A	T_A (ms)	K_F	T_F (ms)	T_R (ms)
G1	5	180	1	150	300	1	0.001	100	20

R=speed regulation or governor droop.
DB=dead band of speed regulator.
T_{SR}=speed-relay time constant.
T_{SM}=servo-motor time constant.

Table A6
Load data.

ID#	Bus	P_L MW	Q_L Mvar	LS
Ld7	7	120	32	Y
Ld4	4	3	0.95	N
Ld6	6	5	1.1	N

P_L and Q_L=load active and reactive power.
LS=load shedding scheme (Y=included, N=not included).

Table A7
Load-shedding scheme.

Frequency step	f (Hz)	f (p.u.)
1	48.539	0.97078
2	48.512	0.97024
3	48.475	0.9695
4	48.422	0.96844
5	48.369	0.96738
6	48.312	0.96624
7	48.25	0.965
8	48.185	0.9637
9	48.115	0.9623
10	48.042	0.96084
	$f_{min,\ Admissible}$=47.5 Hz=0.95 p.u.	

Table B1
STATCOM-SMES data.

Q_{max} (Mvar)	P_{max} (MW)	$E_{SC\ max}$ (MJ)	$I_{SC\ max}$ (kA)	V_d (kV)	C_{d1},C_{d2} (mF)	L_T (H)
100	96	400	4	24	10	50

Q_{max}=maximum rated reactive power.
P_{max}=maximum rated active power.
$E_{SC\ max}$=maximum rated storage capacity of the SMES system.
$I_{SC\ max}$=maximum rated current of the superconducting coil.
V_d=rated voltage of the dc bus.
$C_{d1,}\ C_{d2}$=capacitances of the dc bus capacitors.
L_T=total inductance of the SMES device.

active power can be rejected, representing 41.66% of the active power load. The operating time delay of each load-shedding step, which utilizes solid-state relays, is 0.2 s (Table A7).

Appendix B

B.1. STATCOM-SMES controller data

Tables B1–B3 summarize the most important data corresponding to the STATCOM, chopper and SMES sub-systems.

Table B2
SMES model data.

#Seg.	L_i (H)	M_{ij} (H)	C_{Si} (μF)	C_{Shi} (μF)	R_{pi} (Ω)	R_p (Ω)
6	8.334	3.12	0.01	0.488	0.05	5

#Seg.=number of segments of the coil model.
L_i=self-inductance per segment.
M_{ij}=mutual coupling inductance between segments.
C_{Sj}=series stray capacitance between turns of the coil.
C_{Shj}=shunt stray capacitance between turn and ground.
R_{pi}=ac loss resistance per segment.
R_p=stray resistance between segments due to skin effect.

Table B3
Chopper and SMES filter data.

T_F (μs)	T_T (μs)	V_{FG}/V_{FD} (V)	R_{ON} (mΩ)	C_{S1},C_{S2} (μF)	R_{g1},R_{g2} (kΩ)	C_F (μF)
5	10	1/0.6	1	1.1	27.5	6

T_F=fall time of the GTO of the chopper (similar for the inverter).
T_T=tail time of the GTO of the chopper.
V_{FG}, V_{FD}=forward voltages for GTOs and diodes, respectively.
R_{ON}=internal resistance of the GTO device.
C_{S1}, C_{S2}, C_F=capacitances of SMES filter.
R_{g1}, R_{g2}=ground resistances.

References

[1] M.H. Ali, B. Wu, R.A. Dougal, An overview of SMES applications in power and energy systems, IEEE Transactions on Sustainable Energy 1 (1) (2010) 38–47.

[2] X.P. Zhang, C. Rehtanz, B. Pal, Flexible AC Transmission Systems: Modelling and Control (Power Systems), 2nd Ed., Springer-Verlag, New York, 2009.

[3] S. Panda, Differential evolution algorithm for SSSC-based damping controller design considering time delay, Journal of the Franklin Institute (2011). doi:10.1016/j.jfranklin.2011.05.011.

[4] S. Panda, N.P. Padhy, Optimal location and controller design of STATCOM for power system stability improvement using PSO, Journal of the Franklin Institute 345 (2) (2008) 166–181.

[5] H.M. Solimana, A. Dabroumb, M.S. Mahmoudc, M. Soliman, Guaranteed-cost reliable control with regional pole placement of a power system, Journal of the Franklin Institute 348 (5) (2011) 884–898.

[6] M.G. Molina, P.E. Mercado, E.H. Watanabe, Static synchronous compensator with superconducting magnetic energy storage for high power utility applications, Energy Conversion and Management 48 (8) (2007) 2316–2331.

[7] M.G. Molina, P.E. Mercado, E.H. Watanabe, Improved superconducting magnetic energy storage (SMES) controller for high power utility applications, IEEE Transactions on Energy Conversion 26 (2) (2011) 444–456.

[8] J. Holtz, Pulsewidth modulation—a survey, IEEE Transactions on Industrial Electronics 39 (5) (1992) 410–420.

[9] J. Rodriguez, J.S. Lai, F.Z. Peng, Multilevel inverters: a survey of topologies, controls, and applications, IEEE Transactions on Industrial Electronics 49 (4) (2002) 724–738.

[10] F.Z. Peng, J.S. Lai, J.W. McKeever, J. Van Coevering., A multilevel voltage-source inverter with separate DC sources for static VAr generation, IEEE Transactions on Industry Applications 32 (5) (1996) 1130–1138.

[11] J.S. Lai, F.Z. Peng, Multilevel converters—a new breed of power converters, IEEE Transactions on Industry Applications 32 (3) (1996) 509–517.

[12] M.G. Molina, P.E. Mercado, Controlling a static synchronous compensator with superconducting magnetic energy storage for applications on primary frequency control, Latin American Applied Research Journal 34 (2) (2004) 119–126.

[13] M.S. El-Moursi, A.M. Sharaf, Novel controllers for the 48-pulse VSC STATCOM and SSSC for voltage regulation and reactive power compensation, IEEE Transactions on Power Systems 20 (4) (2005) 1985–1997.

[14] D. Soto, T.C. Green, A comparison of high-power converter topologies for the implementation of FACTS controllers, IEEE Transactions on Industrial Electronics 49 (5) (2002) 1072–1080.

[15] M.V. Aware, D. Sutanto, SMES for protection of distributed critical loads, IEEE Transactions on Power Delivery 19 (3) (2004) 1267–1275.

[16] L. Chen, Y. Liu, A.B. Arsoy, P.F. Ribeiro, M. Steurer, M.R. Iravani, Detailed modeling of superconducting magnetic energy storage (SMES) system, IEEE Transactions on Power Delivery 21 (2) (2006) 699–710.

[17] M. Steurer, W. Hribernik, Frequency response characteristics of a 100 MJ SMES coil—measurements and model refinement, IEEE Transactions on Applied Superconductivity 15 (2005) 1887–1890.

[18] P.C. Krause, Analysis of Electric Machinery, Mc Graw-Hill, New York, 1992.

[19] M. Raoof, A.A. Suratgar, Adaptive control of PLL using neural network, Journal of the Franklin Institute 346 (1) (2009) 81–93.

[20] H. Gozde, M. Cengiz Taplamacioglu, Comparative performance analysis of artificial bee colony algorithm for automatic voltage regulator (AVR) system, Journal of the Franklin Institute (2011). doi:10.1016/j.jfranklin.2011.05.012.

[21] E. Acha, V. Agelidis, O. Anaya-Lara, T. Miller, Power Electronic Control in Electrical System, 1st ed., Newness, United Kingdom, 2002.

[22] M.G. Molina, P.E. Mercado, Power flow stabilization and control of microgrid with wind generation by superconducting magnetic energy storage, IEEE Transactions on Power Electronics 26 (3) (2011) 910–922.

[23] The MathWorks Inc. SimPowerSystems for use with Simulink 7.6: User's Guide, 2010.