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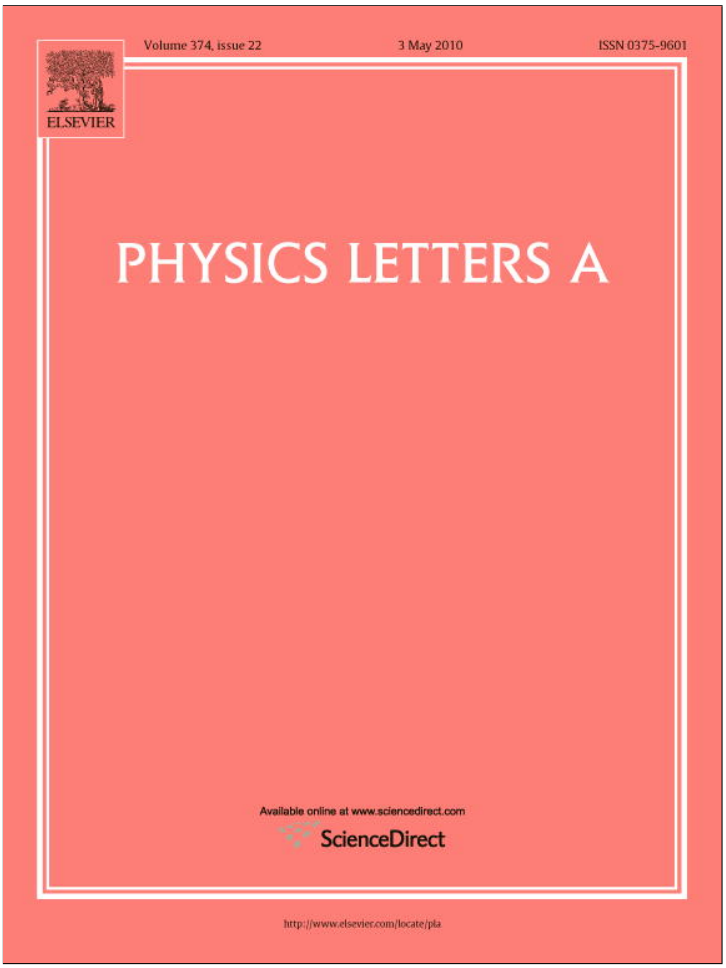

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A memory device sustained by noise

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ABSTRACT

We propose a memory device consisting of a ring of two bistable coupled oscillators. We show that this system is capable of storing a single bit and its performance improves with noise, in agreement with previous experimental results obtained with discrete bistable electronic circuits. The stored bit can be retrieved asynchronously and, after a certain synchronization time, the probability of error does not depend on the interrogated oscillator. Memory persistence is shown to be maximized for the same noise range that both minimizes the probability of error and ensures synchronization.

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1. Introduction

Moore's Law postulates that the maximum number of transistors in an integrated circuit roughly doubles every eighteen months. As such, higher transistor densities and power consumption require the use of smaller voltages leading to tighter noise margins and higher error rates [1]. Several strategies have been suggested to circumvent this problem. Refs. [2,3] explicitly take into account the fact that computation may be correct only with some probability, and [4] uses a set of orthogonal noise processes to represent logic values. Another possibility is to explore the interaction of noise with nonlinearity as in the case of Stochastic Resonance (SR). SR is a phenomenon in a nonlinear system where the noise helps, an otherwise weak signal, to induce transitions between stable equilibrium states. It was first introduced in the context of climate dynamics [5] to explain the almost periodic occurrence of ice ages, and has since been reported in a large number of areas, ranging from biological and neurological systems [6–8] to information transmission sustained by noise [9–16]. For a general review of the area of stochastic resonance we refer the reader to Refs. [17,18]. Following this line of thought, Refs. [19–21] report that basic logical operations can be implemented by using nonlinear systems in the presence of noise.

Noise-resistant memory devices will also be needed in future computing systems. Refs. [22,23] show that a travelling wave can be sustained by noise in a ring of coupled nonlinear oscillators, persisting long after the harmonic driving signal is switched off. In this work, we explore an extension of this scheme using an aperiodic signal driving the shortest possible ring of only two bistable oscillators. It is interesting to note that this system resembles that of two Josephson junctions symmetrically inserted into a superconducting loop [24,25].

A system of two coupled bistable oscillators was also studied in Refs. [26,27]. In particular, Neiman [26] studied the synchronization phenomena of an unforced system. Neiman and Schimansky-Geier [27] added an external harmonic force to both oscillators and studied such metrics as signal-to-ratio. In our case, we drive only one of the two oscillators with an aperiodic signal and study the behavior of the system from the point of view of a memory device, analyzing performance metrics such as probability of error upon information retrieval and memory persistence time.

In Section 2, we describe the system under consideration and its application as a memory device. In Section 3, memory performance is evaluated through numerical simulations. Finally, conclusions are presented in Section 4.

2. A ring of two coupled oscillators as a memory device

Each oscillator is driven by a force proportional to the position of the other oscillator [22]. The equations of motion of a ring of two oscillators are

$$dx_1 = \left[-\frac{\partial U_1}{\partial x}(x_1) + \epsilon\frac{x_2}{x_0}\right]dt + \sigma\, dB_1,$$
$$dx_2 = \left[-\frac{\partial U_1}{\partial x}(x_2) + \epsilon\frac{x_1}{x_0}\right]dt + \sigma\, dB_2, \qquad (1)$$

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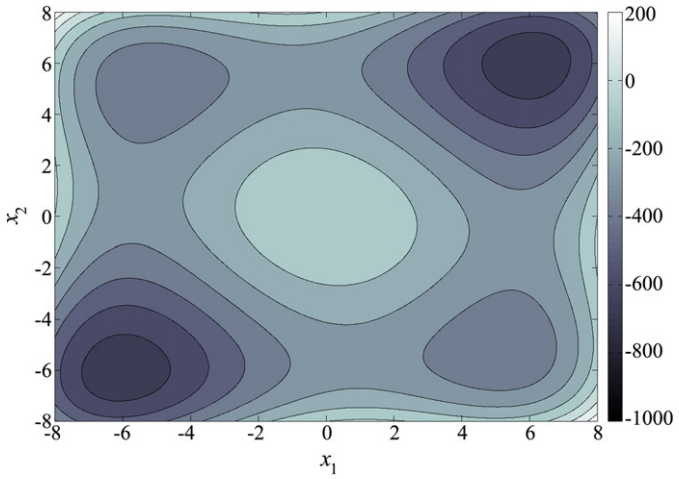

Fig. 1. The potential in Eq. (4) for $U_0 = 256$, $x_0 = \sqrt{32}$ and $\epsilon = 25$.

where B_i represents spatially uncorrelated noise ($\langle B_i \rangle = 0$, and $\langle dB_i\, dB_j \rangle = \delta_{ij}\, dt$), σ^2 is the noise intensity; ϵ is the coupling strength between adjacent oscillators, and $U_1(x)$ is the potential

$$U_1(x) = U_0 \left(\frac{x}{x_0}\right)^2 \left[\left(\frac{x}{x_0}\right)^2 - 2\right]. \tag{2}$$

Eq. (1) can also be written as

$$d\vec{x} = -\nabla U_2(\vec{x})\, dt + \sigma\, d\vec{B}, \tag{3}$$

where we have used $d\vec{B} = (dB_1, dB_2)$ and

$$U_2(x_1, x_2) = U_1(x_1) + U_1(x_2) - \epsilon \frac{x_1 x_2}{x_0}. \tag{4}$$

In the absence of noise the system exhibits different regimes depending upon the value of ϵ. We will concentrate on the case $0 < \epsilon < \frac{2U_0}{x_0}$ in which the potential in Eq. (4) presents four minima, one in each quadrant (see Fig. 1). For larger values of ϵ the origin develops into a saddle point and the system is notably similar to the one-particle bistable potential in Kramers–Smoluchowski [28].

In order to store one bit, the first oscillator is driven with a short pulse of amplitude P_0 and duration T_P. We only consider pulse intensities which are too low to force the system out of the deeper equilibrium states.

Memory retrieval from oscillator i, at any time, is performed by taking the average of x_i during an interval T_P and comparing it to a fixed threshold, arbitrarily set to 0. The system incurs in an error when the average is smaller than zero.

3. Memory device performance

We assess memory performance through the probability of error upon retrieval of the stored bit from oscillator i, p_e^i, estimated as the number of errors divided by the total number of realizations. For a proper operation of the memory device, it is required that stored information can be retrieved from any oscillator and at any time. We say that both oscillators are 'synchronized' if p_e^1 and p_e^2 differ by a small quantity, arbitrarily fixed to be 10^{-3}. Simulation results in Fig. 2 show that the synchronization time (T_s) decreases as noise intensity increases. Moreover, it is observed that there is a range of noise intensities, enclosed by dashed lines, for which both the probability of error is small and the synchronization time is close to its minimum ($\sim T_P$).

It is customary to approximate the dynamics of a bistable potential by a two-state model [17,18]. Similarly, we can understand

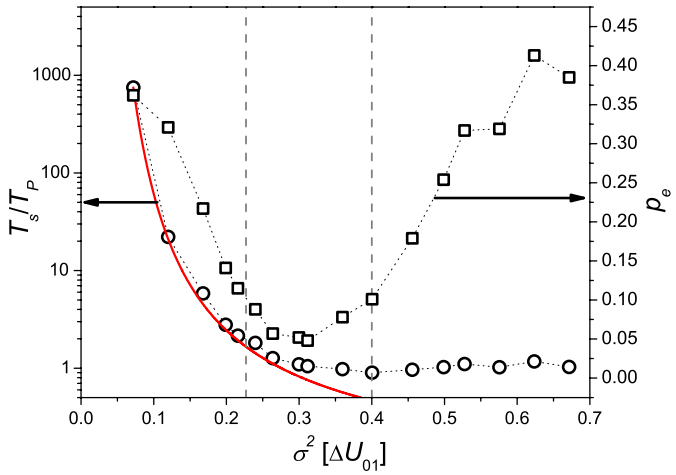

Fig. 2. Synchronization time (T_s) and probability of error at T_s as a function of noise intensity. The solid line corresponds to four-state discrete model. Noise intensity is normalized to $\Delta U_{01} = U_0(1 + \frac{\epsilon x_0}{2U_0})^2$, where $U_0 = 256$, $x_0 = \sqrt{32}$ and $\epsilon = 25$. The duration of the sub-threshold pulse was set to $T_P = 5$. Numerical results correspond to an average over 10000 realizations.

the above results by employing a four-state model of the system, each state corresponding to an equilibrium position of U_2 (Eq. (4)). We enumerate the states from 0 through 3, starting from the first quadrant and moving in counter-clockwise direction. Let $n_i(t)$ be the probability of finding the particle in the state i at time t. We can thus write a master-type equation $\dot{\vec{n}} = \mathbb{W} \cdot \vec{n}$ where $\vec{n} = (n_0, n_1, n_2, n_3)^T$ and $\mathbb{W}$ is the transition matrix. The transition rates can be estimated as [28] $W_{ij} \approx K_{ij} \exp\{\frac{-2\Delta U_{ij}}{\sigma^2}\}$, where K_{ij} is a constant and ΔU_{ij} is the potential barrier that the particle has to overcome when moving from the i-th to the j-th state. Symmetries present in the potential allow to reduce the problem to the calculation of four transition rates that depend upon the following potential barriers

$$\Delta U_{ij} = |j - i| U_0 \left(1 + (-1)^i \frac{\epsilon x_0}{2|j - i| U_0}\right)^2, \tag{5}$$

for $ij = 01,\ 10,\ 13,\ 02$. The four-state model allows to obtain an estimate of the synchronization time when $T_s > T_P$; suppose that memory retrieval is carried out by instantaneously observing the state of the oscillator without computing an average. The probability of error can then be written in terms of the above state probabilities as $p_e^1(t) = n_1(t) + n_2(t)$ and $p_e^2(t) = n_2(t) + n_3(t)$. By solving the master equation one can show that

$$p_e^1(t) - p_e^2(t) \propto \mathrm{e}^{-2(W_{10} + W_{13})t}.$$

Thus, the synchronization time is

$$T_s = \frac{\tau}{2(W_{10} + W_{13})}, \tag{6}$$

where τ is a suitably chosen constant. This theoretical estimate is plotted in a solid line in Fig. 2. W_{10} and W_{13} were computed using Eq. (5) and τ was calculated by adjusting the simulated value of T_s at the lowest noise intensity.

Fig. 2 also shows the probability of error, when both oscillators are synchronized, as a function of noise intensity. Note that there is range of noise intensities that minimizes the probability of error. The beneficial role of noise on the probability of error, a signature of stochastic resonance, has also been observed in information transmission lines [15]. In [16] we observed a similar behavior in experiments with a nonlinear circuit consisting of a ring of two Schmitt triggers. Schmitt triggers (STs) are bistable electronic devices with a hysteretic input-output relation [29] and can be

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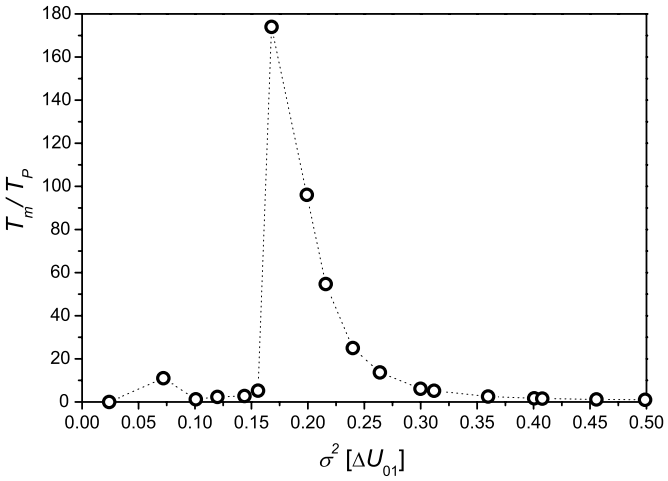

Fig. 3. Memory persistence time as a function of noise intensity.

regarded as 'discrete' models of the bistable potentials in previous sections [30]. In the experimental setup described in Ref. [16], a single pulse, representing the bit that was to be stored, was fed into one ST with a supra-threshold amplitude. Both STs were also fed with white Gaussian noise from independent sources, and their outputs were set to sub-threshold values. By interrogating the state of one of the Schmitt triggers, it was found that the probability of error was minimized in a certain range of noise intensities.

Finally, we characterize the memory persistence time (T_m) as the time elapsed until the first oscillator reaches a probability of error equal to that of the noiseless case ($p_e^1 \approx 0.25$). From this moment on noise no longer helps improve the performance of the device. This definition allows us to specify a 'refresh' time scale, as it is common in Dynamic Random Access Memory (DRAM) devices. In Fig. 3, T_m is shown as a function of noise intensity. Note that there is a range of noise intensities for which memory persistence is large. Furthermore, from Figs. 2–3, it is observed that there is an optimal noise level for which *the memory device not only maximizes the persistence time, but also both oscillators are synchronized and the probability of error is minimal.*

4. Conclusions

In summary, we studied the behavior of a system comprised of two bistable oscillators in a loop configuration. In particular, we showed that such a system is capable of storing a single bit of information in a noisy environment. The proposed device can be regarded as 'asynchronous', in the sense that stored information can be retrieved at any time. Moreover, after a certain 'synchronization' time, the probability of erroneous retrieval does not depend on the oscillator being interrogated. Device performance was also characterized by the memory persistence time, which we defined as the time elapsed until the probability of error equaled that of the noiseless case. We found that this persistence time is maximized for the same noise range that also minimizes the probability of error and ensures synchronization. We believe that the proposed device may serve as a building block for future computing systems which, due to the increasing scale of integration, will have to deal with smaller signal-to-noise ratios.

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