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Performance evaluation of GaN and Si based driver circuits for a SiC MOSFET power switch

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ABSTRACT

Silicon carbide (SiC), new power switches (PSW) require new driver circuits which can take advantage of their new capabilities. In this paper a novel Gallium Nitride (GaN) based gate driver is proposed as a solution to control SiC power switches. The proposed driver is implemented and is performance compared with its silicon (Si) counterparts on a hard switching environment. A thorough evaluation of the energy involved in the switching process is presented showing that the GaN based circuit exhibits similar output losses but reduces the control power needed to operate at a specified frequency.

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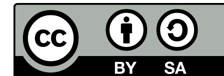

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1. INTRODUCTION

Power electronics technology has always evolved toward higher efficiency, higher power density and more integrated systems [1], [2]. Currently most converters are designed to be embedded into the application housing and therefore its volume is restricted by the size of the product case. This size reduction is achieved using smaller passive elements and higher switching frequencies [3], which poses new challenges system efficiency due to switching and drive losses [4].

Increasing the power density of the system without affecting the overall efficiency requires a performance improvement in the power switches. Unfortunately, silicon (Si) based power devices characteristics are reaching their theoretical limits, and exhibit important limitations regarding blocking voltage capability, operation temperature and switching frequency restricting the use of them [1], [5].

In the past years, a new generation of power devices based on wide bandgap (WBG) semiconductor materials [6] became available as commercial-of-the-shelf (COTS) products. WBG semiconductors, like silicon carbide (SiC) and gallium nitride (GaN), show improved material characteristics making them an excellent option as Si power devices replacements. WBG materials are characterized by their high electrical field strength which allows very thin drift layers with high doping rates [7], [8]. Consequently, devices based on these materials are benefited by reduced on-state resistance leading to reduced conduction losses [9]. Furthermore, carrier mobility in WGB materials is superior than in Si, allowing faster turn-on / off switching times and hence, lowering switching losses.

Power devices based on WBG materials are attractive because of their low input capacitance, low conduction and low switching losses, high operation temperature and high thermal conductivity [10]. The use of these new devices allows increasing the efficiency and a considerable improvement in size and robustness of power converters. In addition to this, SiC is a preferred semiconductor compared to GaN for high-voltage and high-power device applications when both electrical an thermal limitations are considered [11].

Even though power MOSFETs based on SiC have the benefit of being a Normally Off device, their oxide layer creates a large input capacitance [12] which is a challenging problem while designing the driver circuit. This capacitance has to be charged and discharged fast enough to ensure the correct operation of the device. The driver circuit is a critical asset to exploit the superior characteristics on this type of power switch (PSW). Using a driver with insufficient current capability to control the voltage of the gate capacitance will increase switching losses prohibitively, causing the destruction of the device by overheating. The maximum operating frequency of a PSW is bounded by the current handling capacity and the internal losses in the active components of the gate driver circuit. To enable high frequency operation it is critical to reduce them to a minimum [13] while ensuring appropriate drive strength.

Low voltage high electron mobility transistors (HEMTs) based on GaN are good candidates to implement the output stage of a driver circuit. This transistors outperform their Si counterparts in every electrical aspect reducing to a minimum the capacitive load to the controller circuit without compromising the voltage handling or the thermal management of the solution itself. Potential approaches on how to drive SiC MOSFETs have been widely evaluated by [14]-[18], but finally, all of them, implement the drivers using traditional Si based devices. On the other hand, Nagaoka *et al.* [12] introduces for the first time the use of a driver output stage based on GaN HEMTs utilizing discrete custom devices. In addition to Nagaoka's work, Okuda *et al.* [19] show the proof of concept of the GaN HEMT as part of a gate driver that targets a SiC MOSFET in a hard switching environment. Even though Okuda's work proposes the use of COTS devices, the PSW is used at low blocking voltage and drain current. Therefore, no conclusive evaluation has been published regarding the benefits of the use of GaN based devices as active devices in the gate driver circuit.

This work presents the implementation of a PSW gate driver using low voltage GaN HEMTs to control a 1200V SiC MOSFETs plus an in-depth performance evaluation and comparison against equivalent gate drivers using Si based MOSFETs and Bipolar transistors. The rest of the paper is organized as follows: section 2 introduces the concept of the driver topology and the circuit implementation details. Section 3 present the test bench setup used in the Dual Pulse Tester (DPT). Section 4 presents the measurements performed to the each version of the driver. And finally sections 5 conducts discussion on the data gathered and, finally, section 5 shows the conclusions of the work.

2. PROPOSED GATE DRIVER

This section presents the working principles of the proposed PSW gate driver using low voltage GaN HEMTs to control a 1200V SiC MOSFETs. The structure of an SiC MOSFET is such that the gate forms a non linear capacitor [20]. Charging the gate capacitor turns the PSW on and allows current to flow between drain and source terminals, while discharging it turns the device off and a large voltage may then be blocked across the drain and source terminals. The minimum voltage when the gate capacitor is charged and the device can just about conduct is the threshold voltage (V_{TH}). For operating an SiC MOSFET as a switch, a voltage sufficient larger than V_{TH} should be applied between the gate and source terminals.

2.1. Gate driver topology

Figure 1 shows a simplified schematic of the proposed gate driver, an elementary inverter leg structure is made of GaN transistors Q_H and Q_L connected in series between two power supplies V_{ON} and V_{OFF}. The central point of the leg, labeled as "G" in the Figure 1, is connected to the gate of the PSW. When Q_H or Q_L are on resistors R_{GH} and R_{GL} respectively limit the charging current flowing to the gate thus controlling the V_{GS} slew rate and therefore the PSW turn-on / off time. The inductor L_G models the parasitic inductance of the connection to the PSW gate terminal, minimized as much as possible in the design of the PCB.

Gallium Nitride HEMTs EPC-2012 from EPC [21] have been selected as the current booster switches (Q_H and Q_L) due to their high continuous drain current I_D, their high blocking voltage rate V_{DSS}, and their low On-Resistance $R_{DS}ON$. Moreover these transistors presents a fraction of the input capacitance C_{ISS} to the controller in comparison with Si options. Finally their small footprint allows a compact circuit design. Table 1 summarizes the key parameters of the GaN transistor. Resistors R_{BH} and R_{BL} limit the current flow

to the gates of the transistors Q_H and Q_L respectively, reducing the ringing in their gates and lowering the electromagnetic emissions, ensuring a fast transition of the devices while operating them in a secure condition.

The voltages of the isolated power supplies used to actually charge and discharge the gate of the PSW where selected to improve its performance. To turn on the PSW $V_{ON} = 20V$ is used, lowering to the minimum the on resistance (R_{DS-ON}), thus reducing the conduction losses. On the other hand $V_{OFF} = -5V$ was selected to turn off the PSW increasing the noise immunity of the gate of the power device.

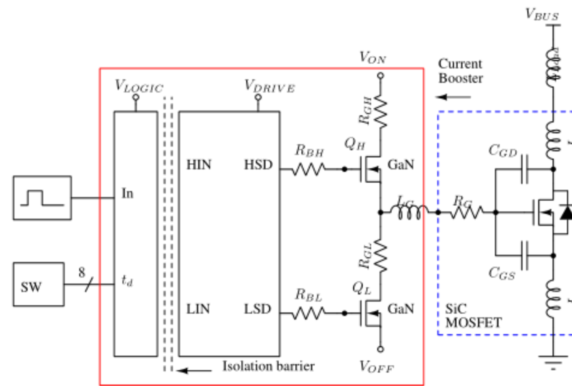


Figure 1. Driver circuit block diagram

Table 1. EPC2012 eGAN transistors key parameters list [21]

Parameter		Value
Breakdown voltage	V_{DS-B}	$200V$
Rated current (Tc=100C)	I_D	$3A$
Gate-source voltage Max	V_{GS-MX}	$-5V/6V$
threshold voltage	V_{TH}	$1.4V$
input capacitance	C_{ISS}	$128pF$
output capacitance	C_{OSS}	$73pF$
gate charge	Q_G	$1.5nC$
on-state resistance	R_{DS-ON}	$70m\Omega$

Operation of the GaN booster stage is achieved using a dedicated controller unit. The unit reads the input signal IN and the dead-time configuration t_D and generates two complementary non overlapping control feeds. These feeds, with the dead-time already injected, are transmitted through the isolation barrier using two high speed Aluminium Gallium Arsenide (AlGaAs) optocouplers. The transmitted signals are sourced into a COTS half bridge controller which finally turns on and off the GaN transistors using a V_{GS} of $V_{DRIVE}/0V$ respectively. For this particular work V_{DRIVE} is $5V$.

Currently GaN HEMTs lacks of a commercially available complementary device. Therefore, to control Q_H, the half-bridge controller must shift V_{DRIVE} voltage and reference it to the source terminal of Q_H which commutes between V_{OFF} and V_{ON}. The t_D is an 8-bit digital input that configures the dead-time (in steps of $20nS$) that is injected in between the state transitions to avoid the undesired shot-through effect in the GaN half-bridge. During the dead-time both Q_H and Q_L are off, and the conduction state of the PSW is retained until it's extinguished. This effect is shown in Figure 2, the shaded zones of the diagram represent the dead-time and its effect in the conduction status of the PSW.

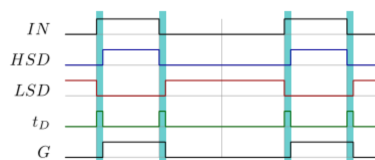


Figure 2. Activation signals of the driver circuit after the isolation barrier

2.2. Operation stages

During a full switching cycle of the PSW the driver circuit goes through four specific stages. A detailed description of the driver operation is shown in Figure 3.

- Stage-1-(S1): signal IN is low and the V_{GSL} of Q_L rises to V_{DRIVE}, turning the device ON. Q_H remains in OFF state ($V_{GSH} = 0V$) and the voltage across V_{GS-PSW} of the PSW is V_{OFF}. During this stage the capacitance $C_{ISS} = C_{GD} + C_{GS}$ is discharged through R_{GL} leaving the PSW in OFF state with no current flow allowed.
- Stage-2-(S2): signal IN changes to high and the dead-time starts running. Q_L is turned off without changing the conduction state of Q_H. The V_{GS-PSW} voltage is maintained by its own input capacitance C_{ISS}.
- Stage-3-(S3): after the dead-time is extinguished and then transistor Q_H is turned ON ($V_{GSH} = V_{DRIVE}$). Q_L remains OFF and the voltage across V_{GS-PSW} rises up to V_{ON}. During this stage the capacitance C_{ISS} is charged through R_{GH} turning on the PSW and allowing the current to flow.
- Stage-4-(S4): signal IN is low and dead-time starts running. Q_H is deactivated while Q_L remains OFF too and the conduction state of the PSW remains unaltered while the dead-time is consumed until Stage-1 begins and the sequence starts all over again.

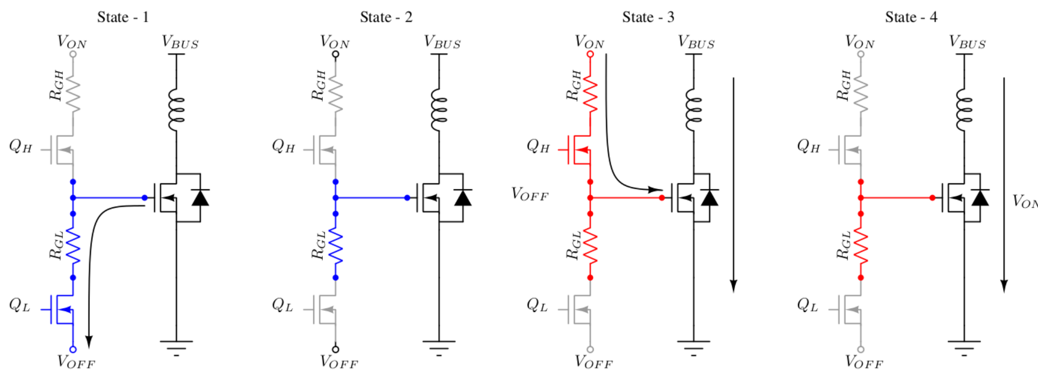


Figure 3. Operation states of the driver and the SiC Power MOSFET

3. EXPERIMENTAL RESULTS

To evaluate the performance of the proposed GaN current booster a prototype was built and tested. Furthermore, for comparative purposes, two variants of the same topology were built one using Si bipolar junction transistor (BJT) FZT1053A [22] and its complementary device FZT951 [23] both from Diodes Inc. and the other one using Si MOSFETs NDT3055 [24], Table 2 describes the main characteristics of each variant.

In order to measure the switching transients and the power losses of the driver and the PSW, a fully configurable Double Pulse Tester (DPT) board [25] with an inductive load was used. This configuration is shown in Figure 4, the dashed box indicates the device under test (DUT). The active device of the DPT is kept unchanged during all the tests. To ensure fast interchangeability and stability in the testbench each tested circuit was designed and built using the same connection footprint.

Table 2. Driver key characteristics

	GAN	MOS	BJT
[l]Booster device FZT951	EPC2012	NDT3055L	[l]FZT1053A and
Footprint	Custom	SOT223	SOT223
Topology	Half bridge	Half bridge	Emmiter follower
PCB Area	$8.14mm^2$	$98mm^2$	$98mm^2$
R_{GH} R_{GL}	10Ω	10Ω	10Ω
R_{BH} R_{BL}	5.6Ω	5.6Ω	56Ω

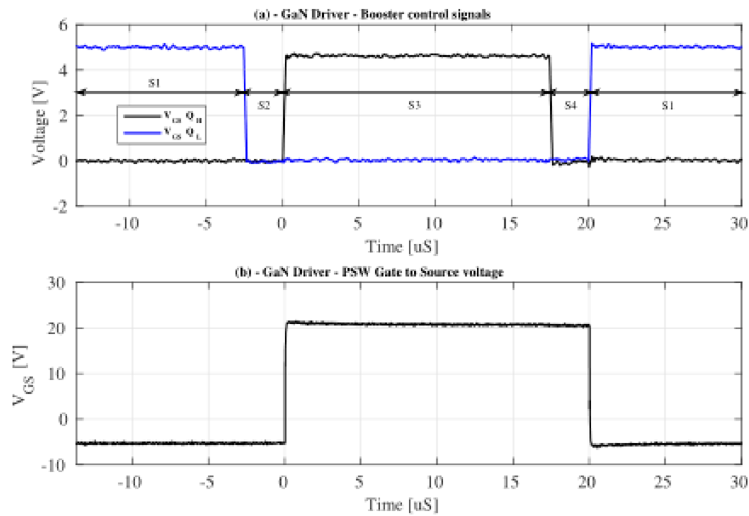


Figure 4. DPT measurement bench schematic with its parasitics components

The load inductor L_{Load} was manufactured with an inductance of $505\mu H$ with an air core to avoid saturation. An ultra fast SiC schottky diode [26] was chosen as a free wheeling diode D_{FW}. The bus capacitance C_{BUS} is composed of a multilayer ceramic and metalized polypropylene film capacitors stack which totalize a capacitance of $5\mu F$ with a maximum rated voltage of $1200V$. The PSW used in the DPT is the SiC MOSFET CMF10120D from CREE [27]. Its key parameters are shown in in Table 3.

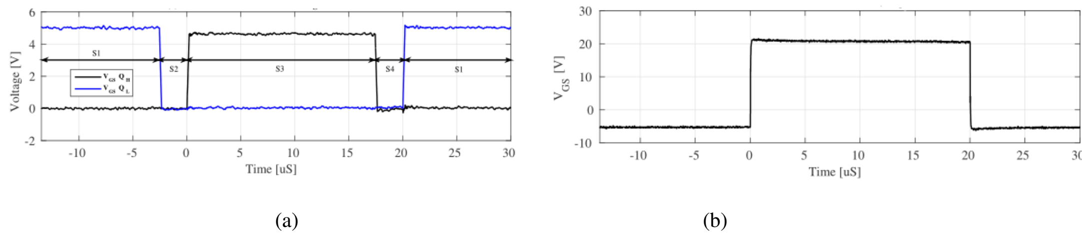
Table 3. CREE CMF10120D transistors key parameters list [27]

Parameter ($T = 25°C$)		Value
Breakdown voltage	V_{DS-B}	$1200V$
Rated current (Tc=100C)	I_D	$24A$
Gate-source voltage Max	V_{GS-MX}	$-5V/+25V$
Threshold voltage	V_{TH}	$3.1V$
Input capacitance	C_{ISS}	[l] $928pF@V_{DS} = 800V$
$1200pF@V_{DS} = 0V$		
Output capacitance	C_{OSS}	$63pF@800V$
Gate charge	Q_G	$47.1nC$
On-state resistance	R_{DS-ON}	$190m\Omega$

The test was carried out aplying two pulses of different durations on the gate of the PSW. To set the drain test current of the PSW to $I_D = 22A$ a *current build-up* pulse with a duration of $T_{build_up} = 20\mu S$ was used with a bus voltage of $V_{BUS} = 580V$. Finally, the turn on time was $T_{ON} = 2.5\mu S$, and the operation frequency was defined as $f_{sw} = 125KHz$ with a duty cycle $D \sim 30\%$. During the measurements the test circuit remains unchanged, only the gate driver is replaced to comapre each variant. All voltage measurements were performed using a *Tektronix THS3014* with four isolated floating channels oscilloscope. As a current transducer a Pearson Electronics INC. current monitor Model: 2878 [28] was used. During the realization of the measurements all the best practices described in [29] were enforced.

3.1. Driver control signals

Figure 5 (a) shows the V_{GS} voltage of each transistor at the output stage in the GaN based driver during the current build up pulse. During the dead-time periods in S2 and S4 both switches, Q_H and Q_L, are off avoiding the shoot-through effect in the GaN half bridge leg. Also it is possible to see that drive voltage level for Q_H is lower lower than for Q_L due to the effect of the bootstrap diode of the half-bridge controller. Figure 5 (b) exhibits the voltage signal generated by the gate driver with the dead-time already injected showing that the dead-time has no direct influence in the pulse conformation.

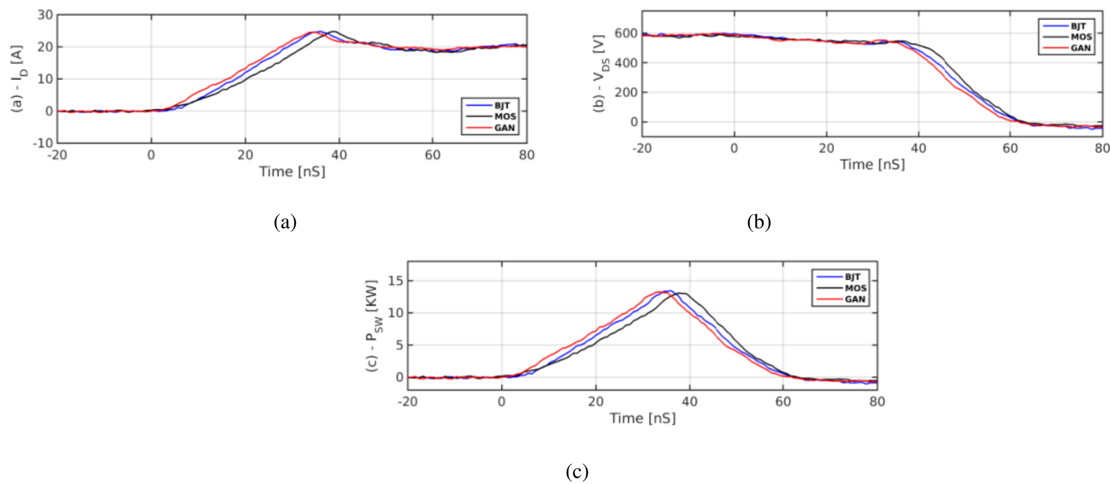


(a) (b)

Figure 5. These figures are; (a) Control signals of the GaN transistors with the dead-time injected during the current build up pulse; (b) PSW gate to source voltage generated by the GaN gate driver during the current build up pulse

3.2. Turn-on characterization

Figure 6 shows the drain-source current I_{DS}, drain-source voltage V_{DS} and instantaneous power P_D during the turn-on transient of the PSW for each driver technology. Because of the inductive nature of the load used in the DPT, at the start of the test pulse, the freewheeling diode D_{FW} conducts the full test current. The PSW current I_D shown in Figure 6 (a) increases displacing the D_{FW} current while the PSW drain voltage V_{DS}, shown in Figure 6 (b), is clamped to the bus voltage V_{BUS} because of the conducting freewheel diode. When the PSW conducts the test current in full, D_{FW} is recovered and blocked. Afterwards the voltage V_{DS} falls down to the on-state level. The instantaneous power dissipated in the PSW was obtained combining V_{DS} and I_{DS} and the result is shown in Figure 6 (c). The shape on each curve is mostly triangular and compatible with an inductive switching. A summary the measurements during the turn-on stage is detailed in Table 4.



(a) (b)

(c)

Figure 6. Electrical quantities measured on the SiC MOSFET during the Turn ON period; (a) Turn ON drain current; (b) Turn ON voltage; (c)Turn ON instantaneous power

Table 4. SiC MOSFET switching ON: transient measurement summary

	GaN	MOS	BJT
Turn-on time (ns)	41	45	41
V_{DS} Fall-time (ns)	21	20	21
V_{DS} Slew-rate ($^{V}/_{nS}$)	-23	-24	-23
I_{DS} Rise-time (ns)	20	25	20
I_{DS} Slew-rate ($^{A}/_{nS}$)	0.8	0.7	0.8

3.3. Turn-off characterization

Figure 7 shows the drain-source current I_{DS}, drain-source voltage V_{DS} and instantaneous power P_D values during the turn-off transient of the PSW for each driver technology. As the on test time for GaN and BJT

drivers differs from the used with the MOS driver the switch off information was separated for clarity: Figures 7 (a), (c), and (e) show the transients for GaN and BJT drivers while Figure 7 (b), (d), and (f). During the off transition the PSW device conducts the test current as the V_{DS} voltage, shown in Figure 7 (a) and (b), rises up to the supply rail. When the voltage transient ends, D_{FW} becomes forward-biased and begins to conduct displacing the PSW current I_{DS}, and falling down to zero as shown in Figures 7 (c) and (d). Figures 7 (e) and (f) show the instantaneous power dissipated in the PSW and in the same way than during the turn-ON transient it presents a triangular shape compatible with a pure inductive switching. A summary of the measurements during the turn-off stage can be found in Table 5.

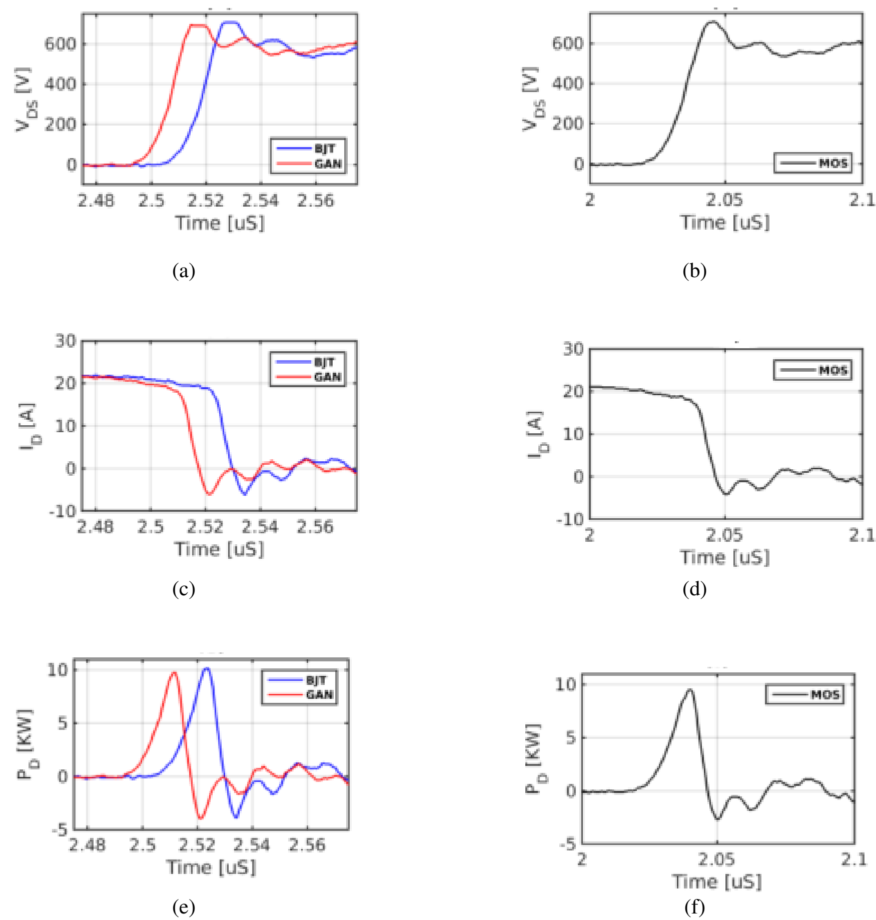


Figure 7. Electrical quantities measured on the SiC MOSFET during the Turn OFF period; (a) Turn ON drain-source voltage for GAN and BJT; (b) Turn ON drain-source voltage for MOS; (c) Turn OFF drain current for GAN and BJT; (d) Turn OFF drain current for MOS; (e) Turn OFF instantaneous power for GAN and BJT; (f) Turn OFF instantaneous power for MOS

Table 5. SiC MOSFET switching OFF: transient measurement summary.

	GaN	MOS	BJT
Turn-off time (ns)	19	22	20
V_{DS} Rise-time (ns)	12	13	13
V_{DS} Slew-rate $({}^{V}/_{nS})$	40	36	37
I_{DS} Fall-time (ns)	7	9	7
I_{DS} Slew-rate $({}^{A}/_{nS})$	-2.4	-1.9	-2.5

3.4. PSW switching energy and driver losses

The switching action of the PSW and the driver itself result in unavoidable losses. The operation of turning on or off the PSW involves the charging and discharging process of the gate capacitance and, therefore,

a certain amount of charge has to be transferred. The power lost due to the driving the PSW input capacitance process is dissipated in the output stage components of the gate driver circuit formed by R_{GH}, R_{GL}, Q_H and Q_L and is computed as *Output losses*. To accomplish this operation the control stage has to command the output devices Q_L and Q_H during the switching process, hence dissipating energy. The power dissipated during the control operation is accounted for in the *control losses*. The driver power losses are summarized in Table 6. In addition to this the switching energy of the PSW during a full period is $470\mu J$ within $1 \pm \%$ despite the gate driver technology.

4. DISCUSSION

This section discusses the results obtained on the bench tests of the PSW using the proposed GaN based gate driver and compares it against their Si based BJT and MOSFET counterparts.

Table 6. Gate drive power dissipation

	GAN	MOS	BJT
Output losses (W)	2.3	2.4	1.9
Control losses (W)	2	33	290

4.1. PSW Current and voltage behavior

Figures 6 and 7 show the voltages and currents in the PSW when is turned on and off using the GaN, BJT and MOSFET drivers. GaN and BJT drivers produce similar voltages, currents and instantaneous power signals. During the turn-on process the rise times of I_{DS} are similar to the V_{DS} taking 20ns to reach the test current and 21ns to achieve full voltage swing, with a total time of 41ns. During the turn-off process the PSW drain current fall time achieves 7ns, while it takes 12ns and 13ns to the GaN and BJT drivers respectively to block the PSW and withstand the full test voltage totalizing a turn-off time of 19ns for GaN driver and 20ns for the BJT variant. Nevertheless, the PSW shows a slower behavior under the control of the MOS driver taking 25ns, a 25% more time, to the device to achieve the test current. Due to the inductive load, the V_{DS} transient start is delayed increasing the total turn-on switching time in 10% totalizing 45ns. During the turn-off the PSW takes 13ns to block the voltage and 9ns to reduce the I_{DS} to zero computing a turn-off time of 22ns.

Figure 8 shows that the MOS gate driver produces a slower V_{GS} slew-rate in the PSW unlike GaN and BJT drivers that exhibit a similar performance. As the output transistors on each driver were selected to have similar current and blocking voltage capacity, the drive strength of each driver implementation is actually limited by the external resistor, R_{GH} or R_{GL}, depending on the transition, plus the contribution of the PSW internal resistor R_G. As shown in Figure 9 (a) when the driver switches from $S2$ to $S3$, to turn on the PSW, Q_H charges the output capacitance composed of C_{OSS}^{QL} and C_{ISS}^{PSW}. Conversely in Figure 9 (b) when the driver switches from $S4$ to $S1$, turning off the PSW, Q_L discharges the gate capacitance, made up by C_{OSS}^{QH} and C_{ISS}^{PSW}.

In Table 7 summarises the output capacitance of the transistors used, it is possible to see that during the $S2 \mapsto S3$ transition, the driven gate capacitance using the GaN driver is 25% smaller than the MOS version, and 50% smaller than the BJT option. In the same way, during the $S4 \mapsto S1$ transition, the driven gate capacitance the GaN solution is 30% smaller than the MOS, and 23% smaller than the BJT. Furthermore, both MOS and GaN driver half-bridge controllers use a supply voltage of $V_{DRIVE} = 5V$ for the output stage in addition to a bootstrap capacitor to operate the high side of the leg with the consequence of reducing the overdrive. While this voltage proves to be sufficient to turn-on the EPC2012 it's not enough for the NDT3055 MOSFET which typically needs 10V of VGS to operate at its full electrical characteristics therefore slowering the V_{GS} rise-time in the MOS driver. Despite the downgraded performance of the MOS driver, all three circuits produce almost the same switching energy loss in the PSW under the same operation condition. These results are consistent with the switching energy informed in the PSW's device datasheet [3]. The slightly increase in switching loss of the MOSFET version is related to its slower performance, but is neglectable in comparison with the absolute energy value.

4.2. Driver loss assessment

The Output Power of each driver show similar losses on each technology variant. BJT exhibits a reduction in 25% on the output loss due to the scatter of the on-resistance $R_{CE}ON$ on each device of the

output stage. On the other hand GaN shows a great improvement in the control losses with 2mW, 14 times smaller than MOS and 145 times smaller than needed for the BJT output stage.

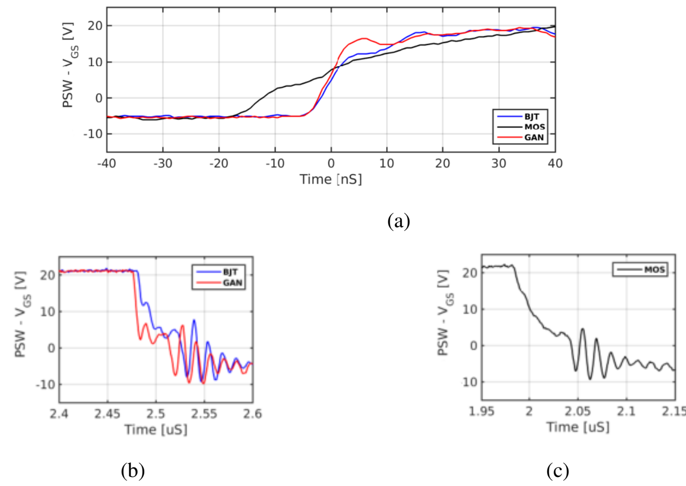


Figure 8. PSW gate to source voltage; (a)Turn ON voltage for GAN, BJT and MOS; (b) Turn OFF voltage for GAN and BJT; (c) Turn OFF voltage for MOS

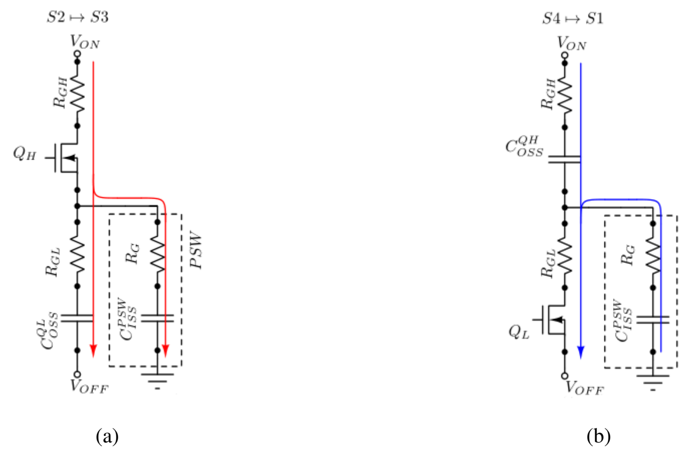


Figure 9. Current flow during the activation of the driver circuit after the isolation barrier; (a) (S2 → S3) current flow during Turn ON; (b) (S4 → S1) current flow during Turn OFF stage

Table 7. Driver transistor output capacitance

Device	EPC2012 [21]	NDT3055L [24]
$C_{OSS}@V_{DS} = 0V\ (pF)$	250	600
	FZT1053A [22]	FZT951 [23]
$C_{JE}@V_{CE} = 0V\ (pF)$	520	1150

5. CONCLUSIONS

A GaN based gate driver was proposed, simulated and experimentally validated in an inductive hard switching environment using a DPT bench with a state of the art SiC MOSFET as active device. Its performance was compared against similar solutions using Si based BJT and MOSFET transistors and during all the evaluations the PSW shows equivalent performance with almost equal switching losses. This is explained since the switching process is dominated by the external gate resistors R_{GH} and R_{GL} neglecting the effects of the on-resistance of the driver output transistors. All three drivers show similar *output losses* due to the fact that

the transistor for each driver were selected with similar electrical output characteristics. On the other hand the GaN driver control loss is negligible in comparison with the BJT and MOS variants relaxing the requirements of the control logic. Finally the GaN based output stage is 12 times smaller. This area reduction in addition to enhanced characteristics of the GaN material makes this option suitable to integrate directly in a dedicated power module reducing the circuit parasitics

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