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Multi-structure Power Converter with H-bridge Series Regulator suitable for High-Current High-Precision Pulsed Current Source

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***Abstract*—This work presents a novel multi-structure power converter capable of generating high current pulses with short rise and fall times, and high precision in the flat-top. The proposed topology is based on the use of three conversion structures operated with current, voltage and switching frequency ratings in line with the different requirements of each pulse stage. In order to achieve the required precision, a switched-mode compensation structure in series with the load is used. Though this structure must handle a high load current, it is designed to deviate most of the load current to an auxiliary inductor; thus reducing the semiconductor devices requirements. Moreover, the use of this compensation strategy results in a first-order model of the circuit, which leads to an oscillation-free response during structures interconnection. This feature minimizes the required flat-top time, which in turn decreases the power losses on the load. Experimental results based on a scaled-down laboratory prototype validate the capability of the proposed topology to produce current pulses according to the specifications of high-precision applications.**

***Index Terms*—Pulsed power supplies, Pulse generator, Septum, Particle accelerator, Current control, Switched-mode power supply.**

I. Introduction

PARTICLE accelerators applied to high-energy physics and clinical treatments employ high-current converters to produce a high-magnetic field on a magnet, which has to be constant throughout the beam length [1]–[5]. In particular, power converters used in septum magnets demand specific technical solutions due to their operational conditions [6]–[9]. For these applications, a key aspect of these converters is that they should deliver high current pulses, with high current stability and precision during the pulse flat-top. Although current rise and fall times are not critical, they should be reduced so as to decrease the output Root Mean Square (RMS) current value and minimize the power losses in the magnet load and its related cooling.

Depending on the application operational conditions and on the different magnets, which are modeled as RL loads, this type of converters are designed to produce current pulses of tens of kA, with a precision in the order of hundreds of parts-per-million (ppm), and flat-top durations up to 10 ms and as low as a few hundreds of μs. Considering typical values of output currents and loads for septum applications, a matching transformer with a suitable transformation ratio is generally used to connect the load to the power converter. The matching transformer adapts the load waveforms to more practical current and voltage values for the power converter, therefore standard capacitors on the primary side can be used [7], [8]. Table I shows typical load values and pulse parameters for a wide range of septum applications.

TABLE I: Primary side power converter requirements.

Matching transformer ratio	∼1:10
Maximum pulsed output current	0.2 - 2 kA
Load inductance	0.1 - 1 mH
Load resistance	10 - 100 mΩ
Flat-top duration	0.1 - 2 ms
Current precision	100 - 1000 ppm
Repetition rate	∼2 Hz

Even though the solution offered to these pulsed converters has been, for many years, the use of a capacitor discharge topology [9]–[13], certain drawbacks in this system (low flexibility and high RMS load current value) have created the need of a new development based on switching converters. For this kind of applications, a trapezoidal waveform is the best possible solution to reduce the RMS current in the load.

The primary side load current, i_L, and the required average voltage, v_{Load}, to generate this waveform over an inductive load are shown in Fig. 1, where I_{REF} is the flat-top reference current. In order to reduce rise and fall times, t_r and t_f respectively, a high voltage, V_H, should be applied during these stages. Taking into account the specifications in Table I, this voltage may be of several kilovolts. On the other hand, due to the resistive component of the load, a lower average voltage of hundreds of volts, V_L, must be generated during flat-top time, t_{ft}. Since a precision of a few hundreds of ppm is required, the use of a single high-voltage converter implies switching the power semiconductors at high frequencies in relation to their current handling capacity. These requirements cannot be fulfilled by current semiconductor devices [14]–[18].

In order to overcome this technological limitation, a multiple structure converter based on different structures, each one specific to a particular operation range in terms of voltage, current and switching frequency, can be used. These struc-

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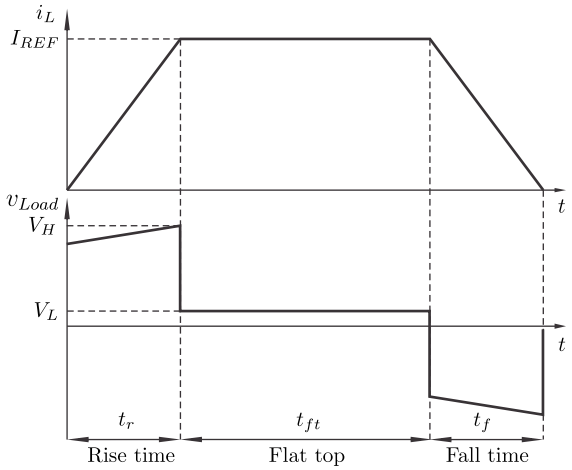

Fig. 1: Current and voltage waveforms on an inductive load.

tures should be connected during one or more stages of the generated waveform to accomplish the specific requirements corresponding to each stage. In this sense, a two-structure voltage converter, based on a high voltage structure for the rise and fall times and a low voltage structure to control the flat-top current, is proposed in [19]. This approach allows to reach the reference current in a shorter time and to decrease the switching frequency at the flat-top when compared to a single structure converter. As shown in [19], this topology results an appropriate solution when moderate currents and precisions are required. However, since the flat-top structure must handle a high output current, precision is bounded by the maximum switching frequency of its high current semiconductors. Consequently, the use of this approach in septum applications as those previously mentioned is restricted.

In [20] a multiple structure converter based on three structures is proposed. As in [19], this converter uses a high voltage structure so as to reduce the pulse rise and fall times. During the flat-top stage, the precision requirement is accomplished by using two low voltage structures: one structure with high current and medium switching frequency to control the flat-top current with moderate precision, and the other with low current and high switching frequency to achieve the required precision. These structures are connected in parallel with the load and are operated as current controlled sources. Then, the inductive nature of the load requires the addition of a capacitor in the interconnection point so as to avoid possible overvoltages. However, the addition of this capacitor produces the existence of undesirable transient responses during structures interconnection, leading to an increase of the settling time. As a result, longer flat-top times must be generated, thus a higher energy is supplied to the load [20]. Moreover, since the load energy is supplied by capacitor banks, the required capacitance increases and consequently the sizing of their chargers, which has a direct impact on the cost and volume of the whole power source. Concerning the power semiconductors, the structure with high current and medium switching frequency results the most demanding structure, as it has to deliver currents of some kA at a switching frequency of some kHz.

This work presents a new multiple structure topology based on the use of a voltage source in series with the load so as to obtain the required flat-top precision. The use of this compensation structure allows to obtain a free transient response interconnection with a simple hysteresis controller. When compared to the previous topologies, the regulation structure of the proposed system presents lower current, voltage and switching frequency specifications, which alleviate the operation of the power semiconductors. Additionally, the proposed topology is designed to recover most of the energy so as to reduce the power requirements of the capacitor chargers.

The proposed topology is presented in Section II, where its operational principle and several aspects associated to the topology operation at each pulse stage are described. An application case of the proposal over a high-current high-precision pulsed current source used for a septum magnet is presented in Section III. Finally, Section IV provides experimental results from a laboratory prototype, and Section V summarizes the conclusions drawn from this work.

II. Proposed topology

A. Operating principle

Fig. 2 depicts the general scheme of the presented converter topology, where the charger systems for the capacitors C_H, C_L and C_B have been omitted for the sake of clarity.

This topology is composed of three main structures. Structure 1 is used to obtain short rise and fall times by adjusting the initial high voltage of C_H. Structure 2 is used to supply most of the required energy during flat-top by connecting C_L in series with the load, while Structure 3 is used to regulate the load current with the required precision by controlling the applied voltage with an H-bridge. Thus, in order to reduce the voltage requirements of the latter structure, the initial voltage of C_L is set close to the voltage drop given by the resistive component of the load, i.e. $I_{REF}R$. Additionally, since the

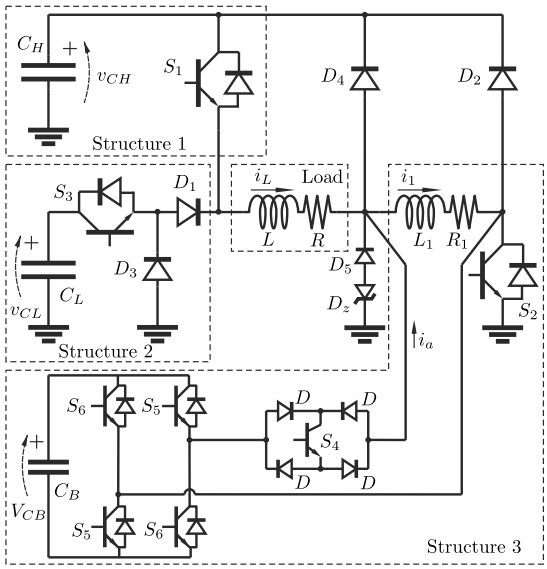

Fig. 2: Multi-structure proposed topology.

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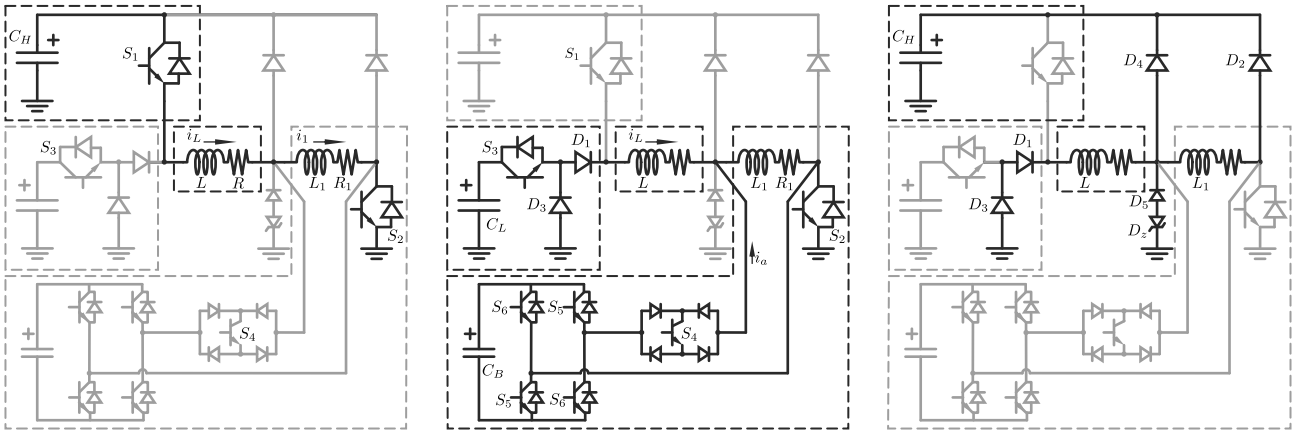

a) Rise Time b) Flat-top Time c) Fall Time

Fig. 3: Equivalent circuit on each pulse stage.

H-bridge is in series with the load, an auxiliary inductor, L_1, is added so as to derive most of the load current; thus, the H-bridge only handles a minor fraction of this current. It should be noted that the reduction of both the voltage and current of the regulation structure allows to increase the switching frequency, and therefore, to improve the precision in the output current.

The operation of the topology for the different pulse stages, illustrated in Fig 3, can be summarized as follows:

- Rise time (Fig. 3.a): During this stage, Structure 1 is activated and Structure 2 is disconnected by turning on S_1 and S_2, and turning off S_3. Regarding Structure 3, the H-bridge is disconnected by turning off S_4, while L_1 remains in series with the load. This condition initiates the charge of L and L_1 through the high-voltage v_{CH}.
- Flat-top (Fig. 3.b): When current $i_L = i_1$ reaches the reference value I_{REF}, Structure 1 is disconnected and Structure 2 and the H-bridge of Structure 3 are connected by turning off S_1 and turning on S_3 and S_4. Then, since a constant current is drawn from C_L, v_{CL} has a linear voltage decrease. In order to compensate such voltage variation and achieve the required precision, the average voltage on L_1, R_1, is controlled by means of the PWM mode operation of S_5 and S_6.
  Diodes D_1 and D_3 ensure a safe connection/disconnection between Structures 1 and 2. D_1 blocks the voltage v_{CH} when Structure 1 is connected, so lower voltage devices could be chosen for S_3 and D_3; and D_3 ensures a circulation path for i_L in case S_1 and S_3 are simultaneously off.
- Fall time (Fig. 3.c): To decrease the load current, all switches are turned off. The energy stored in L and L_1 returns to the capacitor bank C_H through D_1, D_2 and D_3. D_4, D_5 and D_z are used to conduct the differences of current between L and L_1 when the H-bridge is disconnected.

B. Topology analysis

This section describes the main aspects related to the topology operation in each pulse stage. Moreover, the equations that define the system operational conditions as a function of the pulse requirements are obtained. Such equations allow to evaluate the operational range of each device in order to size them. In this analysis, the semiconductor voltage drops are considered negligible for being low, when compared to the voltages employed in the topology.

Rise time: Considering a linear current variation, the initial voltage V_{CH} needed to meet the rise and fall times is obtained from:

$$V_{CH} = \frac{I_{REF} \cdot (L + L_1)}{t_r} + I_{REF} \cdot (R + R_1) \qquad (1)$$

L_1 is adopted approximately an order of magnitude smaller than the load inductance, so as not to significantly increase V_{CH}. Moreover, since C_H, L and L_1 form a resonant circuit, sinusoidal waveforms for i_L and v_{CH} are obtained during the rise time. Then, the value of C_H is calculated to obtain an error between the RMS output current value and the RMS value of a linear current evolution, e_{RMS}, below 5%.

Flat-top: In the flat-top, the load current must be controlled with the required precision. In this stage, the closed loop control of i_L is carried out by a fixed band hysteresis modulator, which controls the H-bridge switches of Structure 3 to define the series voltage v_1. This simple control features a high-dynamic response and provides the required precision by keeping the current within the comparison bands.

Fig. 4 represents an equivalent circuit of the system, where the H-bridge is modeled as a controlled voltage source. Additionally, C_B is selected high enough so as to ensure a constant V_{CB}. Then, the voltage on the load inductance is given by:

$$v_L = v_{CL} - I_{REF} \cdot R - v_1 \qquad (2)$$

where v_1 can adopt the values $\pm V_{CB}$ depending on the state of the H-bridge switches. Additionally, since C_L is designed to have a low voltage variation, the voltage over the load within a commutation period can be assumed to be constant

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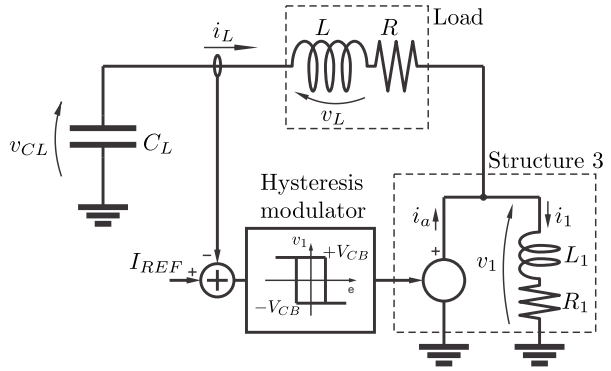

Fig. 4: Flat-top equivalent model.

and the system dynamics can be considered to be of first order. Furthermore, since the H-bridge switching frequency is usually much higher than the load dynamics, the load is supposed to have a linear current variation. Fig. 5 illustrates the current and voltage waveforms within a commutation period.

In this condition, the current variation for the ON and OFF states, ΔI^+ and ΔI^-, respectively, are given by:

$$\Delta I^+ = \frac{{v_L}^+}{L} t_{on} = \frac{v_{CL} - I_{REF}R + V_{CB}}{L} t_{on}$$
$$\Delta I^- = \frac{{v_L}^-}{L} t_{off} = \frac{v_{CL} - I_{REF}R - V_{CB}}{L} t_{off} \quad (3)$$

To ensure the control capability of the compensator, the following conditions must be met, ${v_L}^+ > 0$ and ${v_L}^- < 0$, then:

$$V_{CB} > |v_{CL} - I_{REF}R| \quad (4)$$

Since the fixed band hysteresis controller imposes that $\Delta I^+ = -\Delta I^- = \Delta I$, the duty cycle is defined by:

$$D \triangleq \frac{t_{on}}{t_{on} + t_{off}} = \frac{V_{CB} + I_{REF}R - v_{CL}}{2 \cdot V_{CB}} \quad (5)$$

From this equation, it should be noted that the discharge of C_L produces an increasing variation of the duty cycle. Therefore, by replacing the value of the capacitor voltage on (5) at the beginning and at the end of the flat-top, $V_{CL}(0)$ and $V_{CL}(t_{ft})$ respectively, the minimum and maximum range of the duty cycle can be obtained.

$$D_{min} = \frac{V_{CB} + I_{REF}R - V_{CL}(0)}{2 \cdot V_{CB}}$$
$$D_{max} = \frac{V_{CB} + I_{REF}R - V_{CL}(t_{ft})}{2 \cdot V_{CB}} \quad (6)$$

Taking into account that $D \triangleq f \cdot t_{on}$, the switching frequency, f, as a function of the duty cycle is given by:

$$f(D) = 4 \cdot f_{MAX} \cdot D(1 - D) \quad (7)$$

where:

$$f_{MAX} = \frac{V_{CB}}{2 \cdot \Delta I \cdot L} \quad (8)$$

Equation (8) shows that the maximum switching frequency, f_{MAX}, can be adjusted by means of V_{CB} since the load inductance as well as the current precision are imposed by the application. Then, given the maximum and minimum duty cycles, D_{min} and D_{max} respectively, the frequency range of Structure 3 can be calculated, which establishes the power losses of the semiconductor devices for this structure.

An important design aspect of this converter is the average current provided by the H-bridge over each commutation period, $\langle i_a \rangle$. This current depends on the average voltage $\langle v_1 \rangle$ that must be applied in order to compensate the linear voltage decrease across C_L given by:

$$v_{CL}(t) = -\frac{I_{REF}}{C_L} \cdot t + V_{CL}(0) \quad (9)$$

Then, the average values of v_1 and i_1 are given by:

$$\langle v_1 \rangle(t) = (V_{CL}(0) - I_{REF}R) - \frac{I_{REF}}{C_L} \cdot t \quad (10)$$
$$\langle i_1 \rangle(t) = K_1(1 - e^{-\alpha t}) - K_2 t + I_{REF} \quad (11)$$

where:

$$K_1 = \left[\frac{V_{CL}(0)}{R_1} + I_{REF} \left(\frac{L_1/C_L}{R_1^2} - \frac{R}{R_1} - 1 \right) \right] \quad (12)$$
$$K_2 = \frac{I_{REF}}{R_1 C_L}; \quad \alpha = \frac{R_1}{L_1} \quad (13)$$

As a result, the average current supplied by the H-bridge can be calculated as:

$$\langle i_a \rangle(t) = K_1(1 - e^{-\alpha t}) - K_2 t \quad (14)$$

From this equation, it should be noted that, for a given R, R_1 and L_1, both C_L and $V_{CL}(0)$ define the temporal evolution of the average current. Fig. 6 presents the three possible cases of such evolution for the flat-top interval: monotonically increasing, monotonically decreasing and non-monotonic with a positive maximum within the flat-top time, where the time for the maximum current value, t_M, satisfies:

$$\frac{K_2}{\alpha K_1} = e^{-\alpha t_M} \quad (15)$$

In order to reduce the current value that the H-bridge must handle, a non-monotonic evolution with equal positive peak and final flat-top current magnitude is adopted. Then:

$$\langle i_a \rangle(t_M) = -\langle i_a \rangle(t_{ft}) = \langle \hat{i_a} \rangle \leq \langle \hat{i_{amax}} \rangle \quad (16)$$

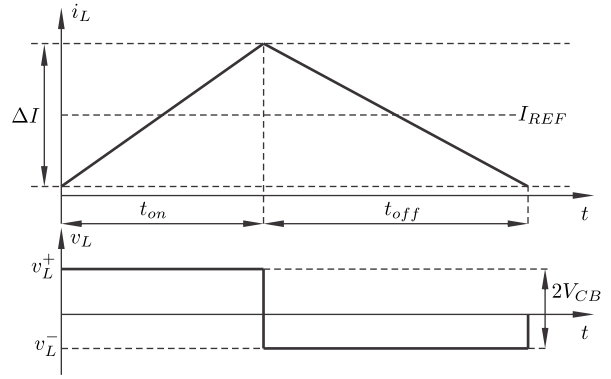

Fig. 5: Load current and voltage waveforms for a commutation period.

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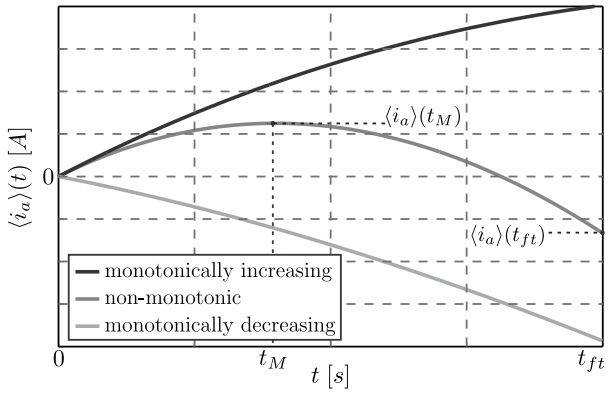

Fig. 6: Different cases of temporal evolution for average auxiliary current in the flat-top.

where $\langle \hat{i_a} \rangle$ is the peak value of the H-bridge current and $\langle \hat{i}_{amax} \rangle$ is the maximum design value defined so as to ensure a safe operation range for the semiconductors devices of Structure 3.

Then, operating with Eq. (14) and (16), and defining X_0 as (17), expression (18) can be obtained.

$$X_0 = \left[\frac{V_{CL}(0)}{I_{REF}} - (R + R_1) \right] \frac{C_L R_1}{L_1} \tag{17}$$

$$\frac{1}{X_0} \ln \left(\frac{1}{1+X_0} \right) = -\left[\left(1 + \frac{1}{X_0} \right) \left(1 - e^{-\alpha t_{ft}} \right) - \frac{\alpha t_{ft}}{X_0} \right] \tag{18}$$

This last equation shows that the auxiliary variable X_0 can be solved as a function of αt_{ft}. Then, since α is a design parameter of the converter, the solution of this transcendental equation can be computed off-line for different t_{ft}. Furthermore, a table with the different pairs of (X_0, t_{ft}) can be stored in advance. Then X_0 allows to obtain the values of both converter parameters C_L and $V_{CL}(0)$.

$$C_L = \frac{\left[X_0 + \ln \left(\frac{1}{1+X_0} \right) \right]}{\alpha R_1} \frac{I_{REF}}{\langle \hat{i_a} \rangle} \tag{19}$$

$$V_{CL}(0) = I_{REF} \left(\frac{L_1}{C_L R_1} X_0 + R + R_1 \right) \tag{20}$$

Equation (19) is used to define the value of C_L so as to bound the maximum current Structure 3 must handle, $\langle \hat{i}_{amax} \rangle$. Furthermore, the value of C_L should be designed for the most restrictive condition. By applying implicit differentiation to (18) and taking into account that $X_0 > 0$, which results from considering $t_M > 0$ and operating with (15), it can be demonstrated that the solution of this transcendental equation gives a monotonically increasing relationship between the auxiliary variable X_0 and αt_{ft}. Then, the value of C_L must be calculated for $I_{REF\,max}$ and $t_{ft_{max}}$.

Finally, once C_L has been selected, Eq. (20) defines the initial voltage $V_{CL}(0)$ as a function of X_0, i.e. t_{ft}, and I_{REF}. Since this voltage can be set before the pulse is triggered, a pulse-to-pulse modulation both in flat-top duration and amplitude can be carried out. It must be pointed out that the voltage rating of C_L is given by solving this equation for the maximum t_{ft} and I_{REF}.

Fall time: In this stage, the energy stored in both inductors is recovered in C_H. This feature is of great importance since it allows to significantly reduce the sizing of the chargers required for the capacitor banks. Then, the recovered energy can be estimated with (21) by evaluating the voltage v_{CH} at the end of the pulse.

$$V_{CHf} = \sqrt{{V_{CHi}}^2 - V^2} \tag{21}$$
$$V^2 = \frac{I_{REF}^2 [(2/3)(t_r + t_f) R_{eq}]}{C_H}$$

where V_{CHi} and V_{CHf} are the voltages on C_H at the beginning and at the end of the pulse, respectively, V^2 is related to the energy dissipated in R and R_1 during t_r and t_f, and $R_{eq} = R + R_1$. Notice that if the ESR of capacitor C_H is relevant compared to R and R_1, it must be included in the expression of R_{eq}.

C. Design procedure and power devices requirements

Table II presents a summarized step-by-step procedure to obtain the main parameters of the proposed topology. This table includes the required equations and the considerations that have to be taken into account in order to obtain either a parameter or an input for the following step. Finally, Table III summarize the resulting operational conditions for the semiconductor devices as a function of the system variables, where f_P is the pulse repetition frequency.

TABLE II: Design procedure steps

N° Step	Used Eq.	Consideration	Obtained Parameter
1	-	$L_1 = \%L$	L_1, R_1
2	-	$e_{RMS} \leq 5\%$	C_H
3	Eq.(1)	-	V_{CH}
4	Eq.(18)	-	X_0
5	Eq.(19)	$\langle \hat{i}_{amax} \rangle$	C_L
6	Eq.(20)	-	$V_{CL}(0)$
7	Eq.(8)	Eq.(4), f_{MAX}	V_{CB}

TABLE III: Semiconductor devices operational conditions

Devices	Voltage	Current	Frequency
$S_{1,2}, D_{1,2,4,5}$	High (V_{CH})	High (I_{REF})	Low(f_P)
S_3, D_3	Low (V_{CL})	High (I_{REF})	Low (f_P)
S_4, D	High (V_{CH})	Low ($\sim \langle \hat{i_a} \rangle$)	Low (f_P)
S_5, S_6	Low (V_{CB})	Low ($\sim \langle \hat{i_a} \rangle$)	Medium (f_{MAX})

III. Application Case

As an example, the use of the proposed topology is evaluated in a high-current high-precision pulsed current source used for a septum magnet in beam injection. Table IV presents the load and pulse characteristics in this application, where the pulse repetition frequency is about 1 Hz. In this table, L, R values include both the magnet elements themselves and the parasitic elements used to connect the converter to the

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TABLE IV: Primary side load and current pulse parameters.

$L = 1\,\text{mH}$	$R = 100\,\text{m}\Omega$
$I_{REF_{max}} = 2\,\text{kA}$	Precision $= \pm 1000\,\text{ppm}$
$t_{ft_{max}} = 2\,\text{ms}$	$t_r, t_f < 1\,\text{ms}$

load (resistance and inductance from wiring, connectors, etc.), referred to the primary side of the interconnection transformer.

The parameters of the power converter are obtained using the design procedure steps indicated in Table II. The value of the auxiliary inductor L_1 is selected 10 times smaller than the load inductor so as not to significantly influence the initial voltage on C_H. With regards to the parasitic resistance R_1, its value can be defined taking into account the associated power losses. In this case, $R_1 = 10\,\text{m}\Omega$ is adopted. Using (1), the value of the voltage in C_H is obtained, resulting $2500\,\text{V}$. Then, in order to obtain an error lower than 5% between the RMS of the output current and the RMS of a linear current evolution during the rise time, $C_H = 5\,\text{mF}$ is chosen. As explained in Section II-B, the solution of (18) provides the values of X_0 as a function of αt_{ft}. Then, the maximum value of X_0 is obtained from $t_{ft_{max}}$. Using this value in (19) and taking into account the trade-off between the maximum current that supplies the H-bridge and the value of capacitor C_L, $\hat{i_{a}}_{max} = 0.1 \cdot I_{REF}$ is defined, leading to $C_L = 35\,\text{mF}$. The maximum voltage in C_L is obtained from (20), which results in $300\,\text{V}$. Finally, taking into consideration the voltage and current ratings that must withstand the active filter, a maximum switching frequency of $10\,\text{kHz}$ is adopted. Then, a value of $V_{CB} = 80\,\text{V}$ is obtained from (8). Table V lists the values and maximum ratings of the main elements of the full-scale prototype. From such parameters and those in Table III, it can be noted that the operational range required for the devices of each structure allows the use of standard semiconductor devices.

TABLE V: Full-scale parameters with series-compensation.

L_1	$100\,\mu\text{H}$	R_1	$10\,\text{m}\Omega$
C_H	$> 2\,\text{mF}$	V_{CH}	$2500\,\text{V}$
C_L	$> 35\,\text{mF}$	V_{CL}	$300\,\text{V}$
C_B	$> 10\,\text{mF}$	V_{CB}	$80\,\text{V}$
f_{max}	$10\,\text{kHz}$	$\langle \hat{i_{a}}_{max} \rangle$	$200\,\text{A}$
f_{S_3}	$\sim 1\,\text{Hz}$	i_{S_3}	$2\,\text{kA}$

Table VI shows the main requirements of the devices when the power converter is implemented using only Structure 1 and Structure 2. In this case, Structure 1 is used to reduce the rise and fall times, while Structure 2 is operated in switched mode to obtain the required accuracy in the pulse flat-top. Although the use of this topology allows to obtain a free-transient response pulse, it must be noted that the high switching frequency and current required (f_{S_3}, i_{S_3}) does not permit the use of currently available standard devices.

TABLE VI: Full-scale parameters without compensation structure.

C_H	$> 2\,\text{mF}$	V_{CH}	$2200\,\text{V}$
C_L	$> 5\,\text{mF}$	V_{CL}	$650\,\text{V}$
f_{S_3}	$70 - 30\,\text{kHz}$	i_{S_3}	$2\,\text{kA}$

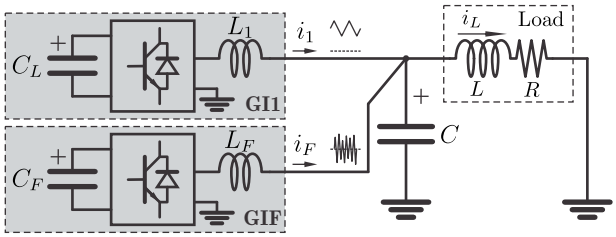

Fig. 7: Simplified scheme of the CSR-based topology during the flat-top.

This power supply can also be implemented using the topology presented in [20], which is named Current Source Regulation (CSR). Similarly to the topology presented in [19] and to the one proposed in the present work, this topology makes use of a high voltage structure in order to produce the high current slopes required to meet the rise and fall times. Then, since all topologies are designed to meet the same pulse characteristics, the required high voltage capacitor and semiconductor devices involved in this structure have similar ratings. In this sense, the main differences between the CSR-based strategy and the proposed topology arise from the active structures during the flat-top. Fig. 7 depicts a simplified scheme of the CSR strategy during this stage, where $GI1$ and GIF are the two current controlled structures and C is an interconnection capacitor used to avoid posible overvoltages. $GI1$ is a high current medium voltage structure used to achieve a moderate precision, and GIF is a low current high frequency structure used to achieve the required precision. Table VII lists the parameters for the power converter when using this strategy.

TABLE VII: Full-scale parameters for the topology based on CSR.

L_1	$500\,\mu\text{H}$	L_F	$50\,\mu\text{H}$
C_H	$> 2\,\text{mF}$	V_{CH}	$3300\,\text{V}$
C_L	$> 35\,\text{mF}$	V_{CL}	$600\,\text{V}$
C_F	$> 10\,\text{mF}$	V_{CF}	$600\,\text{V}$
f_{i1}	$10\,\text{kHz}$	i_1	$2\,\text{kA}$
f_{iF}	$100\,\text{kHz}$	i_F	$60\,\text{A}$

Fig. 8 compares the current and frequency values for the active structures during the flat-top stage of both, the proposed topology and the topology based on CSR. In the latter, the regulation structure $GI1$ must handle the full load current with demanding operational conditions ($2\,\text{kA}$, $600\,\text{V}$, $10\,\text{kHz}$). Concerning GIF structure, it achieves the precision requirements by operating with $60\,\text{A}$, $600\,\text{V}$, $100\,\text{kHz}$. Consequently, the strong stress produced on these components, especially the ones associated to structure GI1, could imply a limitation when using this regulation strategy for higher precision applications. On the other hand, the proposed topology reduces the amount of switching structures, since the devices that should handle the full load current are only switched at the beginning and at the end of the pulse. As for the structure responsible of the load current precision, its operation at reduced voltage values ($80\,\text{V}$) allows switching the devices in this stage at

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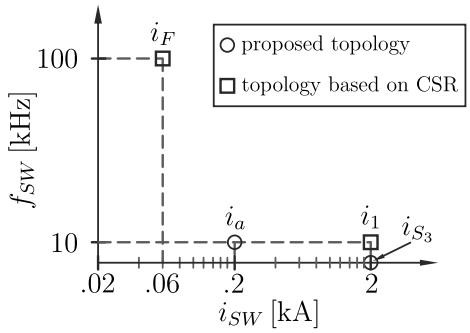

Fig. 8: Switching frequency comparison.

lower frequencies (10 kHz).

Furthermore, the existence of transient responses during structures interconnection in [20], demands the generation of longer flat-top durations, and consequently, it produces a reduction in efficiency. In order to compute the improvement provided by the proposed topology in this case, the energy dissipated on the load as a function of the flat-top duration is calculated. Fig. 9 depicts the ratio between the energy dissipated for the proposed structure, E_s, and the energy dissipated by the converter presented in [20], E_p, where the reported settling time of 200μs is used for its calculus. It should be noted that the proposed strategy requires less energy in the whole range of t_{ft}; this feature becomes more relevant as the flat-top time is reduced. For instance, for a flat-top duration of 2 ms, the required energy is 90% of the one required by the CSR-based strategy, while for flat-top times of 200 μs the improvement amounts to 50%. This does not only imply a reduction in the necessary space for installation but also in the required cooling system, which has a direct impact on the overall cost of the system.

IV. Experimental results

Experimental tests have been carried out on a low-scale laboratory prototype, $I_{REF\,max} = 65$ A. The aim of these tests is to validate the design equations and to verify the feasibility of the proposed control scheme. In this prototype, the current and voltages values are scaled down to laboratory levels. Even though this downscaling would allow to operate the prototype at higher frequencies than those indicated in Table V, the switching frequencies, pulse times, precision and load parameter are adopted as in the full-scale design so as to have the same system dynamics (Table IV). The generation of a current pulse of $I_{REF} = 65$ A and $t_r = 1$ ms defines $V_{CL} = 27.4$ V and $V_{CH} = 96.3$ V.

TABLE VIII: Laboratory prototype parameters.

L_1	100 μH	R_1	15 mΩ
C_H	5 mF	V_{CH}	100 V
C_L	90 mF	V_{CL}	30 V
C_B	10 mF	V_{CB}	10 V
f_{max}	10 kHz	$\langle \hat{i_{a\,max}} \rangle$	10A

Table VIII lists the selected values and operating ratings for the main passive components.

Fig. 10 shows the load current and voltage. It can be noticed that $t_r = 1$ ms, $t_{ft} = 2$ ms, and $t_f = 0.74$ ms lie within specifications. Concerning the load voltage, it varies during rise and fall times due to the discharge and charge of C_H, respectively. The difference between times t_r and t_f is explained by the fact that, in the rise time, the voltage drops associated to the resistive elements, $i_L(R + R_1)$, are opposite to the voltage on C_H; while in the fall time, such voltage drops favour the inductors discharge. The variation on the duty cycle in the flat-top load voltage to compensate the discharge of C_L can also be noted.

A detail of the load current during flat-top is illustrated in Fig. 11. It can be observed that i_L lies within the precision bands due to the use of a fixed-band hysteresis controller. In addition, it can be noted that the transition in the structures interconnection is performed without a transient response. Additionally, a mean switching frequency of 11.5 kHz is measured, which is consistent with the adopted one.

Fig. 12 shows the H-bridge current. It can be observed that the design condition of equal maximum positive and negative current value is met. Furthermore, the parabolic shape of i_a due to the linear voltage applied on L_1 can also be observed.

Voltages in C_H and C_L are shown in Fig. 13. It can be observed that the connection and disconnection of the structures produce step-like voltage variations due to the equivalent series resistance, ESR, inherent to each capacitor. Voltage v_{CL} presents a linear variation during flat-top, from 27.2 V to

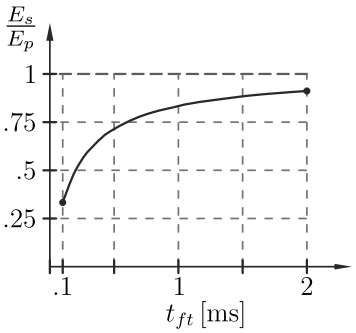

Fig. 9: Comparison of the dissipated energy on the load.

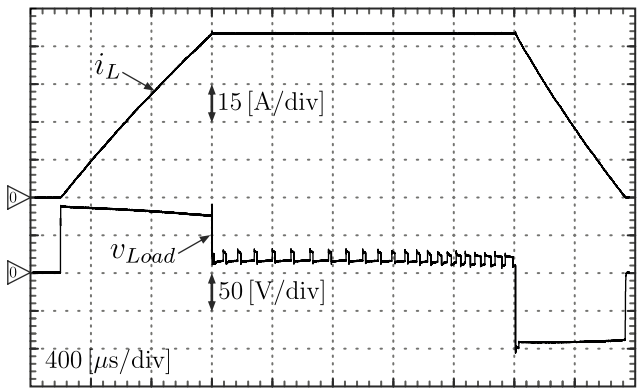

Fig. 10: Experimental results. Load current and voltage.

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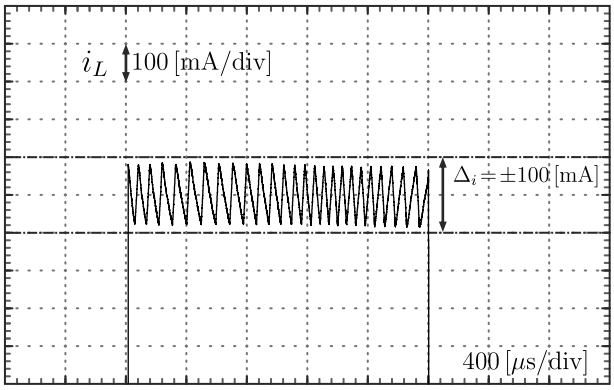

Fig. 11: Experimental results. Detail of load current in the flat-top.

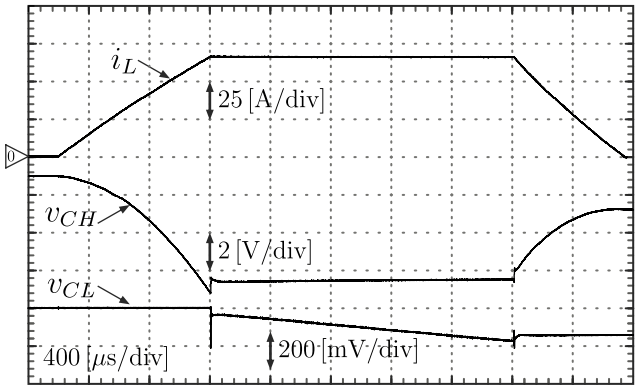

Fig. 13: Experimental results. Load current, high and low voltage DC bus.

25.8 V. As for v_{CH}, it varies during rise and fall times, while it remains constant during the flat-top due to the disconnection of Structure 1 in this stage. Evaluating (21), a final voltage of 95 V is obtained on C_H, while the measured voltage is 94.6 V. This represents an efficiency of 96.5% leading to a lower power rating for the capacitor charger required to restore the energy of C_H between pulses.

V. Conclusion

A topology for a current pulsed source based on a multiple structure scheme suitable for pulsed septum applications is presented. The proposed topology employs a compensation structure in series with the load in order to maintain the flat-top load current within the precision bands. This structure uses an H-bridge converter in parallel with an auxiliary inductor. Even though the use of a series compensation implies operating this structure at full load current, this circuit configuration allows to handle most of the load current on the auxiliary inductor, leading to a switch-mode structure with lower operating current and, consequently, to the use of standard semiconductor devices. Furthermore, since the devices that handle the full load current are switched at a lower frequency, on the order of the pulse repetition, higher current pulses could be obtained. Additionally, the use of a series compensation structure leads to a first-order circuit, which allows to have an oscillation-free structure interconnection. This feature avoids the generation of flat-top durations longer than the specified one, decreasing both the power losses on the load and the requirements associated to the low voltage capacitor bank, which has an impact on the volume and cost of the overall system. Moreover, the energy recovery of the topology allows to alleviate the requirements on the capacitor charger unit of the high voltage capacitor bank. The experimental results via a laboratory prototype validate the design equations and the ability of the proposal to generate a current pulse according to specifications, which would allow the use of the proposed topology in high precision applications.

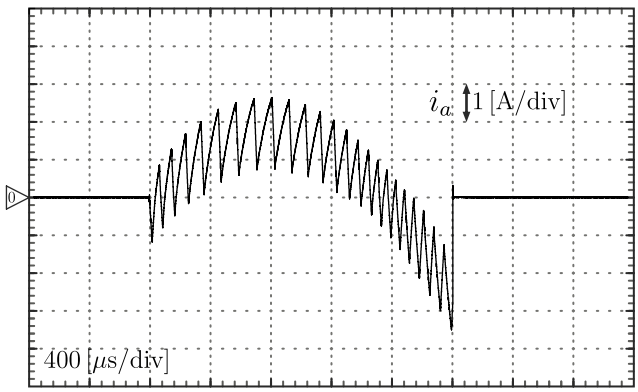

Fig. 12: Experimental results. H-bridge current.

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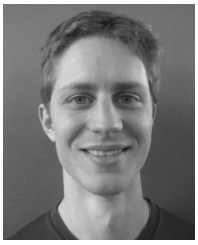

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