Design and Experimental Evaluation of a Time-Interleaved ADC Calibration Algorithm for Application in High-Speed Communication Systems

Benjamín T. Reyes, Raúl M. Sanchez, Ariel L. Pola, and Mario R. Hueda

***Abstract*—In this work we investigate a new background calibration technique to compensate sampling phase errors in time-interleaved analog-to-digital-converters (TI-ADCs). Timing mismatches in TI-ADC degrade significantly the performance of ultra-high-speed digital transceivers. Unlike previous proposals, the calibration technique used here optimizes a metric directly related to the performance of the communication system. Estimation of gradient of the mean-squared-error (MSE) at the slicer with respect to the sampling phases of each interleave, are computed to minimize the time errors of the TI-ADC by controlling programmable analog time delay-cells. Since (*i*) dedicated digital signal processing (DSP) such as cross-correlations or digital filtering of the received samples are not required, and (*ii*) metrics such as MSE are available in most commercial transceivers, the implementation is reduced to a low speed state-machine. The technique is verified experimentally by using a programmable logic-based platform with a 2 GS/s 6-bit TI-ADC. The latter has been fabricated in 0.13μm CMOS process, and it provides flexible sampling phase control capabilities. Experimental results show that the signal-to-noise ratio penalty of a digital BPSK receiver caused by sampling time errors in TI-ADC, can be reduced from 1 dB to less than 0.1 dB at a bit-error-rate of 10^{-6}.**

***Index Terms*—TI-ADC, time-error calibration, FPGA, fractional-spaced equalizer.**

I. Introduction

TIME-INTERLEAVED analog-to-digital-converter (TI-ADC) [1] is the most-used architecture in ultra high-speed digital communication systems. A TI-ADC uses M single converters (or *channels*) that operate in a parallel fashion at frequency $1/T_{ch}$ but with different sampling phases in order to achieve an overall sampling rate of $F_s = M/T_{ch}$ (see Fig. 1). It is well-known that TI-ADCs are sensitive to mismatches of DC offset, gain, and sampling phase among the channels (e.g., see [2] and references therein). Sampling-time errors are more difficult to detect and compensate than the DC offset and gain mismatches.

Numerous sampling-time error calibration algorithms have been reported in the literature [2]–[10]. These techniques are classified according to their (*a*) *detection domain* (i.e., digital or analog), (*b*) *calibration domain* (i.e., digital or analog correction), and (*c*) *run-mode* method (e.g., background or foreground) [11]. Recently, *mixed-signal* calibration techniques using *digital detection* and *analog correction* have received special attention for applications in ultra-high speed optical/wireline communication systems [5], [6], [12]. In this scheme, the analog correction is based on programmable delay-cells in the clock buffers of each sampling phase [4]–[8], [12], [13]. These delay-cells can be applied at high-speed clock rates with relative low power consumption compared to the alternative of a digital compensation of the output data with parallel interpolation filters [9], [10]. The *digital domain* time error detection, is preferred over analog circuits because it is more flexible and allows a simple adjust of coefficients when it is required. The detection techniques previously proposed for *mixed-signal* schemes are based on operations like cross-correlation, derivation, or multiplications between the interleaved channel outputs that are then filtered to generate an error signal with some proportionality to the time mismatch. Some of these techniques do the operations directly between the parallel ADC outputs [4], [5], [7] or use an extra ADC channel as a reference [6], [8], [13]. The common requirement for the mentioned techniques is the extra digital logic for the arithmetic operations directly in the input signal path at high-speed rates. Some of the proposals also demand specific input signal conditions for convergence like

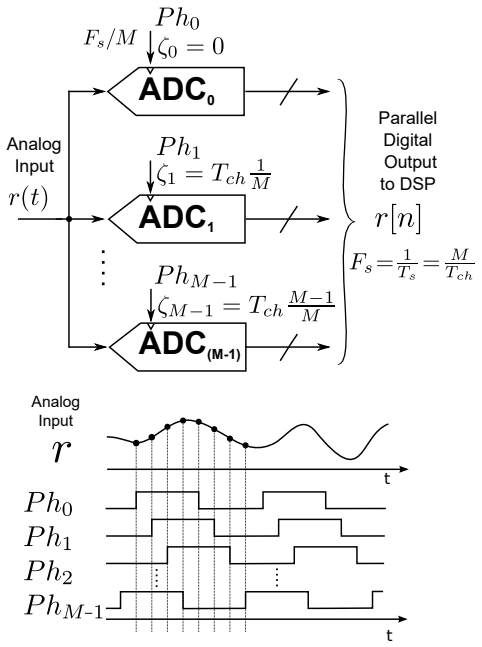

Figure 1. Time-interleaved A/D converter concept [1].

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low relative bandwidth [4] or non synchronous sampling with the input baud rate [5]–[7].

This work investigates a novel mixed-signal calibration scheme designed to compensate sampling time errors of TI-ADCs in multigigabit per second transceivers. The key feature of the new algorithm is that the TI-ADC clock phases are adjusted in a background run-mode by measuring a global performance parameter of the digital receiver. In particular, the technique exploits information available at the digital signal processing (DSP) based receiver such as the *mean squared error* (MSE) at the slicer or the *bit-error-rate* (BER), in order to adjust properly the clock phases of the interleaves [14]. We focus our study on the performance of a receiver with an adaptive digital *fractional-spaced-equalizer* (FSE) [15].

Performance evaluation of most of the previous sampling phase TI-ADC calibration algorithms has been carried out by using computer simulations [2], [9], [14]. Unfortunately, long computer simulation run time is required to adequately evaluate the performance of the different algorithms used in DSP-based communication systems. Hardware emulation platforms can speed-up the testing and validation process. Field programmable gate array (FPGA) chips are particularly suitable for emulation/implementation of digital communication systems. For example, the performance of forward error correction (FEC) blocks is commonly evaluated by using FPGA emulation as a result of the large amount of symbol required (e.g., $\sim 10^{15}$) to provide reliable estimation of the BER [16]. However, FPGA emulation is not limited to FEC blocks, and it could be useful for any other kind of algorithms. This is the case of the sampling-time error calibration algorithm for TI-ADC considered here. Since this technique is based on a relative *slow* averaging of squared error at the slicer, a proper performance evaluation would require to process a large amount of symbols. If numerous settings of the system under study must be tested, the simulation time could scale from days to weeks.

In this work we experimentally investigate the performance of the novel mixed-signal calibration algorithm previously mentioned. Towards this end, we implement an emulator of a digital communication system by using a FPGA platform. The system includes a simplified wireline DSP transceiver built upon an adaptive FSE running over a high-performance FPGA. The platform also includes an analog-front-end (AFE) based on a 6-bit 2-Giga-samples per seconds (GS/s) time-interleaved successive approximation register (SAR) ADC. The latter has been designed and fabricated in 0.13μm CMOS process and includes the sampling phase calibration capability required to evaluate the proposed algorithm [17]. The developed platform is able to process an oversampled DSP-receiver with a T/2-FSE at a transmission rate of 1 Giga-bauds (GBd). Experimental results show an excellent performance of the mixed-signal calibration algorithm. We also demonstrate that the algorithm requires very low complexity in terms of digital logic and negligible power consumption. We emphasize that the proposed calibration technique can operate in a background mode in order to speed up the start-up time of the system (i.e. no time required for off-line calibration process), and to track time delay changes due to voltage or temperature variations during the normal operation of the transceiver. These features make the calibration scheme a good candidate to be considered in next-generation high-speed transceivers such as 400 Gb/s coherent optical receivers and back-plane transceivers [18].

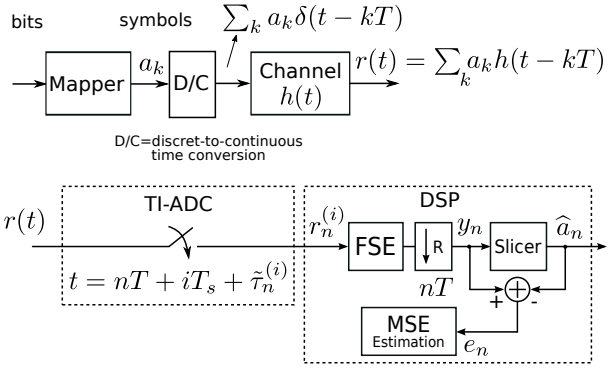


Figure 2. System model.

The rest of this paper is organized as follows. The impact of sampling time error in a digital receiver is discussed in Section II. Section III describes the calibration algorithm. Section IV presents the TI-ADC test-chip and the implemented transceiver. Experimental performance results of the transceiver and TI-ADC calibration are presented and discussed in Section V. Finally, concluding remarks are drawn in Section VI.

II. Impact of Sampling Time Errors of TI-ADC on DSP-based Communication Systems

We analyze the impact of sampling phase errors in TI-ADC on the performance of a typical digital communication system with an adaptive FSE-based receiver. The latter is widely used in commercial transceivers because its performance is independent of the sampling phase [15].

Let a_k and $h(t)$ be the transmitted symbols and the impulse response of the channel, respectively. The noisy-free received signal can be expressed as

$$r(t) = \sum_k a_k h(t - kT), \tag{1}$$

where $1/T$ is the symbol rate. Let $R = T/T_s$ be the integer oversampling factor used by the FSE (e.g., $R = 2$) (see Fig. 2). Based on the polyphase filter representation of the oversampled channel response, the received samples at the output of the TI-ADC with ideal sampling phase result in

$$\begin{aligned} r_n^{(i)} &= r(nT + iT_s) \\ &= \sum_k a_k h(nT + iT_s - kT) \\ &= \sum_k a_k h_{n-k}^{(i)}, \quad i = 0, 1, ..., R-1, \end{aligned} \tag{2}$$

where $h_m^{(i)} = h^{(i)}(mT)$ with $h^{(i)}(t) = h(t + iT_s)$. Let τ be a certain sampling phase error. Expanding $h^{(i)}(t+\tau)$ in Taylor series up to second order terms, we get

$$h^{(i)}(t+\tau) \approx h^{(i)}(t) + h'^{(i)}(t)\tau + \frac{1}{2}h''^{(i)}(t)\tau^2. \tag{3}$$

Let τ_k with $k \in \{0, 1, ..., M-1\}$ be the sampling phase error of the k-th single converter. Since the TI-ADC operates in a parallel fashion at frequency $1/T_{ch}$ to achieve an overall sampling rate of $1/T_s = M/T_{ch}$ (see Fig. 1), we verify that the same sampling phase error will appear every M samples of the received signal at frequency $1/T_s$[1]. Therefore, the effective sampling instant in the presence of sampling phase errors of the TI-ADC can be expressed as

$$mT_s + \tilde{\tau}_m, \tag{4}$$

where $\tilde{\tau}_m$ is the periodic sequence with period M defined by

$$\tilde{\tau}_m = \{\cdots \tau_0, \tau_1, \cdots, \tau_{M-1}, \tau_0, \tau_1 \cdots\}. \tag{5}$$

The samples at the output of a TI-ADC with sampling time error result

$$\begin{aligned} r_n^{(i)} &= r(nT + iT_s + \tilde{\tau}_n^{(i)}) \\ &= \sum_k a_k h(nT + iT_s + \tilde{\tau}_n^{(i)} - kT), \end{aligned} \tag{6}$$

where $\tilde{\tau}_n^{(i)} = \tilde{\tau}_{nR+i}$ with $i = 0, 1, ..., R-1$. Replacing (3) in (6), it is possible to obtain

$$r_n^{(i)} \approx \sum_k a_k h_{n-k}^{(i)} + e_n^{(i)}, \tag{7}$$

where

$$e_n^{(i)} = \tilde{\tau}_n^{(i)} \sum_k a_k h_{n-k}^{\prime(i)} + \frac{1}{2}\left(\tilde{\tau}_n^{(i)}\right)^2 \sum_k a_k h_{n-k}^{\prime\prime(i)}. \tag{8}$$

The impact of $e_n^{(i)}$ on the performance of an FSE-based receiver shall depend on the number of single ADCs, M.

A. Case 1: Single ADC ($M = 1$)

Assume a *single* ADC (i.e., $M = 1$). In this case, $\tilde{\tau}_n^{(i)} = \tau_0 \ \forall \ n, i$, therefore

$$e_n^{(i)} = \tau_0 \sum_k a_k h_{n-k}^{\prime(i)} + \frac{1}{2}\tau_0^2 \sum_k a_k h_{n-k}^{\prime\prime(i)}. \tag{9}$$

Replacing (9) in (7) note that the received samples can be rewritten as

$$r_n^{(i)} \approx \sum_k a_k \tilde{h}_{n-k}^{(i)}, \tag{10}$$

where

$$\begin{aligned} \tilde{h}_m^{(i)} &= h_m^{(i)} + \tau_0 h_m^{\prime(i)} + \frac{1}{2}\tau_0^2 h_m^{\prime\prime(i)} \\ &\approx h(mT + iT_s + \tau_0). \end{aligned} \tag{11}$$

From eqs. (10) and (11) we observe that the model reduces to a *single* ADC with an arbitrary sampling phase, τ_0. On the other hand, with a proper oversampling factor R (e.g., $R = 2$), aliasing can be avoided at the input of FSE [15]. Hence, any constant sampling phase error τ_0 of a single ADC can be easily compensated by an adaptive FSE without penalty (i.e., FSE acts as an interpolator filter). Thus, we conclude that the impact of term (8) on the performance of the FSE-based receiver with $M = 1$ will be negligible.

[1]Without loss of generality, we assume that sampling phase errors τ_k are time invariant.

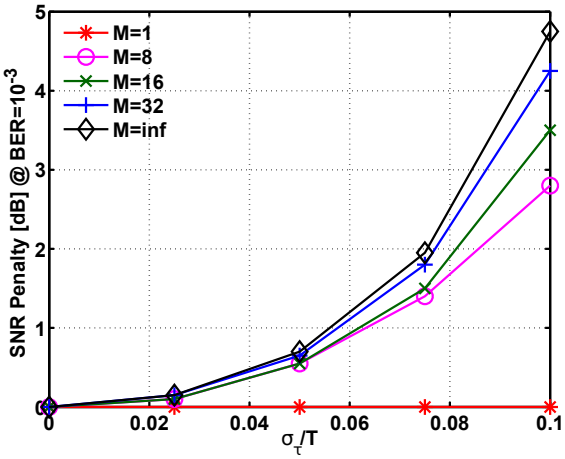


Figure 3. SNR penalty at BER=10^{-3} versus σ_τ/T for TI-ADC with different number of single ADCs (M). Modulation scheme: 16-QAM. Adaptive FSE with 32 taps and $R = 2$.

B. Case 2: TI-ADC with $M \gg 1$

Consider a TI-ADC with $M \gg 1$. In this case, components of the sampling phase error sequence $\tilde{\tau}_m$ can be assumed independent and identically distributed (i.i.d) zero-mean random variables with variance σ_τ^2. Then, sequence (8) can be treated as white noise with variance $\sigma_{e(i)}^2$ given by

$$\sigma_{e(i)}^2 \approx \mathcal{E}_a \sigma_\tau^2 \sum_k |h_k^{\prime(i)}|^2, \tag{12}$$

where $\mathcal{E}_a = E\{|a_k|^2\}^2$. From (12) we infer that a *noise floor* will be caused by time phase errors in TI-ADCs. We emphasize that the impact of this noise component on the receiver performance shall be exacerbated in the presence of high-order modulation schemes.

C. Discussion

Fig. 3 shows the penalty of the *signal-to-noise-ratio* (SNR) at a BER of 10^{-3} as a function of σ_τ/T derived from computer simulations. We consider 16-quadrature-amplitude-modulation (16-QAM) over a non-dispersive channel with additive white Gaussian noise. A raised cosine filter with a rolloff factor of 20% is used. Time sampling errors τ_m are assumed i.i.d random variables with $\tau_m \in \{\pm\delta\}$. We analyze an adaptive FSE with 32 taps and $R = 2$. As expected, no performance degradation is observed when a single ADC is used ($M = 1$). We also verify that the degradation increases as the value of M is increased. Taking into account that high-order modulation schemes such as 64-QAM are being considered for next-generation high-speed networks [18], we infer that the performance degradation caused by sampling time errors will be worse. Therefore, the design and implementation of new efficient algorithms for calibration of sampling time errors in ultra-high-speed TI-ADC becomes mandatory.

[2]In general, notice that the noise variance (12) depends on the polyphase filter index $i \in \{0, 1, ..., R-1\}$.

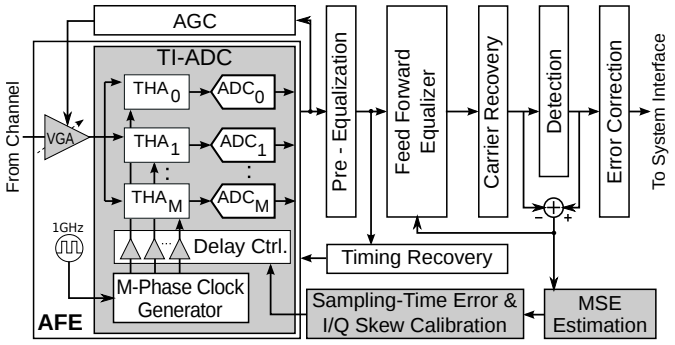


Figure 4. Simplified diagram of a digital receiver for optical/wireline applications with proposed mixed-signal calibration technique.

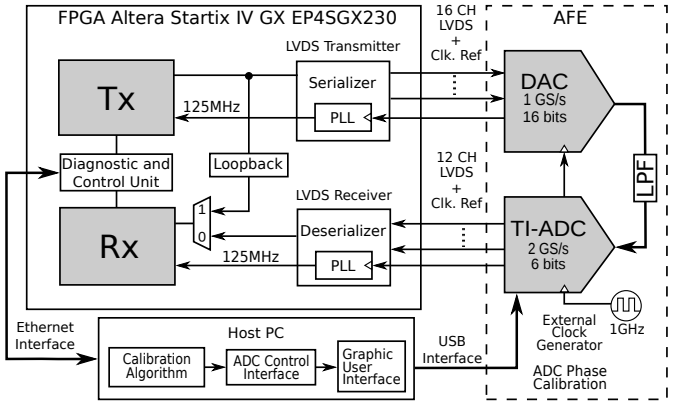


Figure 5. Simplified block diagram of the implemented transceiver.

III. Mixed-Signal Calibration of Sampling Time Error of TI-ADC

As shown in the previous section, the sampling time errors of TI-ADC significantly impact on the performance of DSP-based receivers. In these receivers, the estimation of BER is possible since powerful FEC codes are typically available in optical systems. Taking advantage of this fact, we have proposed in [14] a calibration technique designed to minimize the BER. In this work we consider a calibration approach designed to minimize the MSE at the slicer after the equalization block (i.e., before the channel decoder). Note that this approach (denoted as *MMSE*) avoids the use of information from the FEC decoder. Fig. 4 shows an example of the implementation of the proposed mixed-signal calibration technique.

A. MMSE Calibration Algorithm

The algorithm technique considers an AFE architecture with M ADC channels interleaved and one programmable delay cell controlling each clock phase (see Fig. 4). The sampling phase of the m-th channel can be expressed as

$$\zeta_m = \frac{m}{M}T_{ch} + \tau_m + \hat{\tau}_m, \quad m = 0, 1, ..., M-1, \qquad (13)$$

where, T_{ch} is the channel sampling period (i.e. $T_{ch} = T_s/M$), τ_m is the sampling time error of the TI-ADC and $\hat{\tau}_m$ is the phase provided by the programmable delay-cells, which is controlled by the DSP-based receiver. In an ideal TI-ADC, notice that $\tau_m = \hat{\tau}_m = 0\ \forall m$.

Let $\mathcal{C}$ be the real cost function to be minimized (i.e., MSE). Notice that this function depends on $(\zeta_0, \zeta_1, ..., \zeta_{M-1})$. Then, the *gradient algorithm* can be used to iteratively adjust the sampling phase in order to minimize $\mathcal{C}$, that is,

$$\vec{\zeta}(n+1) = \vec{\zeta}(n) - \mu \nabla_{\vec{\zeta}(n)}\mathcal{C}, \qquad (14)$$

where $\vec{\zeta}(n)$ is the sampling phase vector at the n-th iteration given by,

$$\vec{\zeta}(n) = [\zeta_0(n), \zeta_1(n), ..., \zeta_{M-1}(n)]^T \qquad (15)$$

while,

$$\nabla_{\vec{\zeta}}\mathcal{C} = \left[\frac{\partial \mathcal{C}(\zeta_0, ..., \zeta_{M-1})}{\partial \zeta_0}, ..., \frac{\partial \mathcal{C}(\zeta_0, ..., \zeta_{M-1})}{\partial \zeta_{M-1}}\right]^T \qquad (16)$$

is the gradient of the cost function $\mathcal{C}(.)$, while μ is the step-size (symbol $[.]^T$ denotes transpose). The MSE value depends on multiple factors such as noise, channel dispersion, mismatches of the TI-ADC, etc. Therefore, it is difficult to derive a simple closed form expression of the MSE gradient as a function of the sampling phase of TI-ADC. This fact precludes the use of a well known minimization technique such as (14). Consequently, we use here the following iterative method to adjust the ADC sampling phases:

1: Set to zero the M sampling phases provided by the programmable delay-cells (i.e., $\hat{\tau}_m(0) = 0,\ m \in [0, 1, ..., M-1]$).
2: Select one ADC phase (e.g., $\zeta_k(n) = \frac{k}{M}T_{ch} + \tau_k + \hat{\tau}_k(n)$).
3: Estimate the initial cost function $\mathcal{C}$ (i.e., the MSE at the slicer of the receiver).
4: Move the sampling phase of the k-th ADC (i.e., $\zeta_k(n)$) in a *positive* direction, that is,

$$\hat{\tau}'_k = \hat{\tau}_k(n) + \mu_s, \qquad (17)$$

where μ_s the time step of the corresponding programmable time-delay cell (e.g., 1% of the baud period).
5: Re-estimate the cost function for the new sampling phase, $\mathcal{C}'$.
6: Adjust the sampling phase of the k-th ADC according to

$$\hat{\tau}_k(n+1) = \hat{\tau}_k(n) - \mu_s sgn\left(\mathcal{C}' - \mathcal{C}\right), \qquad (18)$$

where $sgn(.)$ is the *signum* function.
7: Select a new ADC phase and repeat steps 3 through 6. In order to select the ADC phase, a simple circular sequence can be set (e.g., for $M = 8$, the order results $k = 0, 1, 2, .., 7, 0, 1, ...$).
8: After all ADCs have been adjusted, repeat steps 3 to 6.

Let y_n and $\hat{a}_n$ be the signal at the slicer input and the detected symbol, respectively. The MSE (i.e., the cost function) can be recursively estimated as follows:

$$MSE(n+1) = \alpha|y_n - \hat{a}_n|^2 + (1-\alpha)MSE(n), \qquad (19)$$

where $\alpha < 1$. In order to improve the accuracy of the MSE estimation, factor α must be very small. Thus, a proper evaluation of the algorithm by using computer simulation would require a very long run time. Therefore, in this work

the performance of the described algorithm shall be evaluated experimentally by using an FPGA-based platform (see Section IV).

It is interesting to highlight that the error at the slicer is required by the LMS algorithm to implement decision-directed adaptive equalization. This error is used to estimate the MSE, which is necessary to implement out calibration technique. Fortunately, MSE estimator is already available in most commercial transceivers [19]. Therefore, the implementation complexity of the proposed mixed-signal calibration technique is reduced to that required by the algorithm described before. The latter can be implemented by using a low speed state-machine (SM)[3].

IV. FPGA-Platform for Evaluation of the TI-ADC Calibration Algorithm

We experimentally evaluate the performance of the mixed-signal calibration algorithm described in the previous section. Accordingly, we implement an emulator of a digital communication system by using an FPGA platform. The system includes a simplified wireline DSP transceiver built upon an adaptive FSE. Fig. 5 presents the basic diagram of the emulated transceiver proposed. The system is composed of AFE, DSP and physical channel (electrical filter). Digital blocks (i.e. transmitter/receiver) and an embedded processor are implemented in the FPGA. The transceiver operates at a nominal symbol rate of 1 Gb/s ($T = 1\ ns$) and can emulate different scenarios of SNR (e.g. from 4 dB to 30 dB). In next subsections the transceiver implementation is detailed.

A. Analog-Front-End

The AFE[4] is comprised of a commercial 1 GS/s 16-bit DAC board [20] and a prototype 2 GS/s 6-bit TI-ADC. The DAC is interfaced to the FPGA via 16 low-voltage-differential-signaling (LVDS) channels (1 Gb/s each). The TI-ADC is connected to the FPGA via 12 LVDS channels at 1 Gb/s each. The DAC and ADC boards are interconnected in the analog domain by a *communication channel* that is based on an electrical low-pass filters (LPF) like [21]. The channel bandwidth (i.e. LPF) can be changed according to the required dispersion scenario. In the following subsection the TI-ADC test chip designed for this platform is detailed.

1) High Speed Time-Interleaved ADC: It was specially designed and fabricated in a 0.13 μm CMOS process for this experimental mixed-signal calibration demonstration platform. For this purpose, the design comprises a hierarchical time-interleaved ADC architecture with eight interleaved track-and-hold amplifiers (THA) and sixteen 6-bit single SAR converters to achieve an overall high sampling rate such as 2 GHz (see Fig. 6). Each THA is managed by a 50% duty cycle clock at frequency $F_{slice} = F_s/8 = 2\ \text{GHz}/8 = 250\ \text{MHz}$. After tracking phase, the THA output is re-sampled alternatively by one of the two SAR ADC included in each channel for signal

[3]Hard-logic or embedded firmware are typically used to implement SM in commercial CMOS transceivers.

[4]For simplicity, the group of analog and also mixed-signal blocks used in the front-end of digital transceivers are named as analog-front-end (AFE).

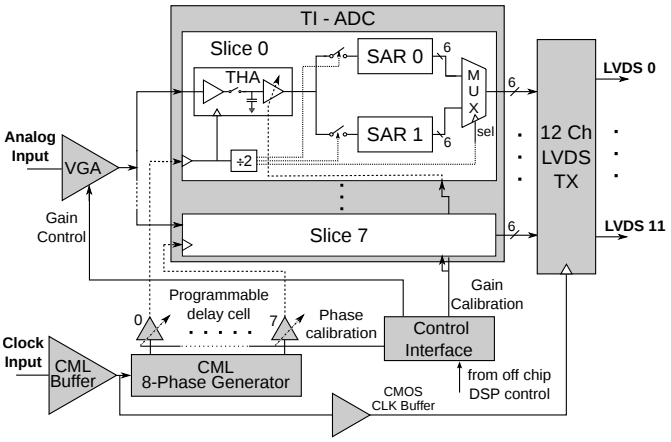


Figure 6. Time-interleaved ADC chip architecture.

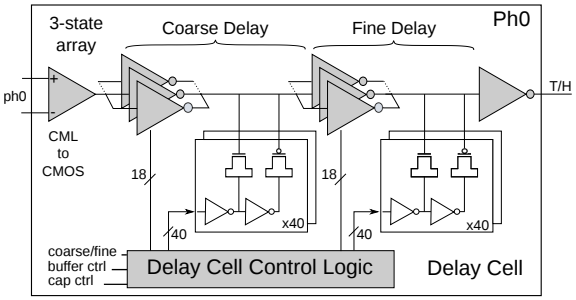


Figure 7. Programmable delay-cell (phase 0 cell only).

quantization. The THA and SARs are synchronized by a clock divider that generates two clock signals from THA clock with 25% duty cycle at $F_{SAR} = F_{slice}/2 = 125\ \text{MHz}$. The digital SAR ADC outputs (16 channels $\times$ 6 bits) are serialized and sent to the 12 LVDS channels interface. Note that, unlike most of the giga-sample ADCs reported [5]–[7], in our design the full data rate (12 Gbps) is sent off-chip without decimation so that it can be used for the digital receiver implementation.

The most interesting aspect of the fabricated TI-ADC for this work is the implementation of a very wide time delay control in each clock phase that allows for the experimental demonstration of the calibration technique. Fig. 7 shows the delay cell circuit used between the multiple phase generator and the THAs. These cells are able to set a time delay (T_d) to adjust the relative sampling time between the clock phases. This design considers a *fine* delay circuit and a *coarse* delay circuit. It also includes a main control of the total range of both, fine and coarse delay control, to adjust the relative control phase at any operating frequency.

The fine delay circuit is used to adjust a very small sampling time mismatch. The maximum *fine* delay control range is $T_{d,max} = \pm 0.03 T_s$, where T_s is the overall sampling period ($T_s = 1/F_s$). Then, the time delay range is divided into 40 time delay steps, that is $T_{d,step} = 0.0015 T_s$. On the other hand, the *coarse* delay control permits a wide phase control such as the one required in emulation of a relative large sampling mismatch scenario (e.g., high-speed TI-ADC in optical receivers). Therefore, the coarse delay circuit is implemented

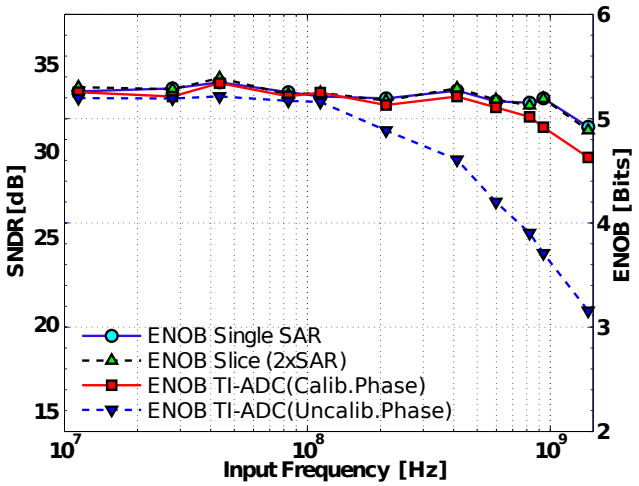


Figure 8. SNDR and ENOB vs. input frequency.

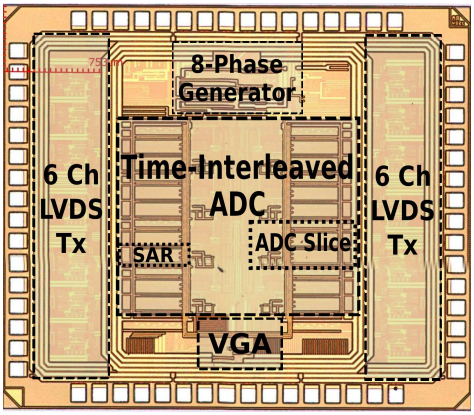


Figure 9. TI-ADC chip micro-photograph. Size: 3.5mm×3mm

with a maximum delay range of $T_{d,max} = \pm 0.3T_s$ and with $T_{d,step} = 0.015T_s$. The fine and coarse delay circuits are based on shunt-capacitor technique. Hence, each buffer is loaded by a 40 equal sized MOS capacitor array (MOScap) that is thermometrically switched [7][5].

The performance of TI-ADC in terms of effective-number-of-bits (ENOB) and SNDR as a function of input frequency is plotted in Fig. 8. Note that only calibrating their clock phases we can achieve the maximum performance near *Nyquist* frequencies. Table I summarizes the measured performance, including power consumption and area of each block [17]. The fabricated chip is depicted in Fig. 9, and main blocks are highlighted (more details of the circuits design can be found in [17]).

B. DSP

The digital part of the transceiver is implemented on a high performance FPGA board [22]. Because of the high speed required and the clock limitations in FPGAs (< 200 MHz), the digital implementation of the transceiver is based on

[5]Note that fine and coarse delay control are daisy-chained but they are not designed to be controlled simultaneously because they have different applications.

Table I
PERFORMANCE SUMMARY OF PROTOTYPE CHIP.

	Single SAR	Full TI-ADC
Resolution [bits]	6	
V_{in} [$V_{pp-diff}$]	0.4	
Sampling Freq. [MHz]	12.5 to 125	200 to 2000
ERBW [GHz]	1	1
ENOB [bits]	5.2	4.92
DNL/INL [LSB]	0.21/0.52	0.16/0.49
Power Cons. [mW]	3.3	192
FOM [pJ/conv-step]	0.63	3.163
Active Area [mm2]	0.065	3.24
	Programmable Delay Cell	
Delay Adjust Mode	Nominal (F_s=2 GS/s)	Max. Delay ($F_s \ll$2 GS/s)
Fine Step [ps]	0.62	3.5
Fine Range [ps]	±12.4	±70
Coarse Step [ps]	7.15	15.25
Coarse Range [ps]	±143	±305
Power Cons. [mW]	3.3	1.1
	8-Phase Generator	
Operating Freq. [MHz]	200 to 2000	
Power Cons. [mW]	33	
	LVDS Transmitter	
Number of Channels	12 Data + 2 Sync. Clk.	
Data Rate / Channel	1 Gb/s (Max. 1.66 Gb/s)	
Power Cons. [mW]	260 mW (18.5 mW/Ch)	
Active Area [mm2]	2.1 mm^2 (0.084 mm^2/Ch)	
Supply Voltage	Core = 1.2 V / Tx + I/O = 2.5 V	
Technology	IBM 0.13μm CMOS	
Die Size	3.5mm x 3mm	
Package	QFN 64, 10mm x 10mm	

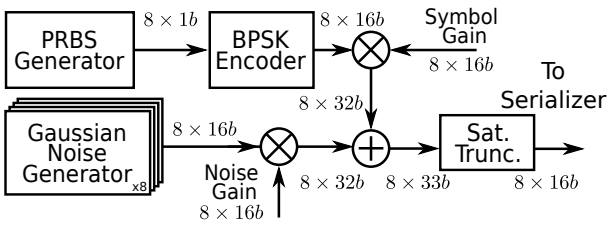


Figure 10. Digital transmitter diagram.

parallel architectures for both, the receiver and transmitter blocks. The transceiver achieves a nominal throughput of 1 Gb/s. The dedicated transceiver blocks and a general purpose microprocessor are fit in a single FPGA chip thanks to a careful hardware description design and digital architecture optimization. Finally, note that a fully digital loopback option (inner loopback) is included (see Fig. 5). It is used to test the DSP performance without considering the analog domain effects from AFE. Next, the digital architecture implementation is detailed.

1) Transmitter: The implemented digital transmitter is depicted in Fig. 10. It generates a pseudo-random binary sequence (PRBS) that is merged with an additive white Gaussian noise (AWGN) signal to define the required SNR. The PRBS sequence ($2^9 - 1$ symbols length) is implemented in a parallel architecture like [23] to achieve 1 Gb/s based on 125 MHz clock. On the lower branch of the transmitter, the noise signal is generated by implementing eight parallel instances of an AWGN IP block with different seeds [24]. The block includes

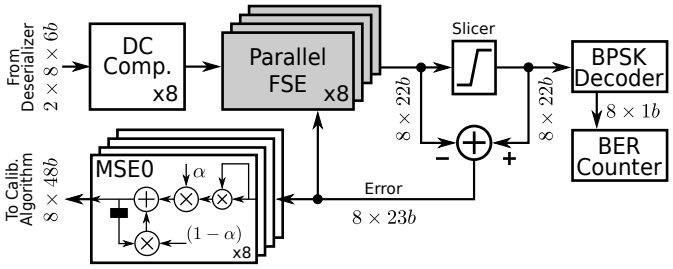


Figure 11. Digital receiver diagram.

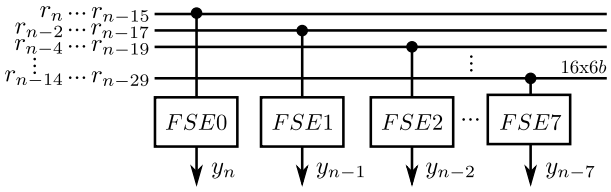


Figure 12. Parallel implementation of the FSE.

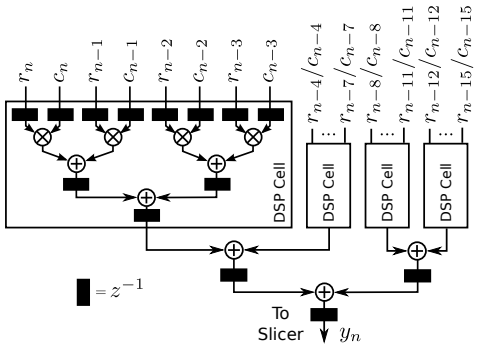


Figure 13. FSE implementation diagram using dedicated FPGA DSP cells.

independent 16-bit gain coefficients for both, signal and noise paths, that allows the user to set any required SNR value, with very high resolution and precision. The resulting output signal is then serialized, transmitted, and synthesized directly to the physical channel by the DAC board.

2) Receiver: The simplified diagram of digital receiver is shown in Fig. 11. The core of the receiver is an adaptive FSE filter. The FSE is implemented with a parallel architecture based on the new generation of coherent optical systems architecture [19]. The receiver input registers operate at a synchronous $T/2$ sampling rate (i.e. 2 GS/s) but the FSE clock is at the symbol rate T (1 GHz). Previous to the FSE inputs, a DC offset cancellation block is used to compensate for DC offset mismatch between the parallel ADCs channels. Note that other typical receiver blocks like carrier recovery and timing recovery are not included because architecture simplification was required to fit the full DSP into the FPGA chip and also because they are not required for calibration tests. At the output of the FSE and slicer blocks, the signal is decoded and sent to a bit-error counter. This last block includes a correlation algorithm for detection and synchronization of the known PRBS sequence and it is used for receiver performance BER tests.

The basic structure of the FSE architecture is shown in Fig. 12. It is based on [19], [25] proposals and it is formed by 8 parallel filters with 16-tap (coefficients) each. The equalizer is adapted by a least mean square algorithm (LMS) [15] and the adapting step factor can be externally set with different values to control the convergence speed. As many other parallel architectures, the trade-off between speed and complexity has to be considered. Unlike [19], [25], where a dedicated chip was used, this implementation was conducted in an FPGA. Due to the limited resources of the latter platform, a detailed study of the dedicated FPGA DSP cells was required in order to optimize the use of resources [26].

In Fig. 13, the detailed architecture of each parallel filter is shown. DSP cells are used to multiply each sample by the corresponding coefficient and to accumulate the partial result. The final result is implemented with logic elements through a parallel adder. With this topology, the amount of conventional logic resources required for multiplication/addition is drastically reduced and also the complexity of the routing is simplified.

The other relevant block for this platform is the MSE estimator. It provides the feedback signal required by the TI-ADC calibration algorithm. The MSE estimation is obtained by using a recursive filter as expressed in (19). The parallel architecture used for this recursive filter is based on [27]. The operation of this block is controlled externally, so that the coefficient α, reset signals and outputs can be controlled and monitored by the user via the control unit. As mentioned before, the latest generation optical transceivers already include a MSE estimator block, therefore no additional hardware is required for this function [18], [19].

The digital blocks were implemented using the Verilog hardware description language and properly verified at gate level simulations [26]. The functional verification was executed for each module individually as well as for their integration. For physical verification, the digital blocks were synthesized for the Stratix IV GX FPGA development kit from Altera [22]. The resource usage is detailed in Table II (see [28] for more details).

C. Diagnostic and Control Unit

The diagnostic and control unit (DCU) is used to configure and register variables of the transceiver block previously described. It is based on an embedded NIOS II processor that runs a real-time operating system (RTOS). The RTOS is used to generate a socket server which enables an Ethernet connection to the emulation platform. A client application was developed to communicate with the server to perform different operations such as controlling noise injection, modifying FSE adaption step, MSE logging, among others. Furthermore, a massive logging system with 16,384 words of 128 bits was implemented with dedicated memory blocks RAM (dual-port) of FPGA.

V. Experimental Results

On the basis of the transceiver implementation depicted in the previous section, we have arranged a fully experimental setup as shown in Fig. 14. The system is connected via

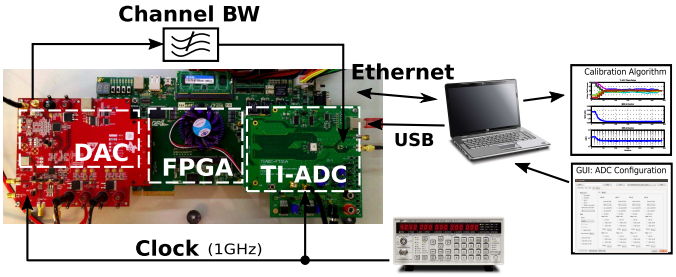


Figure 14. Experimental transceiver setup.

Table II
SYNTHESIS REPORT

Block	Comb. ALUTs	Registers	Memory Blocks		DSP Elements			
			M9K	M144K	18-bit	12x12	18x18	36x36
Receiver								
FSE	5684	8629	3	0	747	128	0	144
BER Counter	1386	560	0	0	0	0	0	0
MSE Estimation	612	438	1	0	52	0	8	9
Transmitter								
PRBS	568	80	0	0	0	0	0	0
GNG	3536	3622	20	0	48	0	32	0
Diagnostic and Control Unit								
NIOS System	9520	11539	815	2	4	0	0	1
Logger	379	577	3	15	0	0	0	0
Other	4343	4887	20	0	80	0	32	0
Total	26028	30332	862	17	931	128	72	154

USB and Ethernet to a computer for transceiver control and monitoring. Additionally, a graphical user interface (GUI) software was developed to configure the TI-ADC registers via a USB port. The first step with this setup is to test the transceiver performance measuring BER versus SNR curves. In Fig. 15 we present results for different operation conditions. We verify that the performance with the inner digital loopback (i.e., bypassing the DAC/ADC converters) agrees very well with the theoretical and simulated curves. When the AFE is used with a nondispersive channel and a calibrated TI-ADC (i.e., without mismatches), a low SNR penalty is observed as a result of the quantization and extra noise added by data converter chips. We also show the performance in the presence of a dispersive electrical channel with a bandwidth of 650 MHz. The time and the frequency responses of the electrical channel are depicted in Fig. 16. From Fig. 15 we verify that the FSE compensates efficiently most of the dispersion introduced by the channel[6]. We highlight that an imperfect equalization increases the MSE at the slicer due to the residual intersymbol interference. Nevertheless, the accuracy of the MSE estimation will be still satisfactory taking into account that sampling phase errors slowly vary with time. Finally, we add mismatches among the phases of the TI-ADC (e.g. up to $\pm 0.15T$ time mismatch, where $T = 1ns$ is the baud rate). In this case, a significant performance degradation can be verified.

A. Impact of sampling-time errors on the receiver

Fig. 17 depicts the ENOB and the SNR penalty as a function of the sampling-time mismatch among the interleaves

[6]The number of coefficients of the FSE is limited to 16 due to resource limitations in the FPGA.

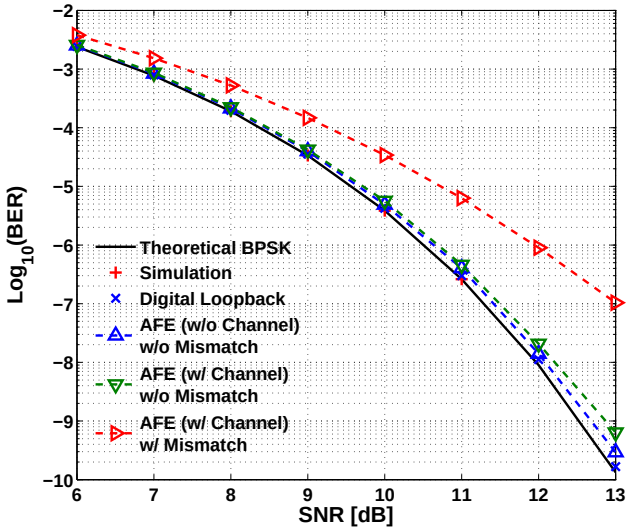
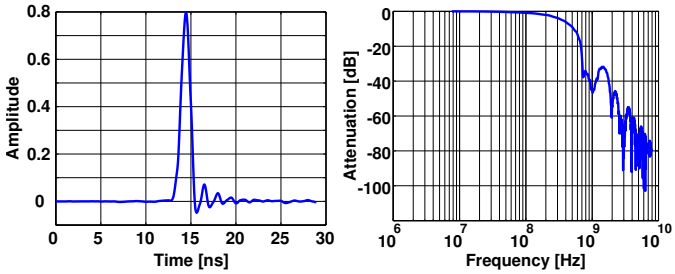


Figure 15. Receiver BER performance under different configurations.



(a) Impulse response. (b) Frequency Response

Figure 16. Electrical channel linear characterization: a) Impulse response, b) Frequency response.

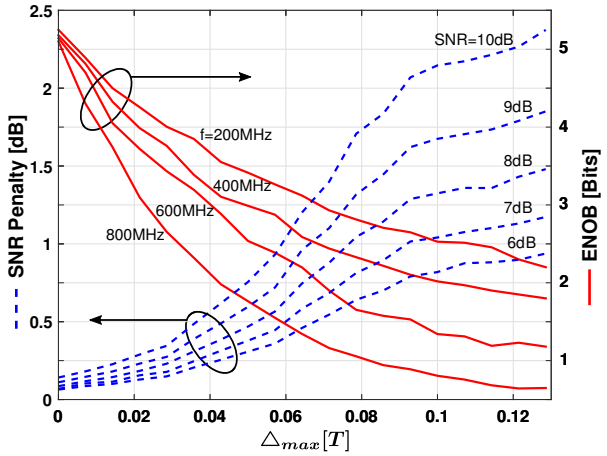


Figure 17. Measured performance versus sampling time error. *Dashed lines*: penalty of SNR for different values of the input SNR. *Solid lines*: TI-ADC ENOB for different input frequencies.

without any calibration. The penalty of SNR is obtained by comparison with the performance achieved with an *ideal* TI-ADC at different input SNRs (i.e., SNR= 6-10 dB). For this test, numerous sets of sampling-mismatches bounded by $\pm \triangle_{max} T$ were tested, and then the set that achieved the worst performance was selected. We verify that the maximum

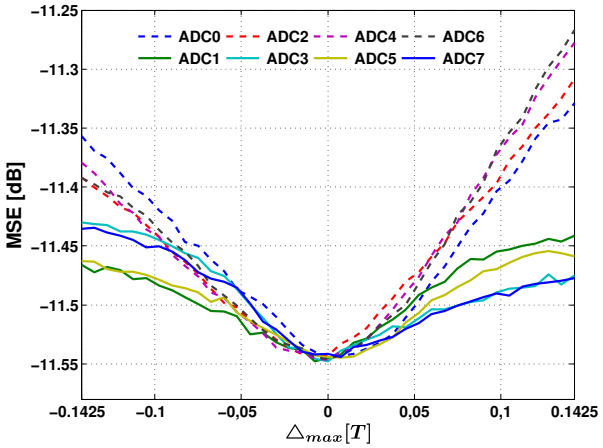
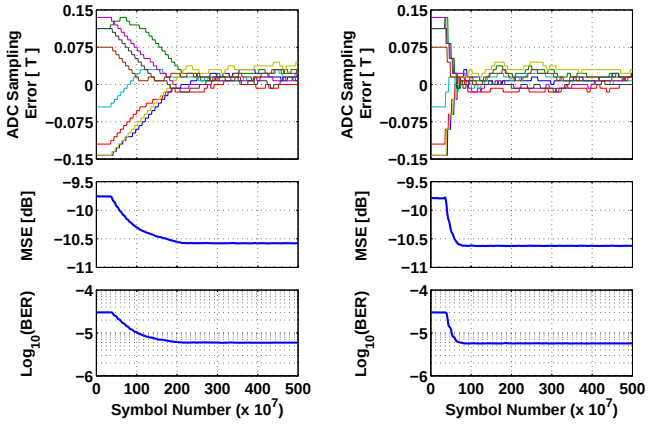


Figure 18. MSE at slicer as a function of individual phase errors.



(a) Constant time step. (b) Non-constant time step.

Figure 19. Calibration convergence and performance: (a) $\mu_s = 0.0075$T (constant), (b) $\mu_s = 0.03$T (initial) to $\mu_s = 0.0075$T (final). Input SNR=10 dB and $\alpha = 10^{-7}$.

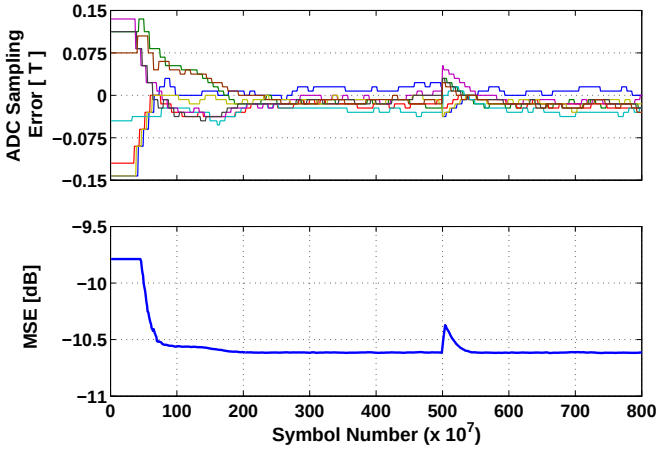


Figure 20. Example of the background operation with SNR=10 dB and $\alpha = 10^{-7}$.

sampling time error in the TI-ADC should be limited to $\sim \pm 0.02T$ in order to achieve an SNR penalty lower than 0.2 dB.

In Fig. 18, a measurement of MSE vs. single TI-ADC phases is presented. This test assumes that all the interleaved phases are ideal sampling except one of them that it is being shifted from negative to positive time values using the corresponding programmable delay cell. From these results, the first aspect that can be highlighted is that any shift from its ideal phase has some impact in the measured MSE (i.e. SNR at the slicer). The second relevant aspect, is that the phases have slightly different impact on the MSE. This can be explained because the A/D converter operates at a T/2 sampling rate so that the *odd* phases (i.e. *ADC1,ADC3,...,ADC7*) and *even* phases (i.e. *ADC0,ADC2,...,ADC6*) of TI-ADC are sampling synchronously at two different points of the received eye diagram. From Fig. 18, we conclude that the impact on the performance of the sampling errors for the *odd* phases will be different than the ones for the *even* phases in a T/2 FSE receiver.

B. Calibration Results

The sampling time error calibration results are presented here for different transceiver operating scenarios. First, let us analyze different algorithm convergence cases. In Fig. 19(a) we can appreciate a calibration case where a uniformly distributed mismatch is set in the TI-ADC. In this example we can see how the BER value and the MSE estimated at the slicer are improved drastically after the algorithm is turned on[7]. Then in Fig. 19(b) a similar setup case except for the algorithm time step (μ_s) is presented. Here, the μ_s starts with a value $4\times$ greater than used in case (a) and then it is progressively reduced to its original value. The advantage of the last implementation is that it allows a much faster convergence without affecting the final BER performance. In terms of speed, it can be noted that in Fig. 19(b) the algorithm requires a relative short time in considering the high symbol rate used in this platform. Furthermore, the algorithm would only take a very few milliseconds if it is implemented in a $>$100 Gb/s optical receiver.

Fig. 20 shows an example of the *background* operation with the proposed calibration technique. After the initial convergence, a disturbance in the clock phases is *artificially* generated by the FPGA-based platform at $\sim 500 \times 10^7$ symbols[8]. Note that an increase of the MSE is experienced when the disturbance is introduced. Then, the MSE is reduced as a result of the sampling phase correction achieved by the calibration algorithm. Therefore, we conclude that the proposed background mixed-signal calibration technique will be able to achieve good performance in the presence of slow-time variations of the sampling phase errors such as those caused by variations of temperature, voltage, or any other nonideal condition.

In Fig. 21 we present a relative long calibration test. It demonstrates the stability of the technique to remain in execu-

[7]For comparison purposes, the calibration algorithm is turned on after $\sim 4\times 10^8$ symbols are logged.

[8]In this experiment, the supply voltage and temperature are not changed. However, in a real implementation, notice that variations of the delays could be caused by time variations of several factors such as voltage or temperature.

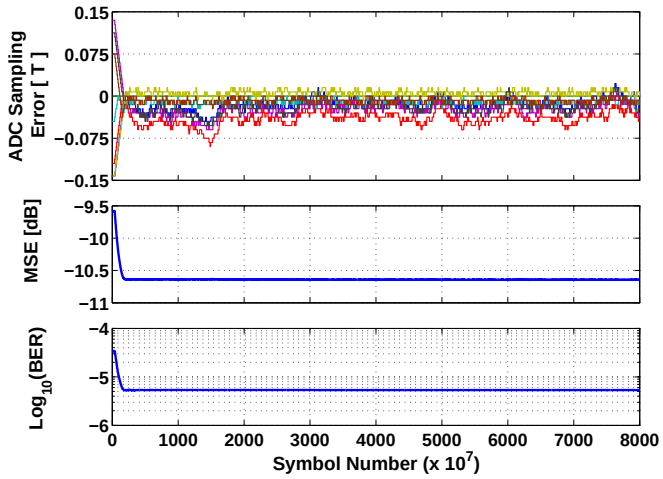


Figure 21. Calibration convergence and stability in the relative *long term*. Input SNR=10 dB and $\alpha = 10^{-7}$.

tion in *background* mode. In this example, we can observe how the small clock phase oscillations after convergence have not impacted on MSE/BER performance. Additionally, note that we have fixed one of the ADC clock phases as a *reference* for the rest of the interleaves (i.e. ADC1 is fixed, however it could be any other). This fact avoid any *long term* general phase derivation that could arise from the interaction between the FSE adaptation and the TI-ADC phase adjustment algorithm.

In Fig. 22 several calibration tests are summarized using SNR vs. BER curves. For this plot, different setups in the recursive filter of the MSE estimation block (i.e., α coefficient) are tried in combination with several input SNR values. For example, we have set SNR=6 dB at the receiver input and we have calibrated the TI-ADC using $\alpha = 10^{-7}$. After calibration convergence, we have measured the BER at the receiver to obtain the corresponding point in the curve of Fig. 22 and then we repeated the test for the other values of α and input SNR. Analyzing these results, we can note that the phase calibration achieves a very good performance and a very low SNR penalty if $\alpha \leq 10^{-5}$. Furthermore, using $\alpha \ll 10^{-6}$ we can obtain a more accurate MSE estimator with no penalty in terms of both, power consumption and logic complexity. However, there is a trade-off between accuracy of the estimator and the speed of the phase adjustment (i.e., more time is required by the estimator to achieve an stable output between each calibration step). Despite this trade-off is not usually a problem in ultra-high speed receivers, in the case of faster calibration is demanded, the non-constant time step methodology previously demonstrated can be used. On the other hand, Fig. 22 shows that the calibration performance using an inaccurate MSE estimator (i.e., $\alpha \gg 10^{-5}$) could result in a relative poor receiver performance and it should be avoid.

To analyze the behavior of the calibration technique at a higher speed than it can be demonstrated in the platform, we can rely in computational simulator of a transceiver model. Fig. 23 shows the performance of calibration algorithm in a coherent optical transceiver with dual-polarization (DP) quadrature phase-shift keying (QPSK) modulation at 40/100 Gb/s (see [14] for simulation setup details). Our results confirm the

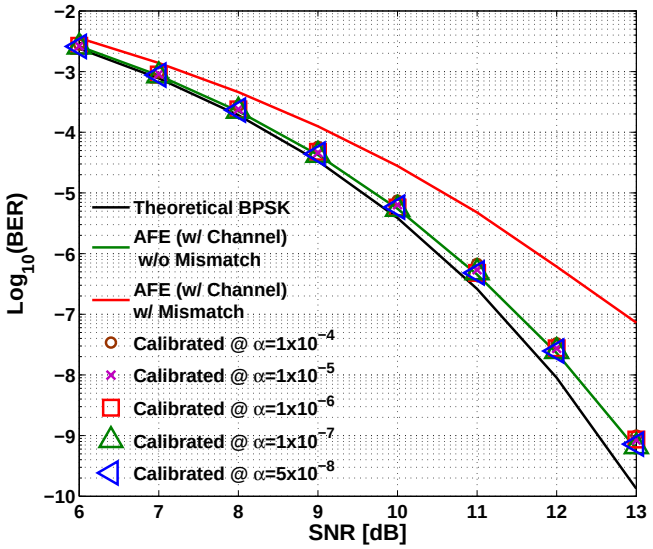


Figure 22. Receiver performance after different α calibration tests.

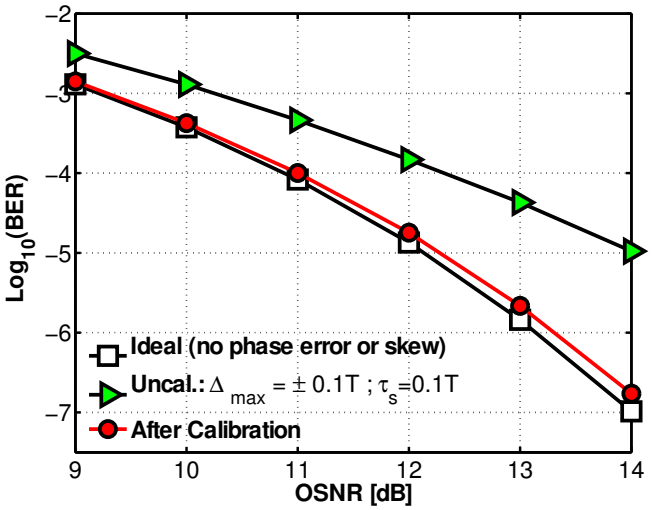


Figure 23. BER vs. optical SNR (OSNR) curve example for a DP-QPSK coherent optical receiver [14].

good performance of the proposed mixed signal calibration algorithm in high speed communication system.

VI. Conclusions

An effective sampling time error calibration technique for TI-ADC in digital receivers has been proposed and experimentally demonstrated in this work. The algorithm exploits information available at the receiver as the MSE at the slicer, to detect and correct the sampling phase mismatch, avoiding thus the use of an external analog reference and/or direct digital signal processing. The phase adjustment is carried out in the analog domain to avoid extra DSP complexity and power consumption penalty. This way, extra complexity required by the calibration method is reduced to a simple state-machine and a recursive filter to estimate the MSE. Moreover, in this work we have designed and developed an experimental platform to evaluate the performance of a communication system with the TI-ADC calibration algorithm. Our measurements

have demonstrated that the SNR penalty of a digital BPSK receiver caused by sampling time errors in TI-ADC can be reduced from 1dB to less than 0.1dB at a BER of 10^{-6} by using the proposed calibration algorithm. The proper background operation has also been experimentally demonstrated. Furthermore, a robust convergence of the calibration algorithm has been verified under different operation conditions such as input SNRs, time delay step used for calibration, and filter bandwidth of the MSE estimator. These features make the proposed technique to be suitable for application in next-generation coherent optical/back-plane digital receivers.

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