All-Digital High-Resolution PWM With a Wide Duty-Cycle Range

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***Abstract*—An all-digital high-resolution pulse-width modulator in standard 130-nm CMOS technology is presented in this work. The architecture is based on a digitally-controlled delay element with variable time interval up to 50 ps and adjustable against process, voltage and temperature (PVT) variations. Post-layout simulation results show a linear response between the control word and delay. The PWM modulator uses several delay elements in a hybrid configuration that allows to obtain duty cycles with 18-bit resolution, without using a high-frequency internal clock while maintaining low power consumption.**

***Index Terms*—Pulse-width modulation (PWM), delay-line, CMOS integrated circuits, high-resolution, programmable delay.**

I. Introduction

Modern CMOS technology is continuously scaling, producing faster transistors while reducing supply voltages allowing to achieve better accuracy in the time domain rather than in the voltage domain. Using a digital pulse-width modulator (DPWM) to encode the information in the position of the signal edges is an effective solution in terms of hardware complexity in comparison to sigma-delta approaches. A key issue of DPWM is to obtain high resolution and good linearity with reduced silicon area and low power consumption.

High-resolution pulse-width modulators (HRPWM) find applications in different fields of electrical engineering. Some examples are high resolution dimming of LED lighting to reduce flicker phenomenon [1], motor control applications [2], digitally-controlled DC-DC converters [3], [4] and other types of switched-mode power supplies that require low quantization noise in their PWM for the elimination of limit cycles and undesirable oscillations [5]. HRPWM are also being used for novel types of RF modulators based on switching amplifiers in which time resolution is one of the main limitations [6], [7]. It could also be used in switching audio amplifiers [8] to achieve high fidelity with low distortion.

Different DPWM topologies that provide high-resolution have been proposed in the literature [9]. Counter-based DPWM is a direct implementation of an analog PWM, where an n-bit counter developes a ramp waveform that is compared to a digital code to produce the output signal. An excellent linearity between input code and duty-cycle is achieved with this architecture, where the required input clock frequency is $f_{\text{clk}} = 2^n f_{\text{pwm}}$ for an n-bit DPWM operating at f_{pwm}. For a high-resolution DPWM, this clock frequency can result in quite hard timing constraints and a great increase of the power consumption. For example, a counter-based DPWM with 12-bit resolution working at $f_{\text{pwm}} = 100$ kHz needs a clock frequency of $f_{\text{clk}} = 400$ MHz.

Delay-line based architecture uses the propagation delay through 2^n delay elements connected in cascade to generate the high-resolution PWM signal, using a 2^n-input multiplexer to select the different outputs of delay cells. In this way, a high clock frequency is not required for the system. This approach is suitable for low power applications. Although the chip area is a limiting factor for this implementation and matching of 2^n delay stages affects the linearity of the digital to time conversion. A hybrid architecture could be used by the combination of the counter-based and delay-line based approaches that provides high-resolution pulse width in a power and area efficient solution, using the counter for a coarse adjustment of the duty cycle and delay-line for a fine adjustment.

In this work, the design of a hybrid HRPWM with 18 (8+10) bits of resolution is described. The most significant bits of the duty-cycle are produced by the conventional DPWM operating at f_{clk} and the least significant bits are generated with a pulse former based on digitally-controlled delay elements. The proposed delay elements allow the calibration of minimum step delay in order to achieve high linearity and improve matching between delay stages.

This paper is organized as follows. A brief review of the circuits used to achieve high-resolution time steps and the proposed delay element are presented in Section II. The pulse former used to generate the high-resolution duty-cycles is described in Section III. Overall system architecture and implementation in a 130-nm CMOS technology are presented in Section IV. Finally, Section V concludes the paper.

II. Delay Elements

For a given VLSI technology, the time resolution that could be achieved depends on one inverter delay, although this delay can be made smaller using certain circuit techniques like Vernier delay-line or resistive interpolation, among others [10], [11]. Delay elements suffer from nonlinearity due to process, supply voltage and temperature (PVT) variations thus

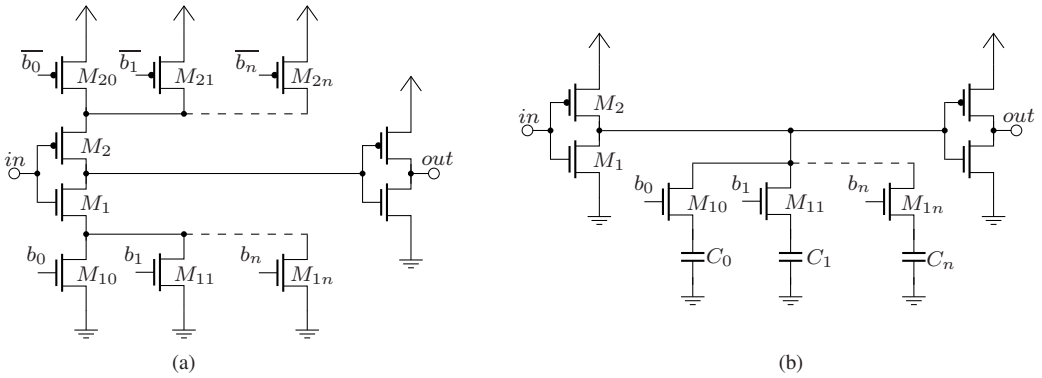

Fig. 1. Circuit schematics of (a) current starved inverter and (b) shunt capacitor inverter.

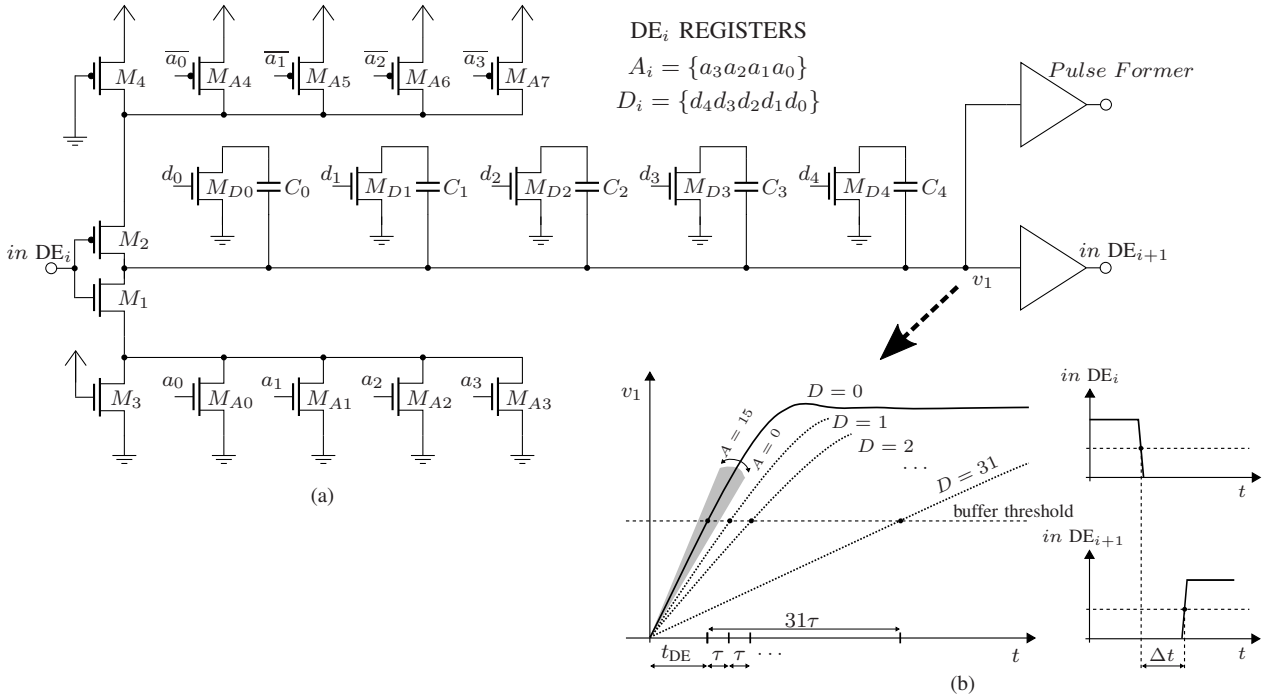

Fig. 2. (a) Circuit schematic of implemented tunable delay element and (b) timing waveforms of the signals in the delay element.

calibration is required to produce the originally intended time interval. This is achieved by the implementation of tunable delay cells, which also can be reconfigured easily allowing flexibility. Delay elements can be controlled through an analog signal or a digital word; the first one achieves the finest delay interval while the latter allows only delay values in discrete steps, but with the benefits of simpler circuits, robust designs and digital programmability which are more convenient for ASIC designs [12], [13], [14].

A. Digitally-Controlled Delay Elements

The most commonly used digital delay-line topologies are based on current-starved inverter (CSI) and shunt-capacitor inverter (SCI) techniques. Fig. 1(a) shows the basic building block of a CSI-based delay element. It consists of an array of parallel connected transistors placed at the source of M_1 and M_2, used to control the rise and fall times of the output voltage of the inverter applying a binary n-bit word to the controlling transistors ($M_{10}, M_{11}, ..., M_{1n}, M_{20}, M_{21}, ..., M_{2n}$) [15]. Usually, their W/L ratios are binary-weighted, and the charging and discharging currents of the output capacitance of the first inverter are modified when each pair is activated.

In SCI-based topologies, the different delay values are achieved by adding load capacitors to an inverter output as shown in Fig. 1(b). Turning on the nMOS switches ($M_{10}, M_{11}, ..., M_{1n}$) through a digital vector allows to vary the capacitive load, changing the speed and response of the delay element [16].

Both strategies have some advantages and drawbacks: CSI-based delay elements have much less power consumption than those based on load-increasing method, but they exhibit a non-linear and non-monotonic behavior between the input vector and the output delay due to capacitance changes when con-

trolling transistors are turned on and off; SCI-based structures have robustness to process variation and can produce linear delay steps in a wide range, although it might be necessary to use large capacitance values which are costly in terms of silicon area.

B. Proposed Delay Element

A hybrid digitally programmable delay element that combines CSI and SCI techniques was designed (Fig. 2). A high-resolution delay that varies linearly with the control word uses a 5-bit register $D_i = \{d_4{:}d_0\}$ to controlling a binary-weighted load $C_4{:}C_0$ by the selector switches $M_{D4}{:}M_{D0}$, where C_0 is equal to the unit capacitance C_u, $C_1 = 2C_u$, $C_2 = 4C_u$, $C_3 = 8C_u$, and $C_4 = 16C_u$. The inverter output current provided by M_1 and M_2 that drives the capacitive load can be adjusted by controlling the binary-weighted transistors $M_{A7}{:}M_{A0}$ by means of the 4-bit registers $A_i = \{a_3{:}a_0\}$ and $\overline{A_i} = \{\overline{a_3}{:}\overline{a_0}\}$ for nMOS and pMOS transistors, respectively. The output of the delay element is provided by two fast buffers that improve the rise and fall times of the waveform. The output of the first buffer is applied to the input of the next delay element, and the other buffer's output is connected to the pulse former circuit. The use of this accurate delay element for generation of the high-resolution duty-cycles is explained in detail in the following section.

III. Duty Cycle Generation

The output time delay of each DE_i is given by:

$$T_i = t_{\text{DE}} + D_i\tau \tag{1}$$

where t_{DE} is the minimum delay (propagation delay of the delay element when $D_i = 0$), τ is the delay resolution (minimum delay step), and D_i is the programmable value, variable between 0 and $2^5 - 1 = 31$ changes of the load. Now, cascading multiple n delay elements and using a simple OR logic gate, it is possible to add a time delay Δt at the end of the input signal with duty-cycle d_{in} produced from conventional digital pulse-width modulator, using the basic circuit shown in Fig. 3. This allows the generation of $N = 31n$ different duty-cycles with temporal resolution τ. If the condition $d_{in} > \Delta t$ is guaranteed by the PWM signal applied in v_{in}, the pulse width of the signal in the OR output will be $d_{out} = d_{in} + \Delta t = d_{in} + n \cdot t_{\text{DE}} + \sum_{i=1}^{n} D_i\tau$. Generally, the propagation delay t_{DE} is not negligible therefore it is mandatory to compensate this unavoidable delay. The propagation delay of the OR gate t_{OR} also affects the waveform and might be considered, although it does not cause changes in d_{out}.

A simple solution for this issue is the implementation of an additional delay line with all the delay elements DE'_i set to the minimum delay, $D'_i = 0$, for all the elements of the complementary delay line, represented as a ground connection in Fig. 4. The time delay between nodes v_m and v'_m is $T_{mm'} = \sum_{i=1}^{m} D_i\tau$, and therefore only depends on τ and the value of configuration registers D_i. The use of a n-inputs multiplexer and n OR gates allows to get N programmable different values of duty-cycles with a time resolution τ using

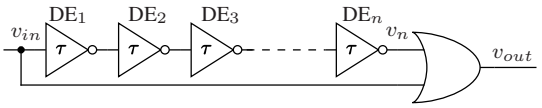

Fig. 3. Basic high-resolution pulse former.

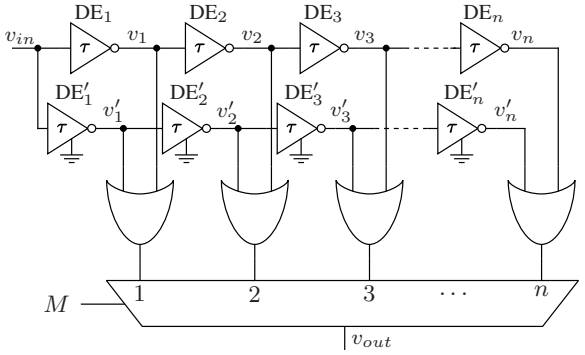

Fig. 4. Pulse former with additional delay line.

$2n$ delay elements. However, this would produce a rising-edge with variable position, which is not desirable: the output signal is shifted a variable time given by $m \cdot t_{\text{DE}} + t_{\text{OR}} + t_{\text{MUX}}$ where m is the selected multiplexer input. Another drawback of this scheme is that signal polarity is inverted for odd multiplexer inputs, thus is necessary to use of $n/2$ additional inverters, and take into account the time delay introduced by them. To ameliorate these effects, a modified architecture was proposed and implemented.

A. Proposed circuit

To generate the high-resolution duty-cycles without variable rising-edge time and to allow the use of the produced signal in a synchronous circuit, the architecture presented in Fig. 5 is proposed. This circuit generates N values of duty-cycles with the same time resolution τ but with fewer delay elements and logic gates than previously discussed topologies and shown in Fig. 3 and Fig. 4. The delay elements are grouped in pairs to minimize the number of logic gates used and the multiplexer size, except the firsts $\text{DE}_{1:4}$ that are implemented individually.

Its operation is described in Fig. 6: delay cell DE_1 is set to zero ($D_1 = 0$) and signal in v_1 is the inverted value of v'_{in} delayed by t_{DE}. Selecting a single stage delay (input 1 of the multiplexer), $d_{out} = d'_{in}$ and the output signal in v_{out} is delayed $T_{out} = t_{\text{INV}} + t_{\text{DE}} + t_{\text{OR}} + t_{\text{MUX}}$. When the multiplexer input selected is 2, the output signal in v_{out} is delayed the same value T_{out} but duty-cycle has changed and now is $d_{out} = d'_{in} + D_2\tau$. The rising edge of the signal in v_{out} keeps on the same time value for successive combinations of the multiplexer, solving the issue of variable shift in the output signal and setting node v_1 as reference for the time delay. The detailed operation of the circuit is described in the next subsections.

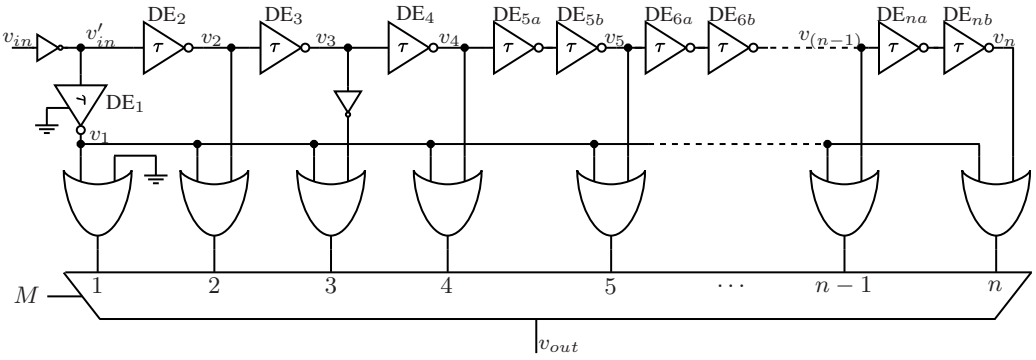

Fig. 5. Proposed high-resolution pulse former.

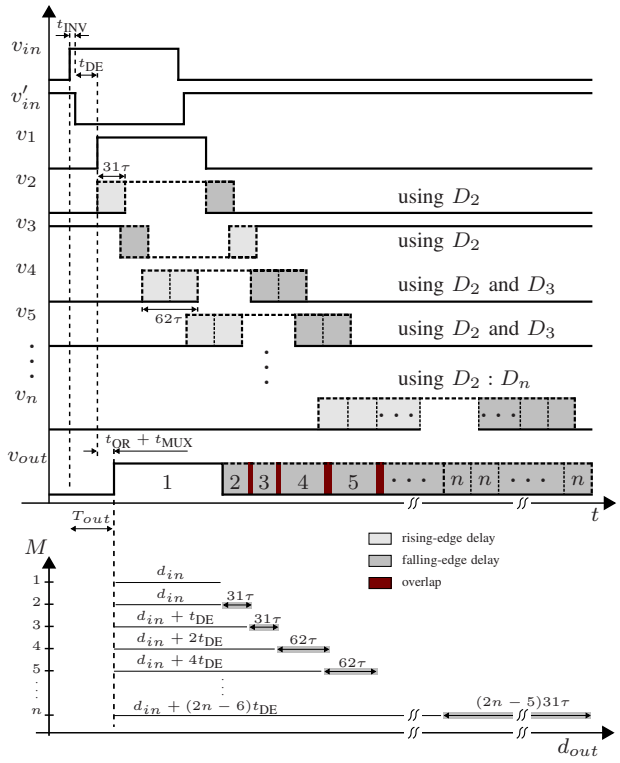

Fig. 6. Timing diagram of pulse former signals and duty-cycle generation for each multiplexer input.

B. Pulse former analysis

The time delay considering the nodes v_2 and v_1 can vary between $0 \leq T_{21} \leq 31\tau$ according to the value of register $D_2 = 0 : 31$. Between v_3 y v_1 the possible variation is now $t_{\text{DE}} \leq T_{31} \leq t_{\text{DE}} + 31\tau$ using only D_3 register while $D_2 = 0$, but if D_2 is used the feasible time steps produced by DE$_2$ are added and the range is duplicated ($t_{\text{DE}} \leq T_{31} \leq t_{\text{DE}} + 62\tau$). To take advantage of the minimum propagation delay t_{DE} provided by every stage DE$_i$, design can be based in achieving an integer relationship $k = t_{\text{DE}}/\tau < 31$. This integer value can be chosen to guarantee a proper operation after calibration under PVT variations, implementing a configurable multiplexer logic that changes its output in agreement with k. Thus, the minimum delay of input signal in v_3 is $2t_{\text{DE}} = 2k\tau$ and delay range for T_{31} is $k\tau \leq T_{31} \leq 2k\tau$, using D_2 or D_3 registers indistinctly. Given that each delay element inverts the polarity of the signal in its input, to generate the correct duty-cycle in the OR gate corresponding to multiplexer input 3 an inverter was added after v_3. For restoring the original polarity of the input signal at the multiplexer output v_{out}, an inverter was also added at the beginning of delay line. Both inverters were designed with minimum size and their propagation delay are less than $\tau/4$, therefore they are not considered in the remaining analysis. In v_4 the polarity of the signal is the same as the input signal v_{in}. For mux-inputs 5 to n the delay elements were grouped in pairs, thus eliminating the need of restoring polarity signal through the addition of inverters. There are several ways to achieve a monotonic increase of the duty-cycle in v_{out} using the topology presented in Fig. 5, the following subsection describes one of them.

C. Logic for duty-cycle generation

Minimum delay for T_{41} is $2k\tau$ while for T_{51} is $4k\tau$, therefore the range of time delays corresponding to mux-input 4 must be $2k\tau \leq T_{41} \leq 4k\tau$ and is achieved varying D_2 for the firsts k steps with $D_3 = 0$, and varying D_3 with $D_2 = k$ for delay steps from $(k+1)$ to $2k$. Because there is no one-to-one correspondence between a desired duty-cycle d_{out} and the D_i registers setting, to simplify the control logic it was chosen to operate the pairs of delay elements as following: for an input $4 \leq i \leq n-1$ of multiplexer, the registers $D_{4:n}$ are set to zero and delays caused by D_2 and D_3 registers are used as variable elements, so that a given delay may be obtained by proper setting of these two registers and choosing the corresponding multiplexer input. The rest of delay elements $D_{4:i}$ could also be used to modify d_{out}, but the increment of duty-cycles in v_{out} would not be monotonically increasing with the selected multiplexer input. Thus, the possible delays between the nodes v_i and v_1 are $(2i-6)k\tau \leq T_{i1} \leq (2i-4)k\tau$, increasing the duty-cycle of the output signal in this amount.

The situation is different for the last multiplexer input n where time delay T_{n1} can be modified using all delay elements from DE$_2$ to DE$_n$, achieving a maximum delay equivalent to two times the delay with registers $D_{2:n} = 0$. Table I lists the values of multiplexer selector according to desired duty-cycle

TABLE I
RANGE OF DUTY CYCLES FOR MULTIPLEXER INPUTS

min d_{out}	max d_{out}	Mux Sel	Register Values[1]				d_{out} with $k=29, n=12$	
d_{in}	d_{in}	1	$D_{2:n}=X$				d_{in}	d_{in}
$d_{in}+\tau$	$d_{in}+k\tau$	2	$D_2=1:k$	$D_{3:n}=X$			$d_{in}+\tau$	$d_{in}+29\tau$
$d_{in}+(k+1)\tau$	$d_{in}+2k\tau$	3	$D_2=1:k$	$D_3=0$	$D_{4:n}=X$		$d_{in}+30\tau$	$d_{in}+58\tau$
$d_{in}+(2k+1)\tau$	$d_{in}+3k\tau$	4	$D_2=1:k$	$D_3=0$	$D_{5:n}=X$	$(D_4=0)$	$d_{in}+59\tau$	$d_{in}+87\tau$
$d_{in}+(3k+1)\tau$	$d_{in}+4k\tau$	4	$D_2=k$	$D_3=1:k$	$D_{5:n}=X$	$(D_4=0)$	$d_{in}+88\tau$	$d_{in}+116\tau$
$d_{in}+(4k+1)\tau$	$d_{in}+5k\tau$	5	$D_2=1:k$	$D_3=0$	$D_{6:n}=X$	$(D_{4,5}=0)$	$d_{in}+117\tau$	$d_{in}+145\tau$
$d_{in}+(5k+1)\tau$	$d_{in}+6k\tau$	5	$D_2=k$	$D_3=1:k$	$D_{6:n}=X$	$(D_{4,5}=0)$	$d_{in}+146\tau$	$d_{in}+174\tau$
...	...	...	...	...	...	...	...	...
$d_{in}+((2n-6)k+1)\tau$	$d_{in}+(2n-5)k\tau$	n	$D_2=1:k$	$D_{3:n}=0$			$d_{in}+523\tau$	$d_{in}+551\tau$
$d_{in}+((2n-5)k+1)\tau$	$d_{in}+(2n-4)k\tau$	n	$D_2=k$	$D_3=1:k$	$D_{4:n}=0$		$d_{in}+552\tau$	$d_{in}+580\tau$
$d_{in}+((2n-4)k+1)\tau$	$d_{in}+(2n-3)k\tau$	n	$D_{2,3}=k$	$D_4=1:k$	$D_{5:n}=0$		$d_{in}+581\tau$	$d_{in}+609\tau$
...	...	...	...	...	...	...	...	...
$d_{in}+((4n-12)k+1)\tau$	$d_{in}+(4n-11)k\tau$	n	$D_{2:(n-1)}=k$	$D_n=1:k$			$d_{in}+1045\tau$	$d_{in}+1073\tau$

[1] X: don't care; k = a fixed register value, according to t_{DE}/τ ratio; $1:k$ = any digital word between 1 and k.

values and corresponding digital words for D_i. This table also shows an example for $k=29$ and $n=12$ stages. This value of k was chosen based on the implemented design and can be digitally programmed according to the calibration done in delay element against PVT variation.

Implemented delay line has a 12-input multiplexer, the same amount of OR gates and 20 delay elements (19 of them programmables and DE_1 fixed). This configuration results in a maximum of 1073 delay steps, limited to 10 bits (1024 steps) in the logic that controls the least significant bits of the duty-cycle. Although the chosen value for k leaves unused values in D_i registers (30 and 31), this is a minor drawback compared to other schemes: to achieve the same 10-bit resolution with the circuit shown in Fig. 3 it would be necessary to use 33 delay elements, and 66 stages using the circuit presented in Fig. 4.

IV. IMPLEMENTED SYSTEM

Fig. 7 shows the system architecture implemented, including the proposed high-resolution pulse former and logic described in the previous section: a counter-based DPWM modulator, an SPI communication module and an SRAM memory with 512 words of 18 bits where the duty-cycles are stored. The upper 8 bits of memory data are used for the DPWM, and the lower 10 bits are used for the high-resolution pulse former. The memory size is enough to store the samples of the signal to be represented as a PWM signal for many applications.

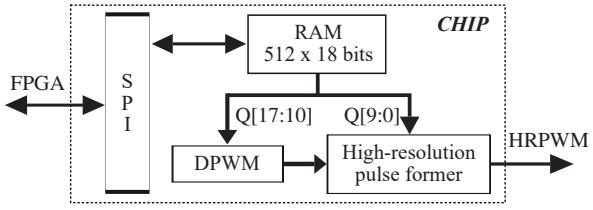

Fig. 7. Block diagram of implemented system.

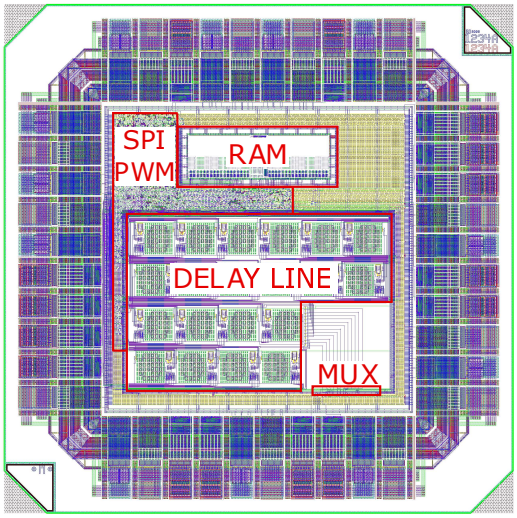

Fig. 8. Layout of the implemented system.

For the purposes of testing, the architecture incorporates several multiplexers (not shown in Fig. 7) to isolate the different modules, allowing the use of the delay line with an external signal. In this way, each delay element DE_i can be tested and calibrated individually using D_i and A_i registers, allowing to choose a proper value for k register. Under normal operation, the user can configure the number of DPWM counts and also HRPWM counts, based on the previous calibration and operating clock frequency; and the synthesized logic sets the value of the D_i registers and multiplexer selector. The proposed system was implemented in a 0.13-μm CMOS process, with a nominal supply voltage of 1.2 V and is currently in fab. The layout of the IC is shown in Fig. 8.

The layout of the delay element was carefully designed, considering identical geometries and wiring for a good matching and including dummy components for all the subcircuits. Post-

TABLE II
DELAY CHANGE FROM NOMINAL CONDITIONS UNDER PVT VARIATIONS

Process		**Voltage**		**Temperature**	
SS	FF	$0.9V_{\text{DD}}$	$1.1V_{\text{DD}}$	125°C	−40°C
16.4%	−14.6%	12.3%	−10.6%	8.2%	−12.8%

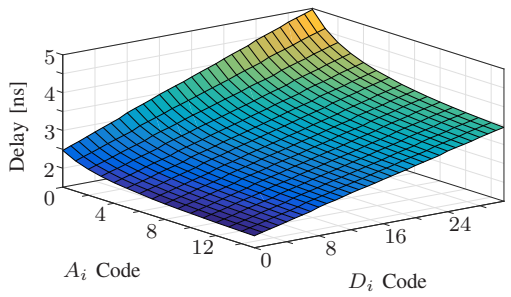

Fig. 9. Propagation delay of the implemented delay element.

layout simulations were carried out to analyze the influence of capacitive coupling between the different building blocks of the delay line.

A. Post-layout simulation results

Under nominal conditions, the proposed delay element has an average time step of $\tau = 65$ ps and $t_{\text{DE}} = 2$ ns for calibration registers set to the value $A_i = 3$, allowing the variation of delay step in a range between 20% and -18% of this value using the calibration registers $A_i = 0$ and $A_i = 15$, respectively. This range is suitable to compensate for the changes in propagation delay due to PVT variations, which are listed in Table II.

The propagation delay ($t_{\text{DE}} + D_i\tau$) of the implemented delay element is shown in Fig. 9, where the performance of the different strategies used to produce the delays can be appreciated: a very linear increase of time delay for increasing values of D_i (SCI topology) and non-linear reduction of delay for increasing values of A_i (implemented through CSI technique).

B. Intended application of high-resolution PWM

Designed IC could be included in several systems where high-resolution time is desired with a clock frequency in the order of 10-20 MHz, reducing the power consumption using standard CMOS technologies. In order to illustrate the operation of the proposed system, a comparison with a conventional digital PWM can be done. Choosing a clock frequency $f_{\text{clk}} = 15$ MHz and a PWM frequency of $f_{\text{pwm}} = 75$ kHz, possible duty-cycles are $f_{\text{clk}}/f_{\text{pwm}} = 200$ for digital PWM with a minimum time step $T_{\text{clk}} = 1/f_{\text{clk}} = 66.67$ ns. Instead, adjusting the delay step of HRPWM in $\tau = 65$ ps, $T_{\text{clk}}/\tau \approx 1024$ steps in each clock period, achieving an equivalent resolution of 17.64 bits against 7.64 bits for the DPWM without high-resolution capability.

V. CONCLUSION

In this paper, a high-resolution PWM with wide range was proposed and fabricated in 0.13-μm process technology. Post-layout simulation results show a monotonic and linear response for the proposed delay element, with the ability to adjust duty-cycle resolution against PVT variations or due to clock frequency changes. The pulse former circuit presented allows to compensate propagation delay of programmable delay elements and minimize the number of stages used to generate high-resolution duty-cycles. Experimental measurements will be carried out to corroborate the suitable performance of the overall system proposed.

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