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# A solution for future single-electron-counting fast-readout Skipper-CCD experiments: high channel density front-end electronics design and noise performance analysis

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## ABSTRACT

The Skipper-CCDs, a special type of charge-coupled device (CCD) sensor that features sub-electron readout noise levels, was proposed decades ago. However, only in recent years it has been possible to develop large size Skipper-CCDs ensuring stable operation. Their extreme low noise operation makes them suitable for experiments that require low thresholds and high energy resolution, such as dark matter and neutrino interactions detection, and more recently quantum-imaging and astronomy. New experiments are planning to use kilograms of active silicon from Skipper-CCDs as sensitive mass. In this way, they can achieve extremely low detection thresholds and a high probability of particle interaction. However, this approach needs arrays of thousands of Skipper-CCDs operating at the same time imposing challenging requirements. Also, introduction of this technology in astronomy and quantum-imaging applications requires a large number of channels per sensor to speed up the readout. The front-end needs to be redesigned from scratch: it must achieve low noise performance, be simple for easy integration and allow the routing of thousands of channels out of the sensors with minimal connections. This paper presents a detailed analysis of options for the front-end electronics and their noise performance. It describes a novel way of using a dual-slope integrator with minimal components to pile up the charge of consecutive readouts of the same pixel in a concept that we call a multi-slope integrator. This reduces drastically the output bandwidth, simplifying the wiring and the warm electronics. These proposals will allow the generation of new scientific instruments based on Skippers-CCD arrays.

**Keywords:** Charge-Coupled Device, Skipper-CCD, Sub-electron noise, Dual-slope integrator, Multi-slope integrator, Differential integrator, CCD readout

## 1. INTRODUCTION

Charge coupled devices (CCDs) are widely used in instruments such as cameras for detection of photons in astronomy, and in cosmology to detect other particles that interact with the silicon atoms of the sensor. The readout noise of an standard CCD is in the order of 2 or 3 e−, mostly limited by the white and $1/f$ noise combination of the output amplifier of the sensor.[1]

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The Skipper-CCD[2,3] is a CCD with a modified output stage that allows to measure the charge of each pixel several times, and, since the noise of each measurement is independent, the pixel value can be obtained by averaging the measurements reducing in this way the noise well below 1 e−. The readout electronics, called Low Threshold Acquisition controller (LTA), specifically designed to control, acquire and processes[4,5] the Skipper-CCD signals was recently presented.[6]

The good performance obtained by the Skipper-CCD and the LTA, achieving sub-electron noise with a wide dynamic range, has allowed the progress and planning of many scientific experiments. The Sub-Electron-Noise Skipper-CCD Experimental Instrument (SENSEI) uses Skipper-CCDs for Light Dark Matter Searches[7] and Dark Matter in CCDs experiment (DAMIC)[8] is also planning to do so. In the same direction, the Observatory of Skipper CCDs Unveiling Recoiling Atoms (OSCURA project), is planning to have a 10 of kg active silicon experiment for dark matter detection based on Skipper-CCDs.[9]

The Coherent Neutrino-Nucleus Interaction Experiment (CONNIE)[10] searches for reactor neutrinos using standard-CCDs detectors, and the next generation of neutrino experiments: the Neutrino Interaction Observation with a Low Energy Threshold Array ($\nu$−IOLETA experiment) is planning to use several kg of Skipper CCDs.[11]

Besides Dark Matter and neutrinos, there are other possible applications for Skipper CCDs such as: spectrograph instruments, single photon counting quantum imaging cameras; high precision measurements of silicon properties (quenching factor, fano factor, ionization energy distribution, temperature dependence),[12] cold neutron quantum measurements,[13] etc.

In all these cases the number of channels increases dramatically, either to speed-up readout by adding more channels to a CCD, or due to the amount of CCDs required to increase the probability of particle interaction. The electronics for those experiments has to be designed to achieve the necessary scalability in terms of bandwidth and mechanical properties. This paper present a new design of the front-end electronic towards that objective. The work is organized as follows: In Section 2 the readout of the Skipper-CCD using Dual Slope Integration (DSI) is reviewed. Section 3 discusses options for a Skipper-CCD system with high channel density, while Section 4 focuses in the front-end electronics which is close to the sensor and is in-charge of computing the pixel value. A novel Multiple Slope Integrator (MSI) is proposed, which integrates the charge of several skipper samples of the same pixel within the analog circuit, reducing the bandwidth required to transmit the information to upstream electronics. Simulations focused on the noise performance of the front-end electronics using the proposed MSI topology are presented in Section 5, and conclusions are presented in Section 6.

## 2. SKIPPER-CCDS READOUT

The traditional scheme/architecture for scientific CCD readout is shown in figure 1. The sensor output signal is fed to a nearby preamplifier and then transmitted to the warm readout electronics outside the cryostat via independent wires. The electronic system then performs a Dual Slope Integration (DSI) to obtain each pixel value using analog processing circuits.[14,15] Recently, new systems have been developed with high speed Analog to Digital Converters (ADCs) to compute pixels through a fully digital processing (Digital DSI).[16]

The DSI results from the implementation of the following equation:[1]

$$P_i = \frac{A}{I_W}\left(\int_{I_W+\tau}^{2I_W+\tau} x(t)dt - \int_{0}^{I_W} x(t)dt\right), \tag{1}$$

where $P_i$ is the final pixel value, $x(t)$ is the CCD output or video signal, $\tau$ is the time spent to transfer the charge to the sensing node after the reset, $A$ is an arbitrary gain of the signal processing chain, and $I_W$ is the pixel integration time. The first integral represents the integration over the charge and the second is over the pedestal (reference level), both integrals are normalized by the integration time $I_W$.

In general the readout noise per pixel decreases with the pixel integration time as described in,[1] but due to the low frequencies components of this noise introduced by the CCDs on-chip output amplifier, the reduction has a limit after which it remains constant despite an increase in the integration time.[2]

Unlike standard CCDs, Skipper-CCDs allow multiples independent measurements (samples) of charge of the same pixel. The $N$ samples are then averaged resulting in a reduction of the measurement noise by a factor of $\frac{1}{\sqrt{N}}$. This remains true even after reaching the limit noise reduction for long integration times mentioned previously. This fact turns the Skipper-CCD into a sub-electron noise device and also positions it among the most sensitive instruments in the world.[3] However, this capacity comes with a price, since each pixel needs to be sampled $N$ times, the amount of information that needs to be transferred and stored also gets multiplied by the same factor $N$. This has some implications that will be described with further details in the following sections.

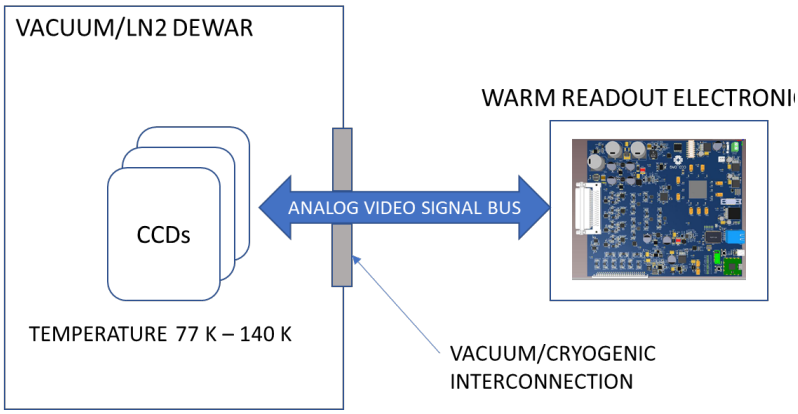


Figure 1. A common readout architecture for scientific CCDs. Sensor are cooled down by liquid nitrogen submersion or using vacuum and cryocoolers. Analog signals are then transported to the warm readout electronics

## 3. HIGH CHANNEL DENSITY FRONT END

One disadvantage of having Skipper-CCDs in low noise readout mode is the amount of time needed for readout. A typical skipper of $1500 \times 9000$ pixels with a readout mode of 100 samples per pixel ($N = 100$) and an integration time per pixel of 13 $\mu$s ($I_W = 13\mu$s) takes around 13 hours to complete using a single output amplifier. This time is approximately proportional to the integration time, the number of pixels and number of samples per pixel. One way to overcome this problem is by dividing the CCD in many sections, where each one has its own output stage, or channel. A single CCD can now be readout using many channels at the same time, decreasing the readout time by a factor equal to the number of channels. Applications like Astronomy and Quantum imaging need shorter readout times and sub-electron noise levels at the same time, so they may require a Skipper-CCD with tens of channels. Different scientific applications like Dark Matter and Neutrino detection require not only ultra low readout noise levels, but also a high amount of sensitive mass, because the predicted event rate per unit of mass is low.[8,17] This means they have to use several CCDs together to reach a minimum required event rate.

In both cases, when using sensors with multiples channels or multiples sensors working together, the system becomes a high channel density front-end.

The readout architectures described in section 2 can be scaled up for a high channel density system only up to a limit. When the number of channels increases by the order of hundreds these architectures become less and less practical. The mechanical constraints generated by the amount of sensitive analog lines mixed with clock lines, power lines and readout boards turn these architectures into an inefficient system, even for highly modular architectures. Also, routing hundreds of sensitive analog signals from the sensor to the upstream electronics increases the chances of cross talk, noise and faulty connections.

Adding to these constraints listed above is the amount of data that would be produced by high channel density Skipper-CCDs array during readout. Scaling it up to hundreds of sensors can produce also storage/transfer problems. This situation is further detailed in the following sections.

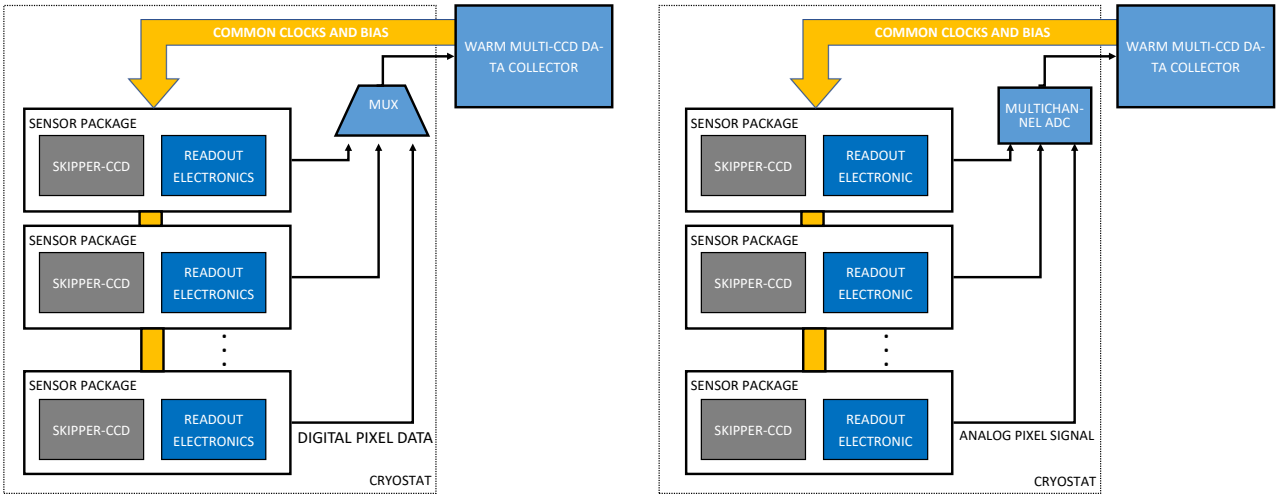


Figure 2. Alternatives of readout architectures for high channel density front-ends. Most of the readout electronics is integrated into the sensor package. The left option considers packages with digital output and digital multiplexing, while the one in the right uses cold multi-channel ADC electronics near the packages with partial integration.

A possible solution for these High Channel Density systems is to put a readout electronics as close as possible to the sensor so most of the processing stays embedded. Figure 2 describes two options, the one on the left integrates pixel signal processing and analog to digital conversion electronics into the CCD package. Digital multiplexing is used to transfer the information to the upstream electronics. The one on the right performs only the pixel signal processing close to the detector and then uses a multi-channel ADC hardware that is also inside the cryostat and close to the detectors. The clocks and BIAS voltages are shared by all sensors.

These modular architectures require a lot less connections outside the cryostat and are scalable even for thousands of channels. A key component shared by these architectures, and the main focus of this work, is the integrated readout electronic close to the sensors. This circuit must be compact because of space constraints, must have low power consumption and provide a low readout noise. An option is described with further details in the next section.

## 4. INTEGRATED ELECTRONICS: COMPACT LOW GAIN MULTI-SLOPE INTEGRATOR

We propose to use a low gain integrator as cold readout electronic near the sensor. This circuit uses a preamplifier and a controllable differential integrator for analog pixel computing as shown in Figure 3. Instead of using a Dual Slope Integration (DSI) as normally is done for skippers-CCDs, this circuit is designed to perform a Multi-Slope Integration (MSI). The difference between these two processes is that the integrator is reset after every pixel sample in the DSI, but only at the end of the last sample of the pixel in the MSI. Figure 4 shows an example of both methods for $N = 3$. Analog to digital conversion takes place only once per pixel in MSI instead of sampling each of the $N$ measurements of the same pixel as in DSI. The MSI output for a Skipper-CCD readout with $N$ measurements per pixel is given by the relation derived from equation 1

$$P_{i,MSI} = \sum_{j=0}^{N-1} \left( \int_{I_W+\tau+t_j}^{2I_W+\tau+t_j} x(t)dt - \int_{t_j}^{I_W+t_j} x(t)dt \right), \tag{2}$$

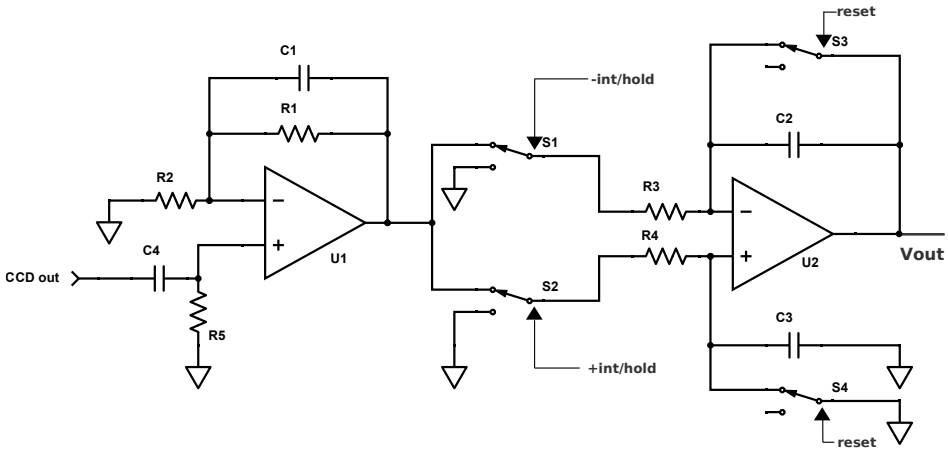


Figure 3. Schematic of the proposed integrated readout electronic with MSI.

where $t_j$ is the initial time of each measurement of the pixel charge and can be computed as $t_j = j(2I_W + \tau + \psi)$, where $\psi$ models any dead time between consecutive pixel measurements, $\tau$ is the time spent to transfer the charge to the sensing node after the reset, and $I_W$ is the pixel integration time.

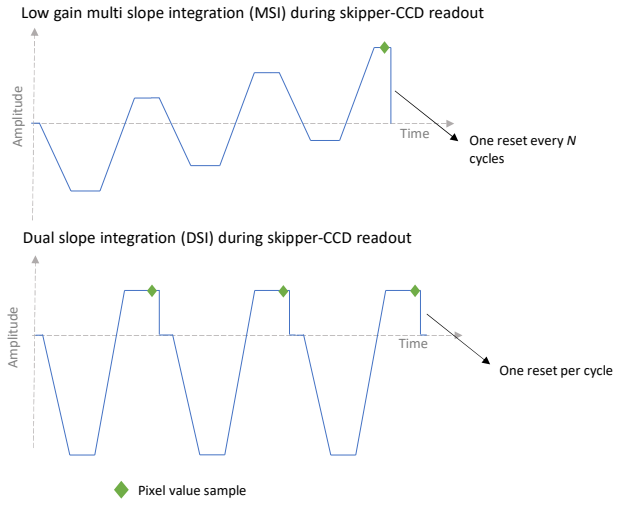


Figure 4. Comparison between dual slope integration (DSI) and Multi-Slope Integration (MSI) during Skipper-CCD readout for 3 samples per pixel ($N = 3$). For $N = 1$ both methods are equivalent except for the amplitude.

## 4.1 Preamplifier

The preamplifier $U1$ in figure 3 provides a first stage with high input impedance to avoid loading the CCD output stage and an amplification gain. Since this is the 1st stage after the CCD, the low noise characteristic and gain ensures a good signal to noise ratio for the rest of the electronic chain. This stage is also used to limit the bandwidth to up to a few hundreds kHz. $R1$ and $R2$ set the gain and $R5$ the input impedance.

## 4.2 Controllable differential integrator

$U2$ along with $R3$, $R4$, $C3$ and $C4$ in figure 3 conform the integrator circuit. This configuration is known as differential integrator[18] and it has the advantage of using a less components compared to the more traditional

approach of an inverting integrator with switchable inverter/non-inverter amplifier. $R3 = R4$ and $C3 = C4$ set the gain as described below.

Three digital lines are required to control the integrator, +int/-int to select positive or negative integration through the switches $S1$ and $S2$, and a reset control line through the switches $S3$ and $S4$. When neither positive nor negative integration is selected the output holds the previous value. The voltage at the differential integrator output is given by the following equation[18]

$$\text{Integrator}_{out} = \frac{1}{R3 \times C3} \int (S2_{out}(t) - S1_{out}(t))dt, \tag{3}$$

where $S2_{out}(t)$ and $S1_{out}(t)$ are the output of the selection switches $S1$ and $S2$.

This integrator also features native cancellation of most of the unwanted effects of non-ideal characteristics from the switches, since they contribute to the output in opposites ways with the same gain (see equation 3). This is important because it makes the circuit less sensible to problems related to analog switches, that otherwise must be compensated adding more components.

In the proposed MSI method, the integrating capacitor acts as a storage device. For each sample of the same pixel, the capacitor accumulates a charge proportional to the charge in the current pixel and it is not reset until the beginning of a new pixel. Therefore, the voltage produced at the end of the process on the integrator outputs is proportional to the charge of the current pixel. A low speed ADC can be used to digitize that voltage right after the end of the process.

The information stored in this way avoids excessive use of storage space. The amount of data produced by a Skipper-CCD using DSI is given by the following equation

$$\text{IMAGE\_DATA}_{\text{DSI}} = \text{bits}_{\text{pix}} \times \text{TOTAL\_PIX} \times N, \tag{4}$$

where, $\text{bits}_{\text{pix}}$ is the ADC bits resolution, TOTAL_PIX is the total number of pixels of the CCD, and $N$ is the number of samples per pixel. For MSI, only one value is sent every $N$ pixel samples, so the amount of data is reduce by a factor of $1/N$ as show in the following equation

$$\text{IMAGE\_DATA}_{\text{MSI}} = \frac{\text{IMAGE\_DATA}_{\text{DSI}}}{N}. \tag{5}$$

For a $1500 \times 9000$ pixels Skipper-CCD, 16 bits per pixel and 400 skipper samples per pixel, the resulting data storage requirement for the DSI method is 10GB per image, and only 25MB per image for MSI.

Also, since the value of each iteration (MSI cycles) is stored and used in the capacitor, it does not need to be transferred (in analog or digital form) to any other device before the end of pixel processing. The bandwidth required to transfer pixels values from the readout system using DSI is given by the following equation

$$\text{BW}_{\text{DSI}} = \text{bits}_{\text{pix}} f_{\text{pix}}, \tag{6}$$

where, $f_{\text{pix}}$ is the pixel frequency, approximately equal to $1/2I_W$. In the case of MSI only one pixel value is sent every $N$ so the bandwidth per channel is reduced by a factor of $1/N$. Bandwidth for MSI is given by

$$\text{BW}_{\text{MSI}} = \frac{\text{BW}_{\text{DSI}}}{N}. \tag{7}$$

For a integration time of $10\mu$s, 16 bits per pixel and 400 skipper samples per pixel, the DSI method requires a bandwidth per channel during readout of 800Kbps, while MSI only requires 2Kbps.

These reductions represent requirements of bandwidth and storage 99% lower compared to DSI in this configuration and they have critical impacts in a high channel density front end.

### 4.3 Gain considerations

The gain of the chain is limited by the saturation level of the analog stages. From this is clear that in order to avoid saturation, in a Multi-Slope Integration the gain must remain low for any of the possible 3 situations: (1) long integration time; (2) a high number of skipper samples $N$ of each pixel and (3) high charge dynamic range needed. The combination of the aforementioned situations results in a limit for the gain.

The gain of the whole chain is given by

$$\text{Gain[V/e-]} = ANSI_W \left(\frac{1}{RC}\right), \tag{8}$$

where, $A$ is the total amplification gain of analog stages excluding the integrator, $I_W$ is the integration time, $S$ is the sensitivity of the CCD output amplifier, which is around $2\mu$V/e- , $\frac{1}{RC}$ is the gain of the differential integrator , $C$ is the integrating capacitor value and $R$ the input resistor (see equation 3).

The output voltage is given by

$$V_{\text{out}}[V] = \text{Gain} \times \text{q[e-]} + \text{V}_{\text{offset}}, \tag{9}$$

where $V_{\text{out}}$ is the voltage right before the ADC, $q$ is the charge in the current pixel of the CCD and $V_{\text{offset}}$ is an offset value produced by a combination of the CCD and the readout electronics. This component does not decrease the data quality but can reduce the dynamic range. The values of $R$ and $C$ in the equation 8 depend on the application parameters: the dynamic range for current ($q_{max}$), maximum integration time $I_{Wmax}$, the maximum number of samples per pixel $N_{max}$, total chain amplification $A$ and maximum output voltage before saturation $V_{\text{out,max}}$.

For the case studied here $A = 20$V/V, $I_{Wmax} = 26.6\mu$s, $q_{max}\approx$350e$-$, $N_{max} = 500$, $V_{\text{out,max}} = 4.096$V. From equation 9 and 8: $RC = 36\mu$s. For $R = 2$Kohm, $C = 18n$F.

### 4.4 Real switches and capacitors considerations

Analog switches have some unavoidable unwanted characteristics that can affect the performance of this readout system in different ways. These are charge injection, ON resistance *Ron*, which is the resistance during conduction, OFF leakage currents, etc. Charge injection is responsibly for glitches in the signal during the switching.

*Ron* has variations between switches in the same family or even in the same chip, they also depend on the operating voltage. *Ron* affects the gain of the circuit because they connect in series with the inputs of the integrator. See $S1$ and $S1$ in figure 3. They also slow down capacitors discharge during the integrator reset as $S3$ and $S4$ are responsible of short-circuiting integrating capacitors $C1$ and $C3$. Because of the non-null resistance there is a minimum time for fully discharge that must be considered.

$S3$ and $S4$ OFF leakage current can also charge of discharge the integrating capacitors during active integration producing an error in the final result.

The differential integrator is less sensible to this non-ideal characteristics of analog switches. However, a switch with low glitch, medium to low *Ron* and super low OFF leakage current is recommended.

## 5. SIMULATION AND NOISE ANALYSIS

### 5.1 Circuit simulation

Simulations were carried out using spice models with different levels of accuracy according to each type of components: low levels of accuracy for resistor and capacitor models, including tolerance errors and parasitic resistances for capacitors. A moderate level of accuracy for operational amplifiers, including finite gain and bandwidth, finite input impedance and non-null output impedance. For analog switches, high accuracy models from vendors were used, that includes the behavior of ON/OFF resistance, charge injection, ON/OFF time and OFF leakage currents. The different precision levels allow to focus the analysis on those components that are known to be critical to noise and distortion, without increasing unnecessarily the simulation time.

The simulation covered the dynamic characteristics of each model with tolerance errors but did not include their noise contribution. However, one the main interests was to produce a noise contribution equivalent to the real CCD output amplifier as addictive noise at the input of the circuit, which is what impose a limit on noise performance to any CCD readout system.[16] Also meaningful was the transient simulation that allows to model the glitches and transient response of the switches, which are nonlinear phenomena that can not be captured with standard spectral noise simulations that correspond to linear circuits. The software used for simulation was LTSpice XVII® from Analog Devices® and simulation step was set to 10 ns.

### 5.2 Skipper-CCD simulation

The left plot in figure 5 shows the Power Spectra Density (PSD) of the output amplifier of the Skipper-CCD provided by designers S. Holland et al,[2] from Lawrence Berkeley National Laboratory (LBNL). This output amplifier of the CCD is a MOSFET in source follower configuration. The shape of the PSD shows the 1/f pink noise at lower frequencies and the flat or white noise at frequencies higher than 200KHz. That pink noise component at the lower part of the spectrum is that limit the noise reduction using only Dual Slope Integration (DSI).[16]

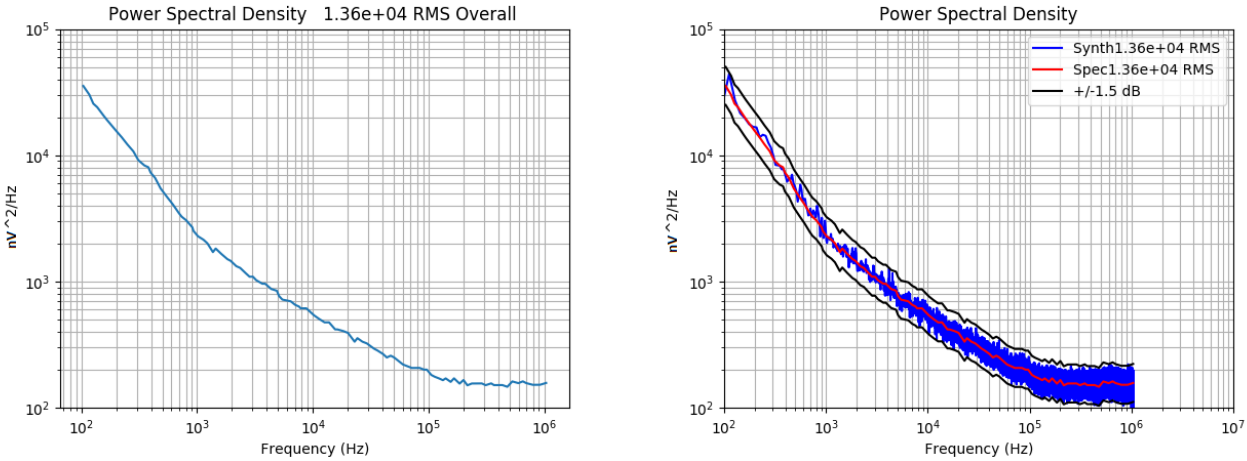


Figure 5. On the left the measured Power Spectra Density (PSD) of CCD output stage from.[2] On the right, the PSD of 4 seconds of synthesized noise (Blue) along with the the specified target PSD and +/-1.5dB verification marks (black).

A noise signal of 4 seconds was synthesized using the CCD output real PSD and the open source Signal Analysis Package GUI by Tom Irvine.[19] The plot on the right in figure 5 shows the PSD of this synthesized noise signal (blue) along with the specified target PSD (red) and ±1.5dB verification marks. This noise is added to an ideal CCD output generator to produce realistic CCD signals as shown in the schematic of figure 6 along with its output signal (video). In the center of the video signal, a pixel can be observed between two voltage dips caused by clock feedthroughs. The peak (another clock feedthrough) at the center of the image separates the pedestal or reference level from the signal level. The charge in pixels can be set to any desired values.

### 5.3 Results and noise analysis

A histogram of the simulation of a signal with 2500 pixels is shown in figure 7. 1000 pixels were set with a charge of 200 e−, the rest 1500 pixels were left with 0 e− of charge and one sample per pixel $N = 1$ (DSI equivalent). The output was converted to 18 bits values using a reference of 4.096 V as full scale to simulate the quantization noise effect introduced by an ADC. The two peaks in the histogram correspond to the groups of pixels with 0e- (left one) and 200e- of charge. They scatter around a mean value with a Gaussian distribution as expected. Then Gain in ADU/e- (ADC Units per electron) can be calculated from the distance between the mean values

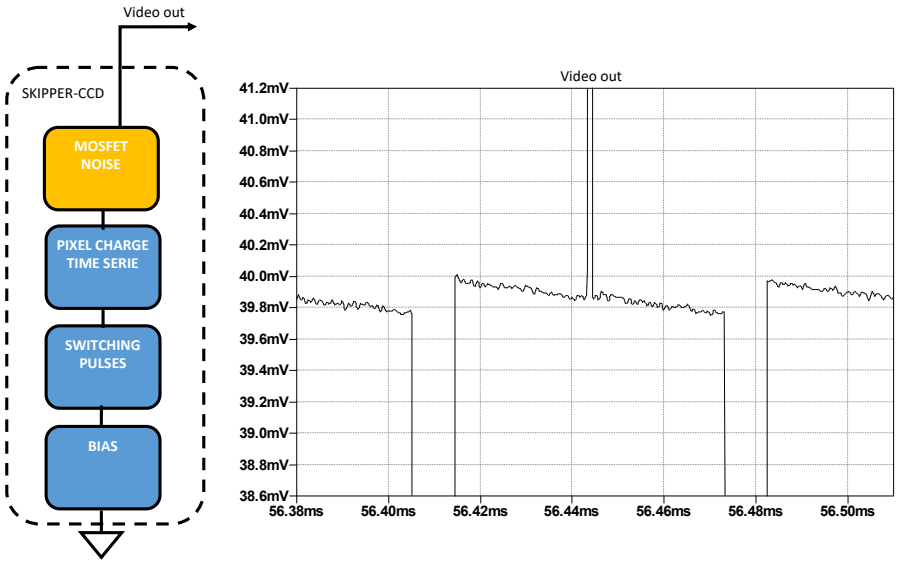


Figure 6. Schematic of the CCD signal generator with a capture of the signal for a single pixel

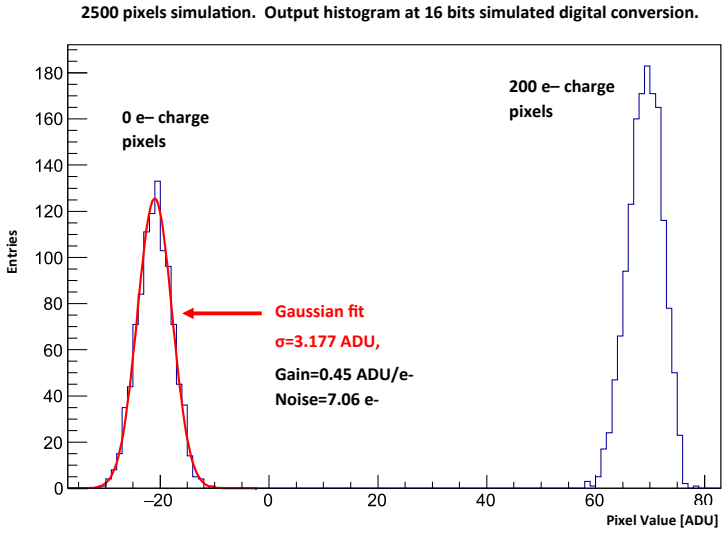


Figure 7. Histogram of the output for 2500 pixels

of the two groups

$$\text{Gain}[\text{ADU/e}-] = \frac{\overline{X}_{200e^-} - \overline{X}_{0e^-}}{200e^-}, \tag{10}$$

where, $\overline{X}_{0e^-}$ and $\overline{X}_{200e^-}$ are the mean final values of pixels corresponding to 0e− charge and 200e− charge.

the noise in e− rms (root mean square) from the standard deviation of the pixels distribution[16]

$$\text{noise[e- rms]} = \frac{\sigma_{0e-}}{\text{Gain}}, \tag{11}$$

where, $\sigma_{0e-}$ is the standard deviation of the pixels with 0e− charge in ADU.

Using equations 10 and 11 a noise scan was performed. This measures the noise ine− rms for the integration times of 5$\mu$s, 10$\mu$s, 20$\mu$s, 35$\mu$s and 55$\mu$s using one skipper sample ($N = 1$) per pixel and 1000 simulated pixel for each configuration. The results are shown in figure 8.

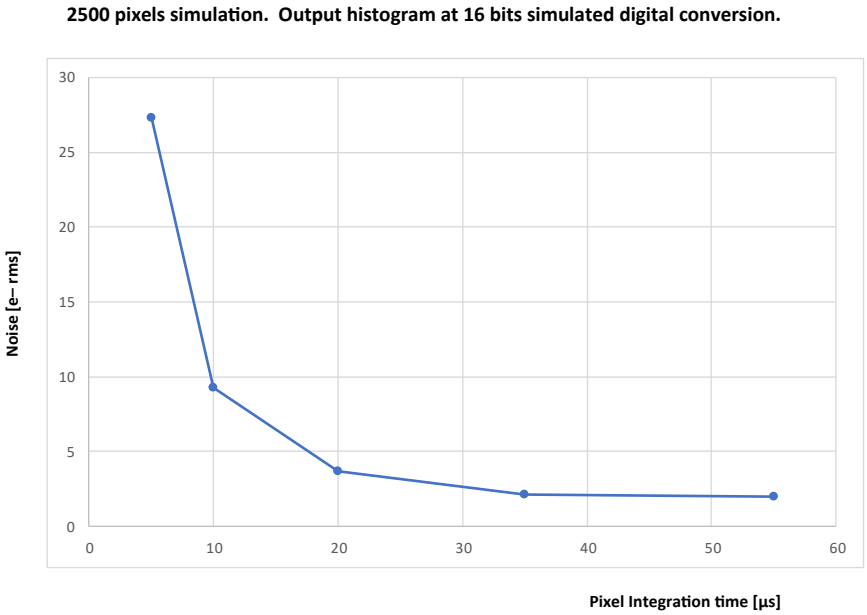


Figure 8. Noise versus pixel integration time.

The plateau in the noise scan shown in figure 8 shows that this noise reduction using one sample per pixel (DSI) has a limit as mentioned in section 2. Even for integration times above 55$\mu$s the noise levels remain at around 2e− rms.

The histogram and the noise scan results were very close to previous experimental results with other type of electronics which are not suitable for scaling up to thousands of channels.[3,16,17] The noise limit was slightly higher for experimental data, around 2.5e− rms. This comparison was used to validate the simulation before staring with the MSI mode.

Figure 9 shows the results of the last part of the noise analysis. This is a noise scan using the number of skipper samples per pixel $N$ as parameter in a range of 1 to 49 with the MSI mode of the circuit. Two integration times were used, 13.3$\mu$s and 26.6$\mu$s. The noise were reduced approximately by a factor of $\frac{1}{\sqrt{N}}$, which is seen as a straight line in the log-log plot. This is the expected noise reduction for $N$ averages of independent measurements of the same pixel charge. The plot also shows that the noise reach sub-electron levels for $N > 5$ in the case of $I_W = 26.6\mu$s and for $N > 22$ in the case of $I_W = 13.6\mu$s.

### 5.4 Power consumption considerations

Using ±5 V for all the analog stages the power consumption showed in simulation was 33mW per channel. This is considered a raw estimation, since this parameter depends heavily on the operational amplifier selected.

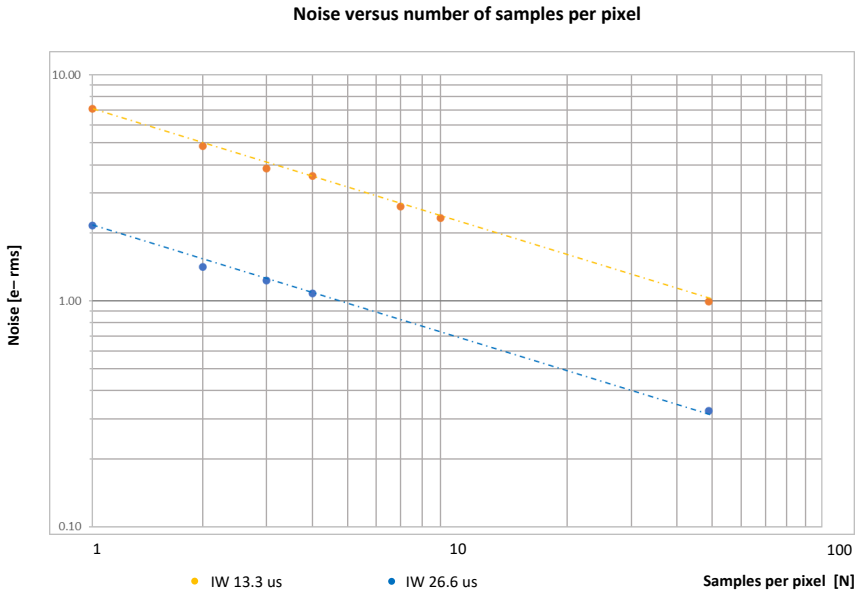


Figure 9. Noise versus number of samples per pixels for integration times of 13.3$\mu$s and 26.6$\mu$s using low gain MSI.

## 6. CONCLUSIONS

Two raw options for architectures that are compatible with a high channel density front ends were described along with their basic requirements. The analysis showed that for systems in the order of hundreds of channels using Skipper-CCDs it could be possible to reach easy scalability and less problems related to mechanical constraints if the readout electronics are integrated into the sensor package.

A circuit was proposed as an option for the integrated readout electronics. The simulation results showed evidence that it can process Skipper-CCD signals and reduce the noise to sub-electron levels while saving storage and bandwidth by a factor equal to the number of samples per pixel selected. This is despite the non-ideal characteristic of analog switches and tolerance errors of passive components. It also meets the requirement of low complexity and low power needed in a high channel density front-ends.

The noise levels obtained in simulation were coherent with previously obtained experimental data. This means that this method is valid to test options for different readout circuits, filters or pixel computation techniques. The reason behind the slightly lower noise levels in simulation could be that this work just covered a limited band of the Skipper-CCD PSD and exclude components noise contribution to avoid excessive simulation times. A more realistic simulation with the full PSD and all the noise contributors can be set for further study.

After these results, a hardware implementation of the readout circuit proposed is being built for testing with Skipper-CCDs at Fermi National Accelerator Laboratory.

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