

Generalised predictive current-mode control of passive front-end boost-type converters

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Abstract

In this work, an average current-mode control strategy based on a generalised predictive control formulation for passive front-end three-phase boost-type converters is proposed. A novel design procedure for the generalised predictive control strategy is introduced which considers both the cost function and disturbance model as design parameters to set the controller's dynamic response and robustness against component variations. A maximum robustness criterion was used for achieving stability up to a 70% inductance reduction with maximum possible bandwidth. The proposed strategy was compared against both a PI and a predictive deadbeat average current-mode control using both simulations and experimental results on a 2-kW converter. The generalised predictive control presented less performance variations between different operating points than the PI controller. Also, the proposed strategy is more robust than the predictive deadbeat strategy, showing a better transient response with a 50% inductance reduction and remained stable for a 71% inductance reduction, while the predictive deadbeat could not. Finally, the proposed strategy achieved a 1.4% output voltage load transient response for a 595 W load power step, and a 2.8% output voltage line transient response for a 100 V input voltage step, outperforming existing state-of-the-art strategies.

1 | INTRODUCTION

In distributed three-phase AC power generation systems such as wind turbines, the generator AC voltage can be converted to DC voltage through a DC bus, from which a voltage source inverter (VSI) can inject power to the grid. This AC/DC conversion can be made using a passive front-end (PFE) three-phase boost-type converter, which consists of a three-phase diode rectifier connected to a DC/DC boost converter [1]. Even though the obtained input power factor is lower than with its active front-end (AFE) counterpart, PFE converters represent a simple, low cost and efficient way to extract power from the source [2]. They are also considered more reliable than AFE converters, reason by which some wind turbine manufacturers use them for their products [3].

As the diode rectifier is an uncontrollable part of the system, PFE converter control can only be achieved by acting on the DC/DC boost converter switch. This converter can be operated in Continuous Conduction Mode (CCM), Discontinu-

ous Conduction Mode (DCM) [4], Critical Conduction Mode (CRM) [5], and Mixed Conduction Mode (MCM) [6]. CCM implies that input current is not allowed to be zero in steady-state. DCM implies that input current is allowed to be zero for a given time in each switching period. CRM implies that input current is allowed to be zero only at the negative peaks of the switching waveform. Finally, MCM implies that the converter can operate in both CCM and DCM. Although each of the aforementioned modes has each its advantages, in high-power applications, this converter is best operated in CCM [7].

Many control strategies can be applied to the converter, which can be classified into voltage-mode control (VMC) [8] and current-mode control (CMC) strategies. VMC uses a single loop with an associated compensator to achieve the desired output voltage setpoint. However, because the input-to-output voltage transfer function presents right-half-plane (RHP) zeros, bandwidth is restricted. On the other hand, CMC consists of an inner current control loop whose setpoint is commanded by the control signal of an outer voltage loop; it has several

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advantages such as a straightforward voltage control loop design, fast dynamic response, inherent line feedforward, good line regulation, automatic overload, and short-circuit protection [9]. Therefore, the inner current loop should have the maximum dynamic response possible to guarantee that the current setpoint imposed by the slower outer voltage loop is achieved in the minimum possible time, allowing to neglect the current loop transfer function in the voltage loop control design. Another important aspect to consider is its robustness, as it extends the stable operation of the system by making it insensitive to parameter variations or model mismatch. Finally, its performance should be similar for every operating point of the system.

At present, there are several CMC strategies for DC–DC boost converters which can be classified into ripple current-mode control (RCMC) [10], constant-on [11] or off-time [12, 13] current-mode control (COTCMC), and average current-mode control (ACMC). The RCMC strategies use the instantaneous values of the input current ripple, such as the peaks or valleys, as the feedback variables for the current control loop. They present the disadvantage of sub-harmonic oscillations without proper compensation techniques. COTCMC strategies set a constant on or off time of the converter switch, using the off or on times as control variables, respectively. This results in variable frequency switching frequency. These strategies present a fast transient response, as RCMC strategies, but do not require a compensation ramp. However, as they present variable switching frequency, they cause electromagnetic interference (EMI) problems [12]. Finally, ACMC strategies use the average value of the input current in a switching period, calculated either by analog or digital filtering, as the feedback variable for the current control loop. They make use of a pulse-width-modulation (PWM) module which guarantees a fixed switching frequency and simplifies control hardware.

An ACMC can be implemented using analog techniques [14], but its performance relies heavily on the component tolerances and aging. On the contrary, digital ACMCs present less performance variation over time than their analog counterparts. Digital predictive deadbeat (PDB) [15, 16], proportional-integral-derivative (PID) [17, 18], PI with Clegg integrators (PI+CI) [19], and state-space-based [20] ACMC strategies have been proposed. The PDB-based strategies calculate the optimal duty cycle of the switch for the next switching period to minimise the error between the input current reference and measured average values. This calculation relies on a model of the converter to predict the future input current average value. The PID-based strategies yield the control input as a sum of proportional, integral, and/or derivative terms of the error between the input current reference and measured average values. The PI+CI is similar to the PID-based strategies, but it does not use a derivative term of the error and includes an additional Clegg integrator which is a resettable integrator, to avoid the effects of the second-order response typical of such controllers. Finally, state-space-based strategies use a state-space representation of the system and, using a state-feedback procedure, place the poles of the closed-loop system in the desired frequencies, given that the system is controllable. The PID-based and the state-space-based ACMC make use of a linear model of the system and seek to achieve closed-loop stability, but their performance

depends on the system operating point unless some feedback linearisation strategy is used [18]. On the contrary, the PI+CI strategy performance is independent of the system operating point but it presents a slow dynamic response. Finally, the PDB strategy obtains the maximum dynamic response, and its performance is independent of the system operating point. However, its main drawback is a high sensitivity to model mismatch.

Based on the limitations of the mentioned digital ACMC strategies, model predictive control (MPC) could be a proper alternative, as it can deal with multiple control objectives simultaneously [21]. MPC strategies could be classified into finite-control-set (FCS) [22] and continuous-control-set (CCS) [23] families. Both strategies make use of a system model to predict the states' trajectories, and also of a cost function which can optimise error, control input magnitude, and other terms by applying the proper control input sequence. In the case of FCS–MPC strategies, the number of control input values is limited, but the optimisation procedure must be carried out in real time, that is, it is an online optimisation procedure [24]. This optimisation gets more computationally demanding as the prediction horizon is increased. Additionally, in the case of switching converters, the resulting control signal is used to drive converter switches directly, which leads to variable switching frequency. This can be somewhat mitigated if a switching frequency weight term is included in the cost function [25]. Conversely, on CCS–MPC strategies, the number of control input values is virtually infinite, that is, a continuous control input can be applied to the controlled plant. Moreover, by using a PWM module, the switching frequency is fixed, keeping the converter at its optimal power efficiency point.

A particular CCS–MPC strategy known as generalised predictive control (GPC) [26] has been applied recently in wind energy systems [27] and speed control of permanent magnet synchronous motors (PMSG) [28]. It is different from other MPC strategies because it relies on a transfer function model of the system; the model includes a filtered disturbance polynomial acting as an observer, with its coefficients defining its gain. This particular difference improves control system immunity to measurement noise. Also, it uses a cost function with quadratic error and control dynamics terms, which allows an offline optimisation procedure if no constraints are included in the formulation. This has the advantage of obtaining a computationally efficient fixed-coefficients control law avoiding the intensive processing needed in online optimisation procedures. However, neither the disturbance polynomial nor the cost function design has an analytical procedure, but they are based on the application-specific demands instead. Several variants have been proposed such as the fast GPC [29], fuzzy GPC [30], and neural networks based GPC [31]. The fast GPC is a microcontroller-based implementation that uses a time series model instead of the Diophantine equation formulation, achieving less computational burden with increasing prediction and control horizons. The fuzzy GPC uses a fuzzy model and the neural networks based GPC uses an artificial neural network model to manage highly non-linear plants. Regarding its application in power electronic converters, it has proven to be fast and robust as inner current control compensator of grid-connected voltage source inverters with

both L [32] and inductor-capacitor-inductor filters [33], where a cost function design procedure was provided, and an anti-wind-up algorithm was added to include the control input constraint without the need for online optimisation, keeping computational complexity low. In the aforementioned works, the cost function was considered as the only control design parameter to obtain the best control system robustness and bandwidth trade-off possible. However, the disturbance model, which is another possible design parameter, was not taken into account.

Therefore, in this work, a digital GPC-based ACMC strategy for PFE three-phase boost-type converters is proposed. To further improve the performance of the GPC strategy, a novel two-degree-of-freedom GPC design procedure is presented, considering both the cost function and the disturbance model as design parameters, obtaining a better trade-off between dynamic response and robustness against model mismatch than in previous works. The proposal is first evaluated considering its performance variation with different converter operating points, and compared with that of a PI ACMC. Then, its robustness is assessed by both sensitivity analysis and experimental results and compared with that of a PDB ACMC strategy. Output voltage line and load transient responses are also measured. Finally, a quantitative comparison of the proposal with the state-of-the-art control strategies is given.

The main contributions of this work are: (1) a novel ACMC for a PFE three-phase boost-type converter based on a GPC strategy is proposed which presents similar performance with converter operating point and robustness against model mismatch as its main distinguishing features; (2) a novel two-degree-of-freedom GPC design procedure is also introduced where it is shown that not only the cost function, but also the disturbance polynomial model has an effect on both dynamic response and robustness, and (3) the effect of adding an anti-wind-up (AWU) algorithm to the GPC strategy is also analysed for the first time, highlighting its importance to keep the closed-loop operation of the system at all times.

The work is organised as follows: first, in Section 2, the proposed GPC-based inner current control loop design is explained. The design process includes the formulation of the input current model for the PFE three-phase boost-type converter, and the two-degree-of-freedom GPC design procedure is explained. Then, in Section 3, application details of the proposed control strategy related to its digital implementation are given, and Section 4 includes simulation and experimental results, and a comparison with existing results taken from state-of-the-art control strategies is also given. Finally, in Section 5, conclusions arising from this work are discussed, and the main advantages of the proposed GPC ACMC strategy are highlighted.

2 | CURRENT CONTROLLER DESIGN

2.1 | Input current model

The PFE three-phase boost-type converter is shown in Figure 1. The grid-connected VSI is modelled as a current source i_o con-

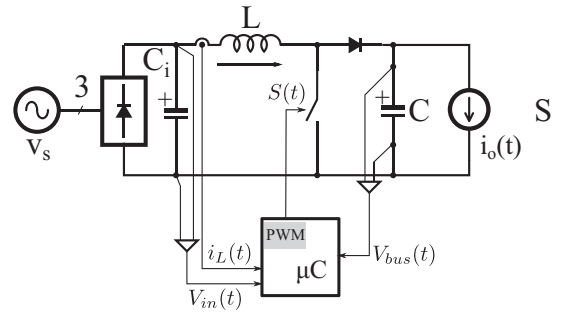


FIGURE 1 Digitally controlled PFE three-phase boost-type converter

nected to the DC bus of capacitance C at a voltage v_{bus} . The converter switch S uses an electronic driver to generate the voltage and current needed to change its state. The control system uses input current and both input and output voltage measurements to generate the control action to be applied to the converter. Input capacitor C_i filters the three-phase AC rectified voltage v_{in} , to minimise input voltage ripple. Input current i_L is extracted from the generator through the inductance L .

The model to be used for ACMC can be obtained considering the inductor current differential equation

$$\frac{di_L(t)}{dt} = \frac{v_{in}(t) - u(t)}{L}, \quad (1)$$

where $u(t) = v_{bus}(t)(1 - s(t))$ and $s(t)$ is the switching function of the boost switch. When using a PWM module, $\bar{s}(t) = d(t)$, where $d(t)$ is the duty cycle applied to the switch. Therefore, $\bar{u}(t) = \bar{v}_{bus}(t)(1 - d(t))$ and

$$\frac{d\bar{i}_L(t)}{dt} = \frac{\bar{v}_{in}(t) - \bar{u}(t)}{L}, \quad (2)$$

which is the model of the average current through the inductor. Defining $\bar{u}^*(t) = \bar{v}_{in}(t) - \bar{u}(t)$ as the control input, then, using the Laplace transform, the control-input to inductor-current transfer function (TF)

$$G_i(s) = \frac{\bar{I}_L(s)}{\bar{U}^*(s)} = \frac{1}{sL} \quad (3)$$

is obtained.

2.1.1 | Discrete-time model

To use a discrete-time domain controller, an anti-aliasing (AA) filter is needed [34]. The simplest form for an AA filter is

$$G_f(s) = \frac{1}{1 + \frac{s}{s_0}}, \quad (4)$$

where $s_0 = 2\pi f_0$ and f_0 is the 3-dB bandwidth frequency. To give the predictive control a more accurate model of the system,

the AA filter transfer function is included in the plant model, resulting in

$$G_{ii}(s) = G_i(s) \times G_f(s). \quad (5)$$

To use the system model in a discrete-time control system, the previous transfer function needs to be transformed to the discrete-time domain. Using a zero-order hold on the control input and a sampling period T_s , the resulting discrete-time transfer function is

$$G_{ii}(z^{-1}) = \frac{\sum_{i=2}^3 b_i z^{-i}}{1 + \sum_{i=1}^2 a_i z^{-i}} = z^{-1} \frac{B(z^{-1})}{A(z^{-1})}, \quad (6)$$

where b_i and a_i depend on both the L and AA filter values. It is worth noting that even though the discrete transfer function denominator has the same order as its continuous counterpart, the numerator index starts at $i = 2$, including an additional unit delay to the discrete transfer function which represents the ACMC delay.

2.2 | GPC design

A design procedure for the GPC strategy was previously given in [32, 33], where the optimal value of the control increment weighting factor λ was calculated to obtain the best control system robustness and bandwidth trade-off possible. However, we propose a new design procedure with two degrees of freedom where, as we will show next, a better trade-off can be obtained by also including the disturbance model polynomial coefficient c_2 as a design parameter.

The GPC formulation is based on a Controlled Auto-Regressive and Integrated Moving-Average transfer-function model which has the form:

$$A(q^{-1})\Delta y(k) = q^{-d}B(q^{-1})\Delta u(k) + C(q^{-1})v(k), \quad (7)$$

where q^{-1} is the unit delay operator in the discrete-time domain, $y(k)$ is the controlled variable, $u(k)$ is the controlled plant input, $v(k)$ is an immeasurable disturbance signal and $\Delta = 1 - q^{-1}$ is the discrete differentiation operator. Assuming that the coefficients of $A(z^{-1})$ and $B(z^{-1})$ are equal to the coefficients of $A(q^{-1})$ and $B(q^{-1})$, the obtained plant model can be used for the GPC design procedure. Also, d is the number of additional discrete delays of the model, not included in $B(q^{-1})$, which considering the model (6), results in $d = 1$. Finally, $C(q^{-1})$ is a disturbance model polynomial which sets the dominant eigenvalues of the GPC inherent observer. Considering a minimum-order disturbance term,

$$C(q^{-1}) = q^{-1} - c_2 q^{-2} \quad (8)$$

reflecting the fact that $y(k)$ is affected solely by $v(k-1)$ and $v(k-2)$, and the dominant eigenvalue is set in $z_d = c_2$. As will

be shown later, the location of this eigenvalue affects the GPC behaviour both in terms of robustness and disturbance rejection capability, consequently requiring a careful selection process, which was not considered in previous works.

Another design requirement for a GPC strategy regards setting its cost function parameters. The GPC cost function $V(k)$ is

$$V(k) = \sum_{i=H_w}^{H_p} [\hat{y}(k+i|k) - r(k+i)]^2 + \sum_{i=0}^{H_c-1} \lambda [\Delta \hat{u}(k+i|k)]^2, \quad (9)$$

where H_w is the initial prediction sample instant, H_p is the prediction horizon length, H_c is the control horizon length, r is the reference trajectory and λ is the control increment weighting factor. The argument $(k+i|k)$ means that the prediction of the variable at time $k+i$ is calculated at time k . The first term of the cost function weighs the error for each step over the prediction window in the optimisation procedure and the second term weighs the rate of change of the control input over the control window. The cost function weight relationship between both terms is set by λ , affecting controller behaviour.

After defining the model and the cost function parameters, the GPC controller is obtained by optimisation through solving

$$\frac{\partial V(k)}{\partial \Delta \hat{u}(k+i|k)} = 0 \quad (10)$$

for $\Delta u(k)$ which results in

$$\Delta u_{\text{opt}}(k) = K_{GPC} \mathcal{E}(k) \quad (11)$$

$$\mathcal{E}(k) = T(k) - \Psi \hat{x}(k|k) - Y u(k-1), \quad (12)$$

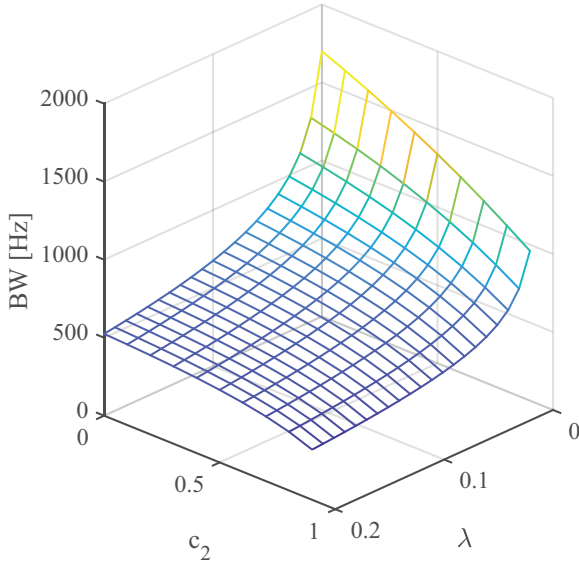
where K_{GPC} is a vector of constant elements, $\mathcal{E}(k)$ is the error sequence, $T(k)$ is the setpoint sequence, $\Psi \hat{x}(k|k)$ is the system free-response up to H_p based on the actual state estimation and $Y u(k-1)$ is the system forced response up to $H_c - 1$ based on the last control input applied. Then,

$$u_{\text{opt}}(k) = u(k-1) + \Delta u_{\text{opt}}(k). \quad (13)$$

In the absence of system constraints, the GPC optimisation problem can be solved offline and is similar to an infinite-horizon linear quadratic regulator (LQR), assuming sufficiently long $H_p - H_w$ and H_c [35]. This has the advantage of reduced computational cost in comparison with online optimisation algorithms. Usually, $H_w = d + 1$ and $H_c \leq H_p$ to further minimise computations. For the ACMC application presented in this work, $H_w = 2$, and because the controller acts sample-wise, the same control and prediction horizons are chosen for the

TABLE 1 List of system parameters

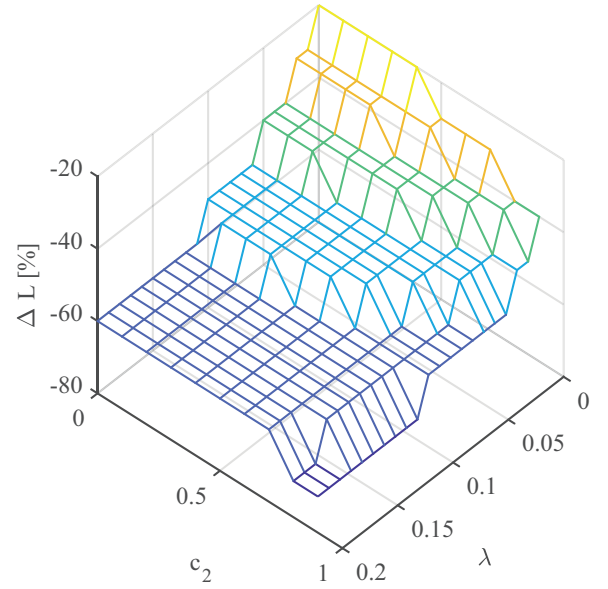
Parameter	Value
Nominal DC-Bus Voltage V_{bus}	800 V
Nominal Input Voltage V_{in}	400 V
Maximum Output Current I_o	8.25 A
Switching frequency f_{sw}	10 kHz
Sampling frequency f_s	30 kHz
Input Inductance L	6.14 mH
Output Capacitance C	470 μF
AA filter 3-dB bandwidth frequency f_0	4.5 kHz

**FIGURE 2** Relationship between λ , c_2 and bandwidth

optimisation, that is, $H_p = H_c$. For the system model in question, $H_p - H_w = H_c - H_w \geq 19$ could be considered infinite because no significant differences were found in the resulting control law, regardless of the chosen disturbance model or cost function.

As previously stated, the inner current control loop should have the maximum dynamic response possible and robustness against model-mismatch. The maximum dynamic response possible can be obtained by maximising the control system bandwidth and robustness can be determined by analysing the controller performance in the event of inductance variation. In [32, 33], it was shown that there is a trade-off between bandwidth and robustness considering λ as the only design parameter. However, the design provided in those references did not consider that the disturbance model polynomial coefficient c_2 could also be used as a GPC design parameter, as it will be shown next.

Using simulations, the relationship between λ , c_2 , and BW for the system described by parameters shown listed in Table 1 is shown in Figure 2. Simulations included in this work were carried out using circuit simulation software NL5 [36].

**FIGURE 3** Relationship between λ , c_2 and maximum inductance variation

The maximum value of $c_2 = 0.9 < 1$ guarantees observer stability. As can be seen, by increasing both c_2 and λ , system bandwidth gets lower. There is no lower bound in the bandwidth criterion for the GPC design. However, considering that a CMC strategy is used, lowering the current control loop bandwidth imposes a lower bandwidth for the outer voltage control loop, given the fact that the inner loop should be much faster than the outer loop. This figure suggests that in order to maximise system bandwidth, (λ, c_2) should be $(0,0)$. Nevertheless, that choice of GPC parameters has the disadvantage of reduced system robustness as shown in Figure 3, where the maximum inductance variation ΔL is plotted as a function both λ and c_2 . The design goal chosen is to maximise current loop robustness against inductance variations. Therefore, with $(\lambda, c_2) = (0.18, 0.8)$, the resulting bandwidth is $BW = 389.5$ Hz and the maximum inductance reduction is $\Delta L = -70\%$. With this selection, the resulting GPC transfer function $G_{GPC}(\tilde{z}^{-1})$ can be obtained as

$$G_{GPC}(\tilde{z}^{-1}) = \frac{u_{opt}(\tilde{z}^{-1})}{e_i(\tilde{z}^{-1})} = \frac{\sum_{i=0}^2 b_i \tilde{z}^{-i}}{1 + \sum_{i=1}^3 a_i \tilde{z}^{-i}}, \quad (14)$$

where $e_i(\tilde{z}^{-1})$ is the error between the input current setpoint and the actual input current in the \tilde{z} domain, with the coefficients shown in Table 2.

In this two-degree-of-freedom GPC design process, bandwidth and robustness surfaces were obtained as a function of both λ and c_2 , which can be considered a more general case of the previous design proposed in [32, 33] where only λ was used as a design parameter, with an arbitrary c_2 value, that is, a single bandwidth versus robustness curve was obtained. Therefore the proposed two-degree-of-freedom design process represents a clear improvement as it has the advantage of providing additional bandwidth versus robustness trade-off possibilities.

TABLE 2 List of GPC transfer function coefficients

Coefficient	Value	Coefficient	Value
b_0	10.52	a_1	-1.381
b_1	-10.19	a_2	0.424
b_2	0.566	a_3	-0.0426
b_3	7.409×10^{-7}		

3 | CONTROL IMPLEMENTATION

The control system block diagram is shown in Figure 4. As can be seen, each of the acquired variables is passed through a low-pass filter such as the ones described in Section 2.1.1 whose pole frequency f_0 can be set near the switching frequency f_{sw} using an oversampling technique. These techniques allow the inclusion of a digital filter to reduce the switching frequency components in the current measurement waveforms used in the control system. This is achieved by setting the sampling frequency f_s as an integer multiple of the switching frequency, that is, $f_s = N \times f_{sw}$.

The input current contains a switching sawtooth waveform which requires a considerable amount of filtering to decrease its aliasing effect on the current control loop. Likewise, output voltage ripple is a function of the current ripple magnitude and capacitors' ESR. Using a notch finite impulse response (FIR) filter at the switching frequency results in a greater attenuation than using only the AA filter alone. Besides, even if it adds a phase shift at the notch frequency, the control cutoff frequency is at least a decade lower keeping the phase margin unaltered. Both filtered variables are sampled using a sample and hold circuit and applying an oversampling strategy with $f_s = 30$ kHz allows that $f_0 = 4 - 5$ kHz without measurable aliasing.

A notch FIR digital filter of the form

$$\bar{x}(k) = \frac{1}{N} \sum_{i=-\frac{N-1}{2}}^{\frac{N-1}{2}} x(k+i) \quad (15)$$

can be used, where N is an odd integer number of samples, to have the same forward and backward samples of the moving

average window. As can be seen, the filter is non-causal so a modification is needed to make possible its realisation. For $N = 3$, the modified FIR filter has the form in the z domain [32]

$$H_{FIR}(z^{-1}) = \frac{2}{3} + \frac{1}{3}z^{-1} + \frac{1}{3}z^{-2} - \frac{1}{3}z^{-3}, \quad (16)$$

where a linear extrapolation was used to estimate the current sample.

In the case of the input voltage v_{in} measurement, as it does not contain a high-frequency switching waveform, it is filtered using an additional digital infinite impulse response (IIR) filter to avoid sensor noise affecting the duty cycle calculation. The IIR filter has the form

$$\bar{x}(k) = b_0x(k) + a_0\bar{x}(k-1), \quad (17)$$

where a_0 defines the location of the pole in the z -plane and $b_0 = 1 - a_0$.

The duty cycle calculation block implements the function

$$d(k) = 1 - \frac{v_{in}(k) - u_{GPC}(k)}{v_{bus}(k)}. \quad (18)$$

This frees the controller from dealing with the inherently non-linear nature of the converter, and its performance is similar in every operating point of the controlled system. The PWM modulation signal is indirectly synchronised with the ADC timer and updated every three sampling periods obtaining a switching frequency $f_{sw} = f_s/3$.

The available input voltage v_{in} and output voltage v_{bus} impose a constraint in the current loop control signal, which could lead to integral wind-up and duty cycle saturation. In online optimisation GPC strategies, this constraint could be included and the optimal control signal could be calculated avoiding integrator saturation. However, in offline optimisation GPC strategies, this problem can be solved by adding an anti-wind-up algorithm as in [33]. Therefore, as the current-control GPC block contains the transfer function (14) which has integral action, an additional current anti-wind-up (AWU_i) algorithm was added. It saturates the GPC block control output to

$$u_{GPC\text{-max}}(k) = v_{in}(k) \quad (19)$$

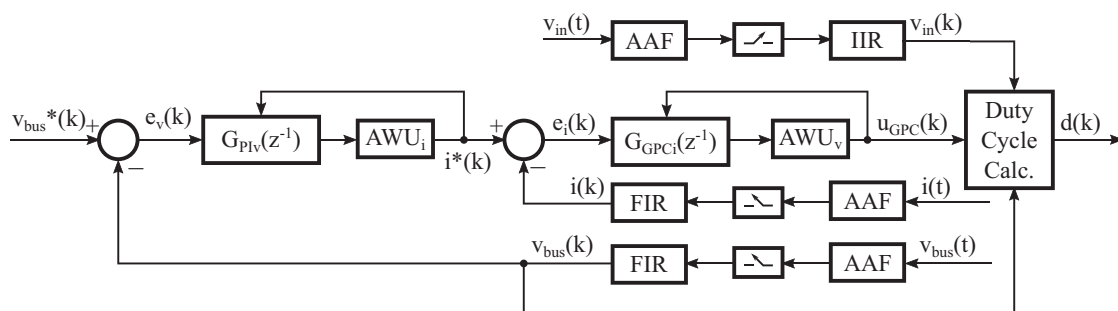


FIGURE 4 Proposed control system block diagram. AAF = Anti-Aliasing Filter, AWU_i , current anti-wind up; AWU_v , voltage anti-wind up; FIR, finite impulse response; IIR, infinite impulse response

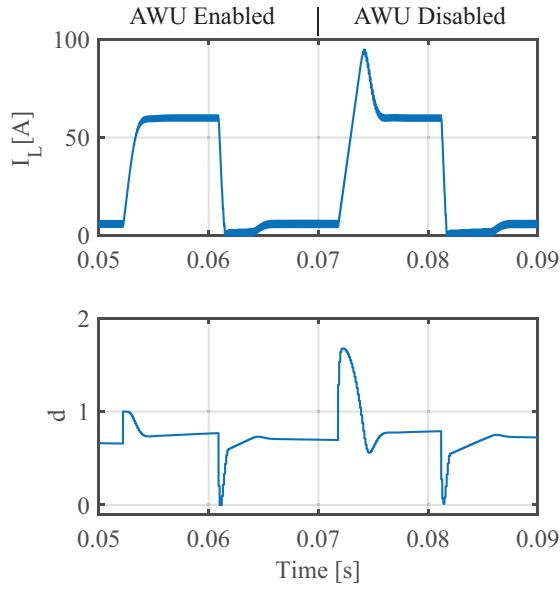


FIGURE 5 Input current (top) and duty cycle (bottom) waveforms with commanded step from 6 A to 60 A, showing the effect of the AWU_i algorithm

$$u_{GPC_{min}}(k) = v_{in}(k) - v_{bus}(k) \quad (20)$$

and feeds back this value to the control law difference equation, realigning it with the applied voltages, which guarantees the closed-loop operation of the control system at all times. This effect is shown in Figure 5. As can be seen, when the AWU block is enabled, the duty cycle d is constrained to its limits, that is, $0 \leq d \leq 1$, and the input current waveform follows its setpoint without any overshoot. On the contrary, when it is disabled, $d > 1$ from $t = 71.8$ ms to $t = 73.9$ ms, which results in a significant current overshoot, due to the loss of closed-loop operation.

The voltage-control PI block is designed considering that its bandwidth is much lower than the current control loop bandwidth. For a $BW = 5$ Hz, and considering a $PM \geq 45^\circ$, results in a PI controller of the form

$$G_{PIv}(z^{-1}) = \frac{0.01082 - 0.01079z^{-1}}{1 - z^{-1}}. \quad (21)$$

The model used for designing the voltage loop is explained in the Appendix.

4 | RESULTS

For obtaining the experimental results, the proposed strategy was tested in a prototype of a PFE three-phase boost-type converter, which uses a Semikron SKM75GB128D IGBT module, an array of aluminium capacitors obtaining $470 \mu F$ of output capacitance, and an array of aluminium and film capacitors obtaining $2260 \mu F$ of input capacitance. The digital control framework comprises a custom board based on a

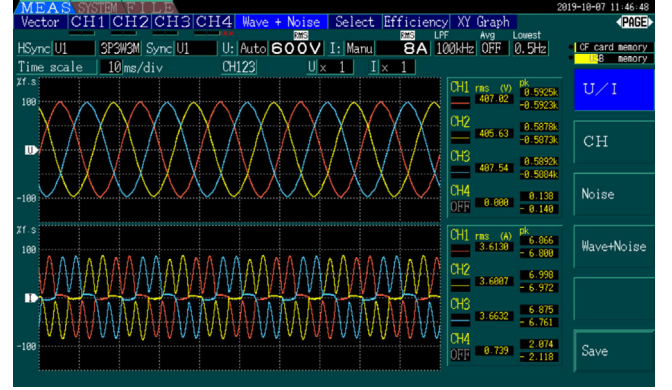


FIGURE 6 Three-phase AC voltages (top) and currents (bottom). $v_{in} \approx 300$ V_{DC}, $R_{load} = 210 \Omega$, $v_{bus} = 600$ V_{DC}

Freescale KV31 floating-point digital signal controller which has an embedded digital signal processor running at 120 MHz, a PWM module, and a 12-bit ADC. The remaining system parameters are as stated in Table 1.

The PFE converter was connected to a 3×380 V_{RMS}, 50 Hz utility grid. Line voltages and current waveforms, obtained using a three-phase power analyzer, are shown in Figure 6, for $v_{in} \approx 300$ V_{DC}, $R_{load} = 210 \Omega$, and $v_{bus} = 600$ V_{DC}. The input voltage was reduced using a variable auto-transformer. As can also be calculated from the figure, the input active power was $P_{in} \approx 1.7$ kW and the apparent power was $S_{in} \approx 2.4$ kVA.

4.1 | Performance variation with operating point

The proposal performance variation with the operating point of the system was compared to that of a digital PI ACMC strategy, which is its main drawback [18]. The digital PI ACMC was designed using the Ziegler–Nichols method for $V_{in} = 150$ V, $V_{bus} = 300$ V, and $R_{load} = 210 \Omega$, resulting in $K_p = 0.162$ and $T_i = 3.84$ ms. With these constants, the digital ACMC PI compensator has the form

$$D(z) = \frac{0.188 - 0.162z^{-1}}{1 - z^{-1}} E(z), \quad (22)$$

where $D(z)$ and $E(z)$ are the duty cycle and current error in the z -domain, respectively.

To assess performance variation with the operating point of the system, a series of current setpoint steps were commanded for both strategies, and the resulting transient responses are shown in Figures 7(a)–8(c). Figure 7(a)–(c) corresponds to the GPC strategy while Figure 8(a)–(c) corresponds to the PI strategy. Figures 7(a) and 8(a) show the transient response of both strategies when a 1 A step is commanded while $i_L = 1$ A. The transient response for a 2 A step, while $i_L = 2$ A, is shown in Figures 7(b) and 8(b), and while $i_L = 4$ A, in Figures 7(c) and 8(c).

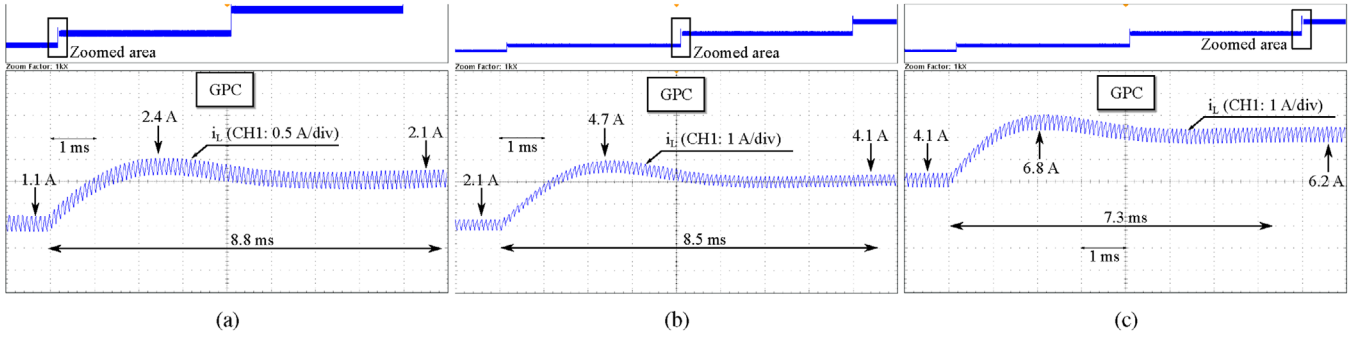


FIGURE 7 Inductor current with overshoot and settling time information included for the GPC strategy. $V_{in} = 60 \text{ V}$, $R_{load} = 210 \Omega$. (a) 1 A step is commanded while $i_L \approx 1 \text{ A}$. (b) 2 A step is commanded while $i_L \approx 2 \text{ A}$. (c) 2 A step is commanded while $i_L \approx 4 \text{ A}$

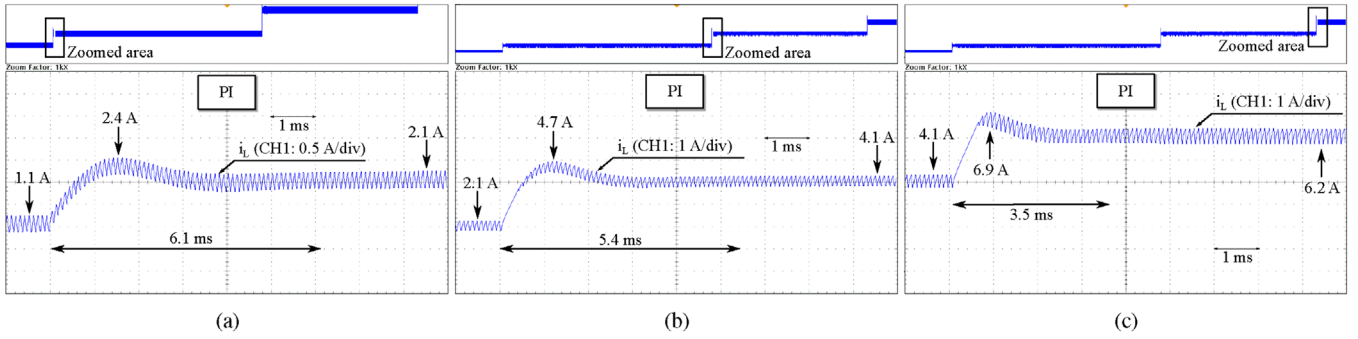


FIGURE 8 Inductor current with overshoot and settling time information included for the PI strategy. $V_{in} = 60 \text{ V}$, $R_{load} = 210 \Omega$. (a) 1 A step is commanded while $i_L \approx 1 \text{ A}$. (b) 2 A step is commanded while $i_L \approx 2 \text{ A}$. (c) 2 A step is commanded while $i_L \approx 4 \text{ A}$

Even though some differences can be seen directly from the oscilloscope captures, they were quantified by comparing their closed-loop pole location. From each of the step responses, a closed-loop second-order approximation of the form,

$$T(s) = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad (23)$$

was calculated by considering

$$\xi = \frac{\ln OS}{\sqrt{\pi^2 + \ln^2 OS}} \quad (24)$$

$$\omega_n = \frac{4}{ST_{2\%}\xi}, \quad (25)$$

where $OS = i_{L_{max}}/\Delta i_L^*$ is the transient response overshoot and $ST_{2\%}$ is the settling time with 2% tolerance. Both parameters were calculated from the average current value in each switching period. The resulting pole location for each $T(s)$ approximation is shown in Figure 9. As can be seen, the GPC strategy presents much less pole location variation than the PI strategy for the same tests. In quantitative terms, the PI presented closed-loop system poles with $\Delta\sigma \approx 490 \text{ rad/s} \approx 78 \text{ Hz}$ and $\Delta\omega \approx 1860 \text{ rad/s} \approx 296 \text{ Hz}$ while the proposed strategy kept $\Delta\sigma \approx 94 \text{ rad/s} \approx 15 \text{ Hz}$ and $\Delta\omega \approx 283 \text{ rad/s} \approx 45 \text{ Hz}$.

4.2 | Robustness

Robustness of the proposal was compared to that of a digital PDB APMC strategy [16] because it features the same performance regardless of the operating point and optimal dynamic response, but it presents high sensitivity to model mismatch.

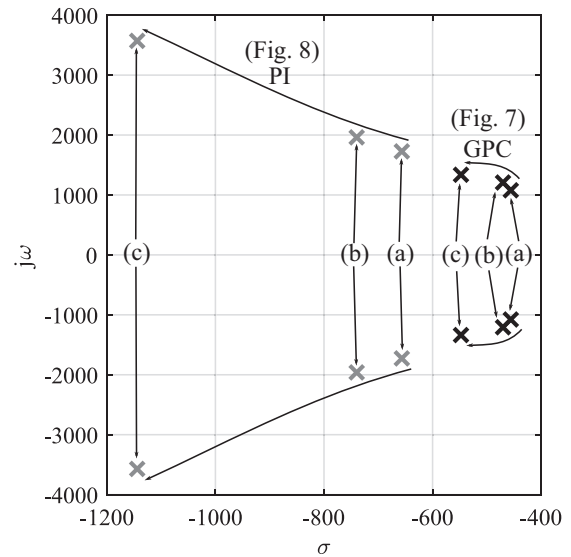


FIGURE 9 Closed-loop pole location in the s plane for Figures 7(a)–8(c)

The PDB strategy relies on the exact plant knowledge and calculates the duty cycle by considering a zero-order-hold (ZOH) in the control input as

$$d(k+1) = 1 - \frac{L}{v_{\text{bus}}(k)T_s} (i_L(k) - i_L^*(k)) - \frac{v_{\text{in}}(k)}{v_{\text{bus}}(k)}. \quad (26)$$

However, as can be seen in the previous equation, if the model inductance L differs from the real value, controller stability could be compromised.

The sensitivity function $S(j\omega)$ was calculated for both the GPC and the PDB strategy to compare their robustness against system variations. Even though the PDB is a non-linear strategy acting directly on the duty cycle, it can be considered a P controller when applying exact feedback linearisation [37]. By rearranging terms, (26) can be written as

$$d(k+1) = 1 - \frac{v_{\text{in}}(k) - L/T_s (i_L^*(k) - i_L(k))}{v_{\text{bus}}(k)}. \quad (27)$$

Comparing (27) with (18), an equivalent linear control input can be defined as

$$u_{\text{PDB}}(k) = \frac{L}{T_s} (i_L^*(k) - i_L(k)) = \kappa_{\text{PDB}} e_i(k), \quad (28)$$

where $\kappa_{\text{PDB}} = L/T_s$ is the proportional gain of the equivalent P controller. With this consideration,

$$S_{\text{GPC}} = \frac{1}{1 + G_{\text{GPC}} G_{ii}}, \quad (29)$$

$$S_{\text{PDB}} = \frac{1}{1 + \kappa_{\text{PDB}} G_{ii}}, \quad (30)$$

where S_{GPC} and S_{PDB} are the sensitivity functions of the GPC and the PDB strategies, respectively, and are shown in Figure 10.

As can be seen,

$$|S_{\text{GPC}}|_{\text{max}} < |S_{\text{PDB}}|_{\text{max}} \quad (31)$$

and, therefore, the GPC strategy can be considered more robust than the PDB strategy against system variations.

Simulations were carried out for analysing both strategies' performance when changing the inductance to 50% of the value used for the control design, as stated in Table 1. According to the robustness criterion used for the GPC current loop design procedure, it should remain stable, but the current transient response could be worse than for the nominal inductance value. Additionally, the GPC stability limits were also proven and compared with the PDB stability limits. Input current steps were commanded while disabling the output voltage controller as shown in Figure 11. As can be seen, settling time is longer with the PDB controller, showing a lower stability margin than with the GPC strategy. Accordingly, the PDB strategy was unstable for $\Delta L > -50\%$ whilst the GPC strategy was unstable for $\Delta L > -70\%$, as considered by design.

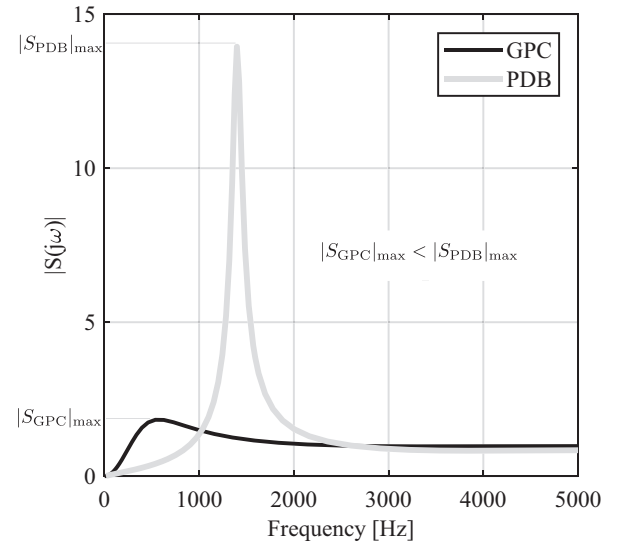


FIGURE 10 Comparison of the sensitivity function between the GPC and the PDB strategies

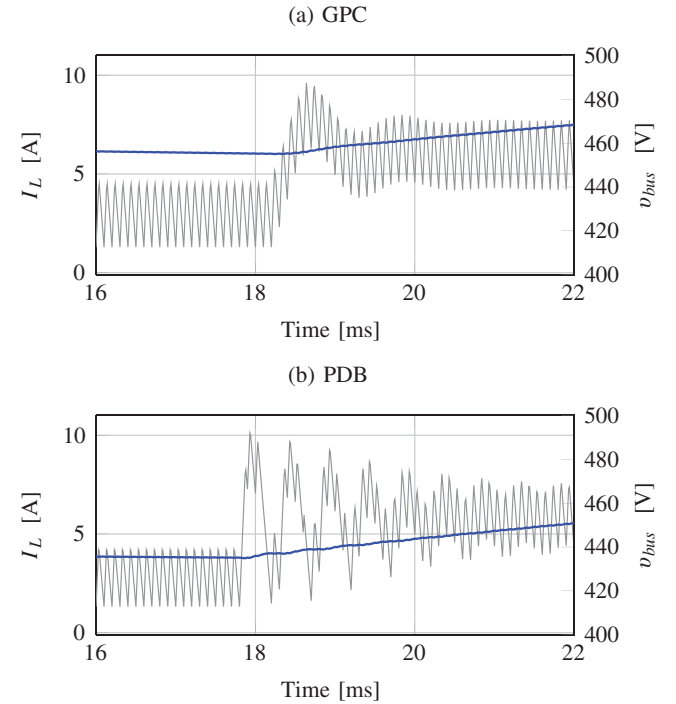


FIGURE 11 Input current (thin line) and output voltage (thick line) waveforms with commanded step from 3 A to 6 A under inductance reduction $\Delta L = -50\%$ from the original value

Robustness experimental results were obtained using a step command in the current setpoint from 3 A to 6 A and compared against that of the PDB. In both cases, the outer voltage control loop was disabled, the output load was resistive with value $R_{\text{load}} = 210 \Omega$, and the input voltage $v_{\text{in}} = 300 \text{ V}$. Transient responses without model mismatch are shown in Figure 12(a) and (b), for the GPC and PDB strategies, respectively. The GPC rise time is $t_r \approx 800 \mu\text{s}$, while the PDB presents a faster

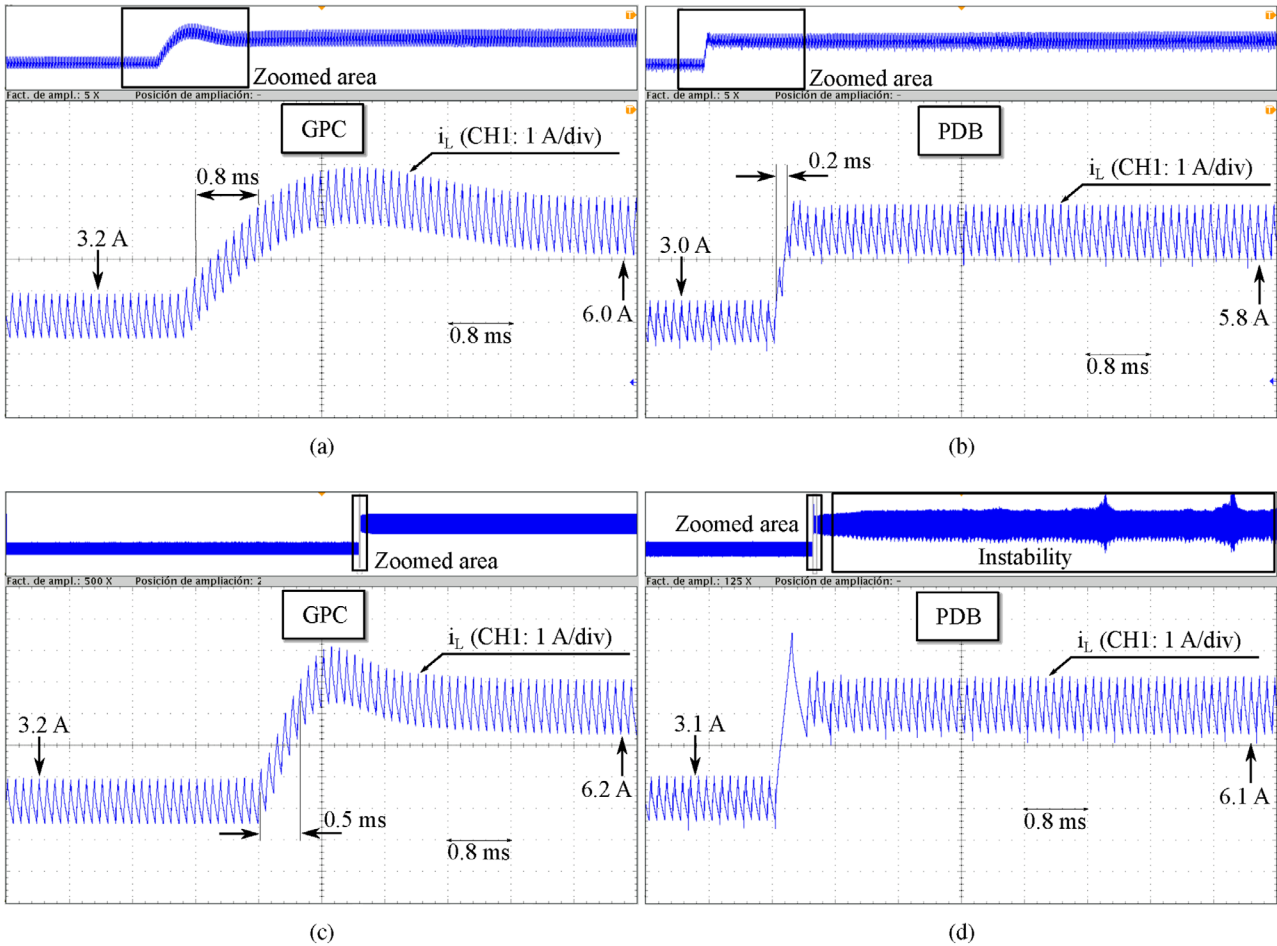


FIGURE 12 Inductor current step response from 3 A to 6 A. $R_{load} = 210 \Omega$. (a and b) Without model mismatch. (c and d) With model inductance 3.5 times greater than the real inductance

rise time of $t_r \approx 200 \mu s$. This makes sense because the PDB objective is the maximisation of dynamic response, while the GPC design implied reducing the dynamic response in favour of improved robustness.

The transient response with model-mismatch is shown in Figure 12(c) for the GPC strategy and in Figure 12(d) for the PDB controller. In this case, both controllers were designed considering an inductance 3.5 times greater than the real inductance. As can be seen, the GPC strategy presents a faster response than in the case without model mismatch, due to an increased loop gain, and also remains stable at steady state. In contrast, the PDB strategy presents oscillations at steady-state, which are visible in the zoomed out version of the waveform in the upper part of the oscilloscope capture. These oscillations show that the PDB strategy is unstable for this condition, which is a direct consequence of its higher sensitivity to system variations.

4.3 | Additional tests

Voltage loop control was evaluated by its load and line transient responses, which are shown in Figure 13(a) and (b), respectively.

In both cases, the output voltage setpoint was set at 500 V but the oscilloscopes captures are AC coupled to show the transient phenomena with more detail. The load transient response test was carried out by a load change from 420 to 210 Ω with $v_{in} = 250$ V. The line transient response test was carried out using a change in the input voltage v_{in} from 250 V to 350 V. Load and line transient response resulted in a peak transient of 8 V and 14 V, respectively. In both cases, a settling time of $t_s \approx 240$ ms was observed.

Calculation times were measured for the GPC, PDB, and PI ACME strategies. The PI spent 0.8 μs , the PDB spent 1.2 μs , while the GPC current loop needed 3.40 μs , for making the necessary calculations. This reflects a higher computational burden of the proposed current controller. Even though the proposal is more demanding, it only represents 3.4% of the available 100 μs computation time.

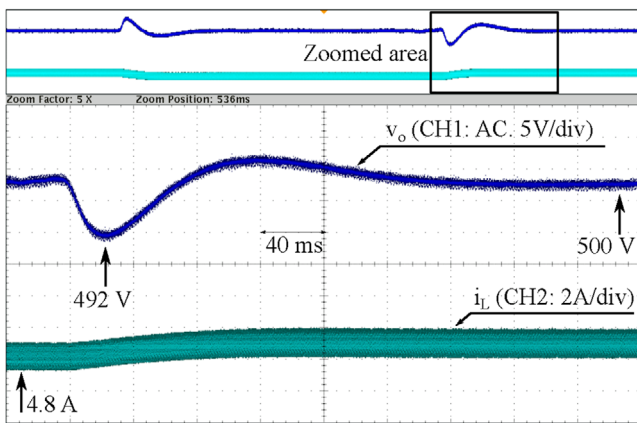
4.4 | Comparison with state-of-the-art control strategies

A quantitative comparison of the proposed GPC ACME strategy with other state-of-the-art control strategies is shown in

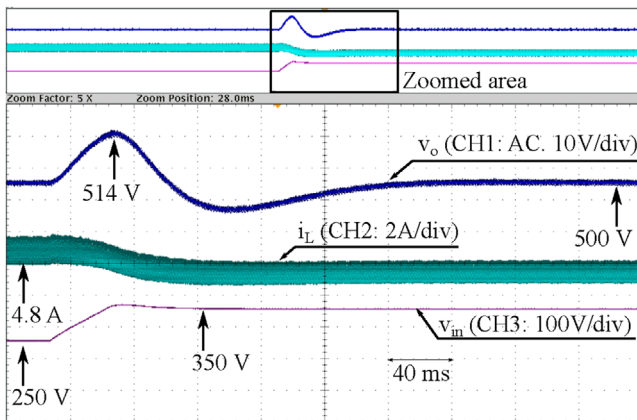
TABLE 3 Comparison with state-of-the-art control strategies

Strategy	Ref.	CT [μ s]	MDC [%]	SFV [%]	CRT [A/ms]	Load TR [%]	Line TR [%]
RCMC	[10]	–	–	–	–	4.2 @ 5 W	1.7 @ 1 V
Constant On-Time	[11]	4 @ 26 MHz	94	22.6	–	–	–
Constant Off-Time	[12]	–	–	1	–	3.15 @ 4.2 W	–
	[13]	–	–	–	–	12 @ 15 W	–
FCS-MPC	[24]	–	N/A	–	–	3 @ 12 W	–
PID ACMC	[17]	–	N/A	N/A	–	8.7 @ 150 W	–
	[18]	–	N/A	N/A	–	8.33 @ 225 W	–
PI+CI ACMC	[19]	–	N/A	N/A	2.5 @ 500 μ H	–	–
PDB ACMC	[15]	–	N/A	N/A	50 @ 40 μ H	0.4 @ 19 W	0.4 @ 4 V
GPC ACMC	N/A	3.4 @ 120 MHz	N/A	N/A	3.75 @ 6140 μH	1.4 @ 595 W	2.8 @ 100 V

Abbreviations: CT, calculation time; CRT, current rise time; MDC, maximum duty cycle; N/A, not applicable; SFV, switching frequency variation; TR, transient response. The bold fonts are there to highlight the proposed control over the existing strategies.



(a)



(b)

FIGURE 13 (a) Measured AC coupled output voltage (top) and inductor current (bottom) under load change from 420 to 210 Ω ($V_{bus} = 500$ V). (b) Measured AC coupled output voltage (top) and inductor current (middle) under input voltage change from 250 V to 350 V (bottom) ($V_{bus} = 500$ V)

Table 3. First, it can be seen that, although computationally efficient, constant on- and off-time strategies suffer from duty cycle limitations and variable switching frequency. Although not

reported, FCS-MPC and RCMC also present variable switching frequency where ACMC strategies do not, because the latter makes use of a PWM module with a constant frequency modulating waveform. Of the ACMC strategies, it is shown that the slowest current rise time is reported by the PI+CI strategy, and the fastest current rise time is reported by the PDB strategy, which is more than 13 times faster than the proposed GPC. However, the proposed GPC was tested in a converter with an inductor more than 150 times larger, which inherently limits the overall current control bandwidth. Therefore, a more realistic comparison was provided in this work, where it is 4 times faster than the GPC proposal. Regarding output voltage load and line transient response, the PDB strategy reports the lowest percentage, with 3.5 times less load transient and 7 times less line transient magnitudes than the GPC strategy. However, the proposed strategy load transient response was tested with a load power step more than 31 times larger, and a line voltage step 25 times larger. Therefore, considering the load transient response per watt and line transient response per volt, the proposal presents the best results. Finally, it is important to highlight that the cited strategies lack results of their robustness and performance variation with the operating point.

5 | CONCLUSION

In this work, a novel ACMC for a PFE three-phase boost-type converter based on a GPC strategy was proposed, also introducing a novel GPC design procedure where it was shown that not only the cost function parameter λ but also the disturbance polynomial model coefficient e_2 affects both dynamic response and robustness. The effect of adding an AWU algorithm to the GPC strategy was also analysed for the first time, highlighting its importance to keep the closed-loop operation of the system at all times.

The proposed strategy was evaluated in terms of performance variation with the system operating point and robustness and compared with a PI strategy and a PDB strategy, respectively. On the one hand, results showed that the poles of the

second-order approximation of the closed-loop system with the proposed GPC strategy had 5 times less real frequency variation and 6 times less imaginary frequency variation than with the PI strategy, for the same operating point variations. On the other hand, to support the robustness criterion taken in the GPC design procedure, a sensitivity analysis was carried out and showed that the PDB current control loop presents more sensitivity than the designed GPC strategy. Also, simulations showed at face value that the GPC strategy presented higher relative stability than its PDB counterpart under inductance model-mismatch. In line with this last statement, experimental results showed that the PDB strategy presented a noticeable overshoot and steady-state oscillations in the case of model mismatch. These phenomena are impossible to prevent because the PDB strategy does not provide the designer with any parameter to modify its stability margins. In contrast, the proposed GPC strategy presented only slightly more overshoot than without model mismatch and no steady-state oscillations appeared. Therefore, taking into account both evaluations, the proposed GPC strategy can be considered a superior choice than the PI and PDB controllers. The previous advantages of the GPC strategy come at the cost of an increased computational burden. However, for microcontrollers running at around 100 MHz and switching frequencies of 10 kHz, the proposal only requires less than 5% of the available calculation time.

The voltage loop was also tested by evaluating the output voltage load and line transient response. The results showed that, compared to the existing state-of-the-art strategies, the proposal presents the best results in load transient response per watt and line transient response per volt.

The proposal has some room for further improvements given enough computational power to carry them out. For instance, adopting an adaptive GPC formulation would further improve the controller performance under input inductance variation scenarios. Also, higher order disturbance models could be included in the design process to capture more complex disturbance phenomena. This should also come with a more complex design process.

In summary, the proposed solution presents the following advantages for the control of PFE three-phase converters:

- Being a CMC strategy, it does not suffer from the presence of RHP zeros, which is the main drawback in VMC strategies.
- By using an average CMC strategy and a PWM module, it guarantees fixed switching frequency without the need for compensation of subharmonic oscillations, which is a must in Ripple CMC strategies and does not impose a maximum duty cycle as opposed to COTCMC.
- As it is implemented in a digital microcontroller, it does not suffer from component tolerances and aging, which are present in analog implementations.
- Compared to the existing digital APMC strategies, the proposal has the same performance regardless of the operating point, which is an advantage compared to the existing PID and state-space-based strategies. It also has a faster dynamic response than the PI+CI proposal and more robustness than the PDB strategy.

- It presents the best results in output voltage load transient response per watt and line transient response per volt, compared to the existing state-of-the-art strategies.
- The previous advantages are achieved with a low computational burden, allowing a direct implementation in most commercial microcontrollers.

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APPENDIX A

A.1 | Outer voltage control loop

The model to be used for the voltage control loop can be obtained considering the capacitor voltage

$$\frac{dv_{\text{bus}}(t)}{dt} = \frac{i_C(t)}{C}, \quad (\text{A.1})$$

where $i_C(t)$ is the output capacitor current, the control variable of the output voltage loop. Therefore, using the Laplace transform, the output voltage TF model results

$$G_v(s) = \frac{V_{\text{bus}}(s)}{I_C(s)} = \frac{1}{sC}. \quad (\text{A.2})$$

However, as the inner current control loop commands input current, it is necessary to transform the desired capacitor current given by the voltage controller to a proper input current setpoint for the inner current control loop.

The capacitor's current $i_C(t)$ can be calculated as

$$i_C(t) = i_D(t) - i_{\text{load}}(t), \quad (\text{A.3})$$

where $i_D(t)$ is the current through the diode and $i_{\text{load}}(t)$ is the current through the load. Considering a lossless converter, the diode current $i_D(t)$ can be calculated as

$$i_D(t) = \frac{v_{\text{in}}(t)}{v_{\text{bus}}(t)} i_L(t), \quad (\text{A.4})$$

which can be deduced from the input and output power equality. Replacing (A.4) into (A.3) and reordering terms give

$$\frac{v_{\text{in}}(t)}{v_{\text{bus}}(t)} i_L(t) = i_{\text{load}}(t) + i_C(t). \quad (\text{A.5})$$

Therefore,

$$i_L(t) = \frac{v_{\text{bus}}(t)}{v_{\text{in}}(t)} (i_{\text{load}}(t) + i_C(t)). \quad (\text{A.6})$$

As $i_{\text{load}}(t)$ is unknown and it is not measured, it can be considered a disturbance at the control input for the voltage loop, which must be rejected. Consequently, it will be considered zero for the input current setpoint calculation.

Therefore, considering (A.6), the input current setpoint in the discrete-time domain can be calculated as

$$i_{L_{\text{ref}}}(k) = \frac{v_{\text{bus}}(k)}{v_{\text{in}}(k)} i_C(k), \quad (\text{A.7})$$

since $i_C(k)$ is the output voltage control variable in the discrete-time domain. It is worth noting that if $i_{\text{load}}(t)$ were measured it could be added to the reference calculation as

$$i_{L_{\text{ref}}}(k) = \frac{v_{\text{bus}}(k)}{v_{\text{in}}(k)} (i_{\text{load}}(k) + i_C(k)), \quad (\text{A.8})$$

lowering the disturbance rejection requirement of the voltage controller. As can be seen, the resulting voltage control input, if acting as the setpoint to the inner current loop, should be modified to accurately define the input current as a function of the desired output current for controlling the output voltage.

Considering the previous calculation, the discrete-time model used for the outer voltage control loop design can be obtained

by assuming that the inner current control loop is much faster than the maximum current setpoint signal bandwidth provided by the outer voltage loop, and, therefore, the current control loop dynamics could be neglected.

Finally, using the model given in (A.2), any compensator design strategy can be used, as long as the gain correction given in (A.7) is used. This would keep loop gain as expected by the linear model, improving line and load regulation of the voltage loop.