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Implementation of output impedance in single-phase inverters with repetitive control and droop control

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Abstract: A strategy for the implementation of the output impedance in single-phase inverters connected in parallel with droop control for uninterruptible power supply applications is proposed in this study. The proposal allows the load current to be distributed in proportion to the power capacity of the inverters connected in parallel, by establishing the magnitude and phase of the output impedance at the fundamental frequency and its harmonics, when the voltage control is performed through odd harmonic repetitive controllers. This is accomplished through the design of an output impedance profile based on the transfer function of a second-order high-pass filter and a virtual impedance loop. The proposal achieves a correct operation of the droop control strategy and the proper sharing of the harmonics of the non-linear load current between the inverters connected in parallel, obtaining reduced values of individual harmonic content and harmonic distortion in the output voltage with reduced processing requirements. The validity of the proposal is verified through a 2 kVA experimental prototype, considering the requirements of the international quality standards IEC62040-3 and IEC61000-2-2, in terms of output voltage regulation, individual harmonic content, and harmonic distortion for inverters operating both in islanded-mode and in parallel.

1 Introduction

The supply of critical loads through static DC–AC converters or inverters that constitute an uninterruptible power supply (UPS) requires consideration of the degree of availability of the power supply, as it is established by international quality standards [1]. The IEC62040-3 [2] standard defines the functional availability of a UPS based on the average operating time in which the output voltage meets the amplitude and frequency variation limits set by the standard. A functional availability of 99.999% (five nines) determines that the electrical supply of critical loads connected to the UPS can be interrupted or be deficient for a little more than 5 min for each year of operation throughout the entire service life of the UPS.

To obtain a power supply with high-reliability rates, the possibility of being connected in parallel is usually supported by UPS. In this case, the power required by critical loads is shared proportionally to the power capacity of the UPS, providing redundancy, tolerance in front of permanent damages, greater autonomy in the case of interruptions in the electricity distribution network and the possibility of integrating different power supplies [1, 3, 4].

The parallel connection of inverters through decentralised control strategies in which communication is not required, reported in the literature under the name of droop control [3, 5–9], is especially suitable in the case of inverters used in UPS. This is because these strategies do not set restrictions to the location of the units connected in parallel thus providing greater reliability.

Droop control allows sharing the power between inverters connected in parallel by emulating the dynamic behaviour of synchronous generators connected in parallel [10]. This is done based on the local voltage and current measurements that are performed independently on each one of the inverters. However, to achieve an adequate sharing of the load between them, while also maintaining a reduced total harmonic distortion (THD), specific values of amplitude and phase of the output impedance at the fundamental frequency and harmonics of the output voltage are required [3, 11]. This feature is difficult to achieve when the control of the output voltage is carried out by odd harmonic repetitive controllers (O-HRCs) [12–14].

The reduction of output impedance through the application of the internal model principle (IPM) [15] in repetitive [12, 13, 16–19] and resonant [19–23] controllers allows achieving the asymptotic tracking of a sinusoidal reference and the rejection of periodic disturbances produced by the load current. Although these characteristics are adequate for the implementation of inverter control systems used in UPS that operate in islanded mode, in the case of inverters connected in parallel a reduced value of the output impedance can cause high circulating currents as a result of parametric differences [3] while also producing differences in the currents provided to the load by each inverter.

The proper sharing of the power required by the load in parallel connected inverters can be achieved through a virtual impedance loop tuned to the fundamental frequency of the output voltage [3, 5, 11, 21–28]. The virtual impedance loop avoids the cost, volume, and losses produced by physical impedance connected in series with the output of the inverters and allow establishing the characteristics of the output impedance that guarantee the proper operation of the droop control strategy [29]. In inverters where the control of the voltage is carried out through a bank of resonant controllers, the output impedance around the harmonics of the fundamental frequency is achieved by the adjustment of the gain of the resonant structures at frequencies different than the fundamental one [21, 22, 24]. However, unlike a bank of resonant controllers, repetitive control does not provide access to the resonant structures at the fundamental frequency and harmonics of the output voltage. For this reason, the amplitude and phase of the output impedance at the fundamental frequency and its harmonics cannot be set independently. This determines that the usual implementation of the output impedance in IPM-based controllers, such as first-order high-pass filters [11, 23, 27] and all-pass filters [30], are not suitable for repetitive control.

The use of a second-order bandpass filter bank was also reported in the literature, to achieve appropriate output impedance values and an accurate sharing of the power required by the load around the harmonics of the output voltage [31–33]. With the same purpose, in [34, 35], a droop control and spectral analysis of the current provided by the UPS around the harmonics of the output voltage were performed. However, these proposals have a high-

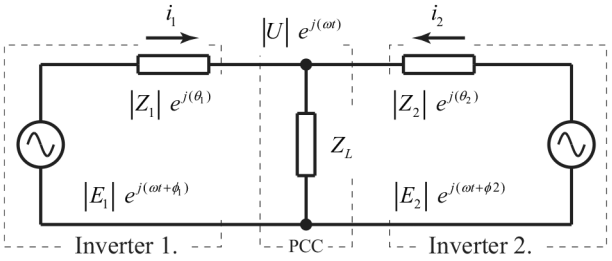

Fig. 1 *Equivalent circuit of two inverters connected in parallel to a load* Z_L

computational cost and, therefore, they can only be implemented at reduced sampling rates.

On the other hand, the output impedance in inverters that can operate both in parallel and in islanded mode must have reduced values at the fundamental frequency and its harmonics to meet with the individual harmonic content and harmonic distortion established by international quality standards [16, 20, 21, 24]. For this reason, the implementation of the output impedance in parallel-connected inverters, where the control of the output voltage is carried out through repetitive control, requires considering a new type of implementation of the virtual-impedance loop.

This study proposes a strategy for the implementation of the output impedance in single-phase inverters connected in parallel with droop control for UPS applications. The proposal allows establishing the amplitude and phase of the output impedance at the fundamental frequency and the harmonics of the output voltage in inverters with repetitive control, to achieve a proper sharing of the power required by the load between the inverters connected in parallel with lower processing requirements with respect to the strategies proposed in [31–35] while meeting the performance and quality requirements of international standards IEC62040-3 and IEC61000-2-2 [36] when inverters operate both in islanded mode and in parallel.

The work is organised as follows. In Section 2, a brief review of the droop control strategy is carried out. Section 3 describes the topology of the control system of an inverter with O-HRCs and the difficulties inherent to this topology in terms of implementing the output impedance. In Section 4, the design and implementation of the output impedance in a single-phase inverter with repetitive control are described. Finally, in Section 5, the experimental results that validate this proposal are shown, considering the regulatory requirements regarding individual harmonic content and harmonic distortion of the power quality standard IEC62040-3 and IEC61000-2-2.

2 Droop control

In this section, a brief review of the droop control strategy and aspects that determine an adequate sharing of power between parallel-connected inverters is carried out.

Fig. 1 shows the Thévenin equivalent circuit at the fundamental frequency of two inverters connected in parallel to a point of common coupling (PCC) from which critical AC loads are supplied. The PCC has a voltage with an amplitude U, a null phase and an angular pulsation $\omega = 2\pi f_0$ with $f_0 = 50\,\text{Hz}$, in this particular case. The output voltage of both inverters has an amplitude E_k with a phase relative to the PCC ϕ_k and an output impedance of magnitude Z_k and argument θ_k, with $k = \{1, 2\}$.

From Fig. 1 and considering a constant voltage at the PCC [27, 37], the active (P_k) and reactive (Q_k) powers developed by each inverter is given by [34, 35, 38]

$$P_k = (U/Z_k)[E_k\cos(\theta_k - \phi_k) - U\cos\theta_k] \tag{1}$$

$$Q_k = (U/Z_k)[E_k\sin(\theta_k - \phi_k) - U\sin\theta_k] \tag{2}$$

Expressions (1) and (2) show that the power developed by the inverters depends on the argument of the output impedance at the fundamental frequency (θ_k). Therefore, the inductive, capacitive, or complex nature of the output impedance has an influence on the power transferred to the PCC [3, 5, 39]. To avoid the cost, volume and losses associated with a physical impedance are connected in series with the output of the inverters [40], the output impedance is usually implemented by a virtual impedance loop, which is a part of the control system of both inverters [5, 23, 24, 26–28, 33, 41].

Table 1 Active and reactive power variation depending on the output impedance

inductive output impedance ($\theta_k \simeq 90°$)
$P_k \simeq (U \cdot E_k/Z_k)\phi_k$
$Q_k \simeq U(E_k - U)/Z_k$
resistive output impedance ($\theta_k \simeq 0°$)
$P_k \simeq U(E_k - U)/Z_k$
$Q_k \simeq -(U \cdot E_k/Z_k)\phi_k$
complex Output Impedance ($0° < \theta_k < 90°$)
$P_k = (U/Z_k)[(E_k\cos\phi_k - U)\cos\theta_k + E_k\sin\phi_k\sin\theta_k]$
$Q_k = (U/Z_k)[(E_k\cos\phi_k - U)\sin\theta_k - E_k\sin\phi_k\cos\theta_k]$

Assuming an inductive output impedance around the fundamental frequency of the output voltage ($\theta_k \simeq 90°$), it is possible to approximate $\sin\theta_k \simeq 1, \cos\theta_k \simeq 0$ in (1) and (2) [23]:

$$P_k \simeq (U \cdot E_k/Z_k)\sin\phi_k \simeq (U \cdot E_k/Z_k)\phi_k \tag{3}$$

$$Q_k \simeq U(E_k\cos\phi_k - U)/Z_k \simeq U(E_k - U)/Z_k \tag{4}$$

where it has also been considered a reduced phase difference between the output voltage of the inverters and the PCC ($\phi_k \simeq 0, \sin\phi_k \simeq \phi_k, \cos\phi_k \simeq 1$).

From these simplifications, it is possible to conclude that the control of the active power supply (3) can be carried out by modifying the relative phase of the inverter's output voltage. On the other hand, the reactive power control (4) can be done by modifying the amplitude of the output voltage with respect to the PCC ($E_k - U$). In the literature, this type of power control is referred to as $P - \omega$ and Q - E to differentiate it from other types of control strategies, where the output impedance of the inverters is resistive or complex [3, 32, 33, 35]. Table 1 describes the different droop control strategies and the powers developed by the inverters connected in parallel, depending on the type of output impedance.

The parallelism of inverters with inductive output impedance through droop control consists of modifying the frequency and output voltage of the inverters connected in parallel according to the supplied active and reactive powers, respectively [6, 35]

$$\omega_{i-k} = \omega_0 - m_k \cdot P_k \tag{5}$$

$$E_{i-k} = E_0 - n_k \cdot Q_k \tag{6}$$

Coefficients m_k and n_k determine the slope of the droop curve for the active and reactive powers, respectively [42]. They are usually determined according to the angular pulsation ($\Delta\omega$) and voltage (ΔU) variations that can be admitted at the PCC [3, 22, 28, 37, 43]

$$m_k = \Delta\omega/P_N \tag{7}$$

$$n_k = \Delta U/Q_N \tag{8}$$

being P_N and Q_N the maximum values of active and reactive power that the inverter can deliver.

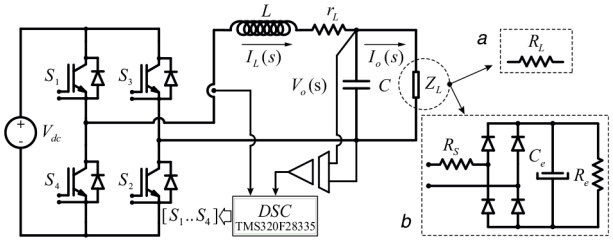

Fig. 2 *Topology of a single-phase inverter with L–C output filter*
(a) Linear load, ***(b)*** Reference non-linear load

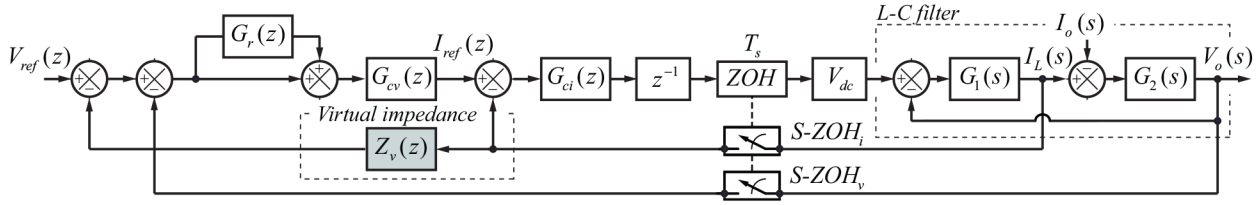

Fig. 3 *Block diagram of the control system of the inverter shown in Fig. 2*

In the literature, it has been indicated that high values of m_k and n_k guarantee a better sharing of the power required by the loads connected to the PCC and a lower circulating current between the units connected in parallel, at the expense of greater variations of voltage and frequency in the PCC [28, 44].

From (5) and (6) it follows that droop control allows controlling the power supplied by the inverters connected in parallel, through local power measurements, providing greater reliability regarding parallelism strategies that require communication [3].

To achieve an adequate voltage regulation and reduced THD in the output voltage of the inverters, a reduced output impedance value must be ensured at the fundamental frequency and the harmonics of the output voltage, respectively [16, 22]. However, a reduced output impedance value can cause a high circulating current between the units connected in parallel as a result of parameter mismatch and phase differences between the inverters. The output impedance must also provide an inductive behaviour around the fundamental frequency of the output voltage (in this particular case) to achieve the correct operation of the droop control, and a resistive behaviour around the harmonic components of the voltage output [7, 32, 33]. Otherwise, the variation of the output impedance with the frequency would produce an increase in the harmonic distortion of the output voltage when the load has non-linear characteristics [11, 25, 45].

3 Implementation of the virtual impedance loop

Fig. 2 shows the topology of a single-phase inverter used in double-conversion UPS [1, 4]. The topology consists of a DC voltage source V_{dc}, a full-bridge inverter, and an L–C filter, with which the amplitude of the harmonics resulting from the modulation is reduced. The control system consists of a multi-loop with an internal loop for controlling the inductor current and an external loop for controlling the output voltage of the inverter.

Fig. 3 shows the block diagram of the discrete-time inverter control system, where the transfer functions of inductor $G_1(s)$ and capacitor $G_2(s)$ of the L–C filter, the internal current-control loop $G_{ci}(z)$, the external voltage-control loop $G_{cv}(z)$ and the plug-in implementation of an O-HRC $G_r(z)$ are indicated, in addition to the sampling zero-order hold and zero-order hold for a sample rate $f_s = 1/T_s$ [16]. In the diagram, the control delay (z^{-1}) due to the digital implementation and the time required for the execution of the control strategy has also been considered [46].

The output impedance in inverters that operate in islanded mode is determined by the design of the multi-loop controllers and the O-HRC. In the topology indicated in Fig. 3, the multi-loop controllers given by $G_{ci}(z)$ and $G_{cv}(z)$ are designed to complement the repetitive control while producing a reduced output impedance that ensures compliance with the requirements of IEC62040-3 and IEC61000-2-2 standards in inverters operating in islanded mode. The reduced value of the output impedance allows synthesising a sinusoidal waveform with reduced THD, while making the output voltage less sensitive to the disturbances produced by variations in the load current. However, a reduced output impedance can produce high circulating currents between inverters connected in parallel as a result of parameter mismatch [47].

The output impedance of the inverters that support the parallel connection is also determined by a virtual impedance loop, formed by the feedback of the inductor current $I_L(z)$ and the transfer function $Z_v(z)$ as illustrated in Fig. 3. The virtual impedance transfer function (Z_v) allows us to set specific values of magnitude and phase of the output impedance for the correct operation of the droop control [5, 23, 26, 27]. However, there are particular considerations depending on the topology of the controller used in the external voltage control loop.

Repetitive control provides high gains around the fundamental frequency and harmonics of the output voltage [14, 48], with which it is possible to achieve asymptotic tracking of a sinusoidal voltage reference and the rejection of periodic disturbances produced by the non-linear load. However, unlike a bank of resonant controllers, it does not provide access to the resonant structures that operate at the fundamental and harmonics frequencies of the output voltage. Therefore, the output impedance at the fundamental frequency and its harmonics cannot be configured independently. Thus, the implementation of the virtual impedance loop in inverters with repetitive control must consider the whole design of the output impedance at the fundamental and harmonics frequency of the output voltage. To overcome this limitation, in this work, it is proposed to integrate the output impedance requirements into a single transfer function, through the implementation of a virtual impedance profile that guarantees adequate load sharing between the inverters connected in parallel while meeting the requirements of regulation and harmonic content of the standards IEC62040-3 and IEC61000-2-2, applied to UPS.

4 Design and implementation of the virtual impedance profile

As indicated in the previous section, the control of inverters connected in parallel through a droop control strategy requires the implementation of a virtual impedance loop to establish the magnitude and phase of the output impedance around the fundamental and harmonic frequency components of the inverter. This section describes the design and a proposal for the implementation of the virtual impedance that guarantees compliance with international power quality standards.

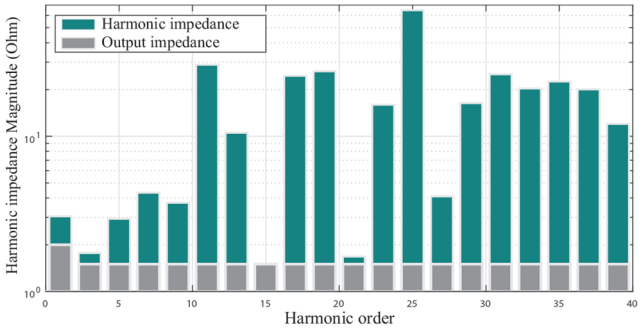

Fig. 4 *Proposed output impedance profile and amplitude of harmonic impedance, considering the requirements of standards IEC62040-3 and IEC61000-2-2*

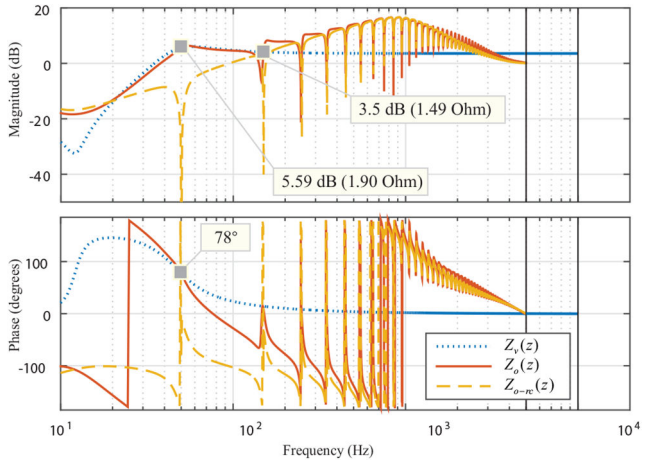

Fig. 5 *Output impedance of the inverter with virtual impedance loop* ($Z_o(z)$) *and without virtual impedance loop* ($Z_{o-rc}(z)$). *Profile of the virtual impedance in discrete time* ($Z_v(z)$)

4.1 Determination of the output impedance

The requirements of individual harmonic content and harmonic distortion for the output voltage of a UPS consider a reference non-linear load (Fig. 2*b*), whose parameters are expressed in IEC62040-3 standards in the function of the power rate of the UPS. Fig. 4 shows the ratio between the amplitude of the individual harmonics of the output voltage required by IEC62040-3 and IEC61000-2-2 standards and the current of a 2 kVA reference non-linear load. The impedance indicated in Fig. 4 is called harmonic impedance [49] and constitutes a means through which it is possible to estimate the output impedance that guarantees compliance with the requirements of individual harmonic content and harmonic distortion. Fig. 4 also shows the amplitude of the output impedance profile proposed in this work, which has an amplitude of 2.0 Ω at the fundamental frequency of the inverter and 1.5 Ω around the harmonic components of the output voltage. As indicated above, the phase angle of the output impedance must also provide inductive behaviour around the fundamental frequency of the inverter to reduce the coupling between the powers developed by the inverter and a resistive behaviour around the harmonics of the output voltage.

Considering the adopted output impedance profile and the amplitude of the harmonics of the current for a reference non-linear load, it is possible to estimate a THD of the output voltage of 5.96%, which is <8% value admitted by IEC62040-3. To obtain a THD of the output voltage lower than that indicated above, it is possible to adopt an output impedance profile with magnitude lower than that indicated in Fig. 4. However, this implies a greater circulating current between inverters connected in parallel under the same parameter mismatch.

4.2 Virtual impedance implementation

This section describes the implementation of the virtual impedance transfer function (Z_v), which establishes the characteristics of the output impedance. The output impedance profile projected above is obtained by the following transfer function of a second-order high-pass filter:

$$Z_v(s) = Z_{th}s^2/(s^2 + 2\xi\omega_n s + \omega_n^2) \tag{9}$$

where s is the complex Laplace variable, ω_n is the natural frequency, and ξ the relative damping factor.

The proposal is to obtain a virtual impedance (9) whose frequency response around the natural frequency corresponds to the behaviour of the output impedance around the fundamental component of the inverter output voltage. On the other hand, the amplitude of the frequency response for frequencies $\omega > \omega_n$ constitutes the amplitude of the output impedance for the harmonics of the output voltage (Z_{th}).

The frequency response of a second-order system has a resonance peak of amplitude M_r at an angular pulsation ω_r, given by the following expressions [50]:

$$M_r = Z_{th}/\left(2\xi\sqrt{(1-\xi^2)}\right), 0 \le \xi \le 0.707 \tag{10}$$

$$\omega_r = \omega_n/\sqrt{(1-2\xi^2)}, 0 \le \xi \le 0.707 \tag{11}$$

The phase at the frequency at which resonance occurs in the frequency response is given by the following expression:

$$\arg[Z_v(s)] = \arctan\left(\xi^{-1}\sqrt{(1-\xi^2)}\right) \tag{12}$$

Since Z_{th} constitutes the amplitude of the impedance for the harmonics of the output voltage, a commitment must be made in the determination of ξ and ω_n, to establish the value of the resonance frequency, the amplitude and the phase of the output impedance around the fundamental frequency.

For a value of $Z_{th} = 1.5\,\Omega$, the relative damping factor $\xi = 0.39$ is determined from (10), to obtain a peak amplitude of 2.0 Ω for the output impedance at the fundamental frequency of the inverter. Since the phase at the resonant frequency (12) for $\xi = 0.39$ provides a value of 64.94°, a value of ω_n slightly higher than that determined by (11) is adopted for $\omega_r = 2\pi f_r$ and $f_r = 50\,\text{Hz}$, to obtain a phase of 80° at the fundamental frequency of the output voltage and to reduce the P–Q control coupling.

Fig. 5 shows the discrete-time frequency response of the virtual impedance profile (9), discretised by Tustin method with pre-warping for a sampling rate of 20 kHz [51]. As shown in the figure, the amplitude of the virtual impedance around the fundamental frequency of the inverter is in this case slightly lower than the design value, as a result of having adopted a value of ω_r greater than the one determined by (11). Fig. 5 also shows the output impedance of the inverter for the parameters indicated in Table 2. In the figure, values consistent with (9) regarding the amplitude and phase of the output impedance at the fundamental and harmonics frequency of the output voltage are verified, as a result of the implementation of the virtual impedance loop.

For illustration purposes, the output impedance of the inverter with a plug-in O-HRC and without a virtual impedance loop [16] is shown in Fig. 5 for the parameters indicated in Table 2. As shown in Fig. 5, the multi-loop and O-HRC allow obtaining reduced output impedance values at the fundamental frequency and around the odd-harmonics frequencies of the output voltage, where periodic disturbances of the current of a reference non-linear load are manifested. Although these characteristics allow reduced THD values to be obtained when inverters operate in islanded mode, it should be noted that the output impedance of the multi-loop with the O-HRC lacks the characteristics that determine the correct operation of the droop control.

As indicated above, the output impedance without the virtual impedance loop depends on the design of the multi-loop controllers

Table 2 Parameters of the inverter as shown in Fig. 2

Inverter		
P_N	rated power	2 kVA
V_N	rated rms voltage	220 V
f_0	rated frequency	50 Hz
L	filter inductance	612 μH
r_L	equivalent series inductor resistance	0.1 Ω
C	filter capacity	50 μF
V_{cc}	DC link voltage	400 V
f_s	sampling rate	20 kHz
m	O-HRC decimated factor(*)	2

Parameters of the reference non–linear load		
R_s	interface resistance	0.97 Ω
R_e	DC load resistance	54.38 Ω
C_e	load capacity	2758.43 μF

Linear load parameters		
R_{L-1}	load resistance 100% P_N	24.2 Ω
R_{L-2}	load resistance 20% P_N	121.0 Ω

Multi-loop and O-HRCs
$G_{ci}(z) = 0.0135 \cdot (z - 0.15)/z$
$G_{cv}(z) = 0.0124 \cdot (z - 0.71)/(z - 1)$
$* \; G_r(z_m) = -0.30 \cdot z_m^{-100} \cdot Q(z_m) \cdot G_f(z_m)/(1 + z_m^{-100} \cdot Q(z_m))$
$* \; Q(z_m) = 0.25 \cdot z_m^{-1} + 0.5 + 0.25 \cdot z_m^{1}$
$* \; G_f(z_m) = (G_{cv}(z_m) \cdot G_{pv}(z_m)/(G_{cv}(z_m) \cdot G_{pv}(z_m) + 1))^{-1}$

* is a reference to the implementation of the transfer functions

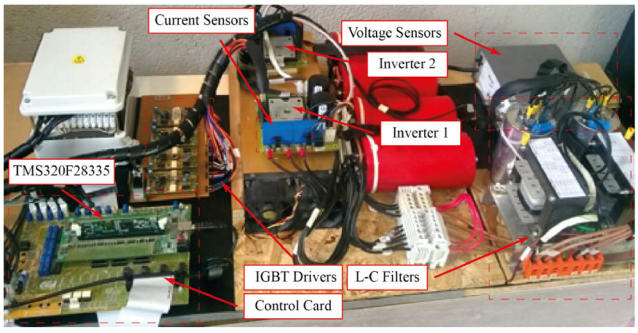

Fig. 6 *Photograph of the experimental prototype of two inverters*

and the plug-in O-HRC. In this particular case, due to the implementation of integral action in the multi-loop voltage controller, the inverters exhibit reduced DC output impedance values [16]. For this reason, in Fig. 5, a virtual resistance of 0.1 Ω has also been implemented in series with (9), to prevent direct current circulation as a result of slight differences in the average value of the voltages of the inverters connected in parallel. Similarly, in the case of even HRCs in which there is inherently an integral action in direct current [14], it will be necessary to implement a virtual resistance to reduce the circulating current. Unlike [52], this proposal does not require particular considerations in the case that inverters operate in islanded mode or parallel and the virtual resistance can be sized based on the expected differences in the average value of the output voltage of the inverters.

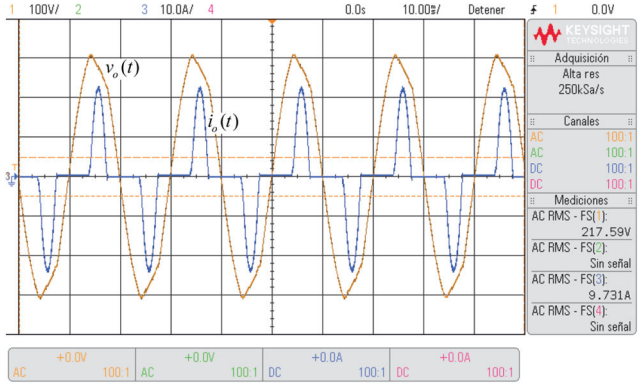

Fig. 7 *Output voltage and current of an isolated inverter connected to a non-linear reference load of 2 kVA. Ch:1 voltage (100 V/div), Ch:2 current (10 A/div)*

Unlike other implementations of virtual impedance reported in the literature where the behaviour of the output impedance at the fundamental frequency is established through the first-order all-pass or high-pass filters [11, 24, 26–28, 33], this proposal allows to consider in the design the reduced magnitude of the output impedance in inverters with repetitive control of the output voltage. On the other hand, the proposed strategy allows establishing the output impedance around the harmonics of the fundamental frequency with lower processing requirements in the digital implementation, with respect to a bank of bandpass filters tuned to the harmonic frequencies of the output voltage [31–33] or the spectral analysis of the load current [34, 35]. This last aspect allows an adequate distribution of the load current between the inverters connected in parallel, particularly in the case of non-linear loads. In this sense, the proposal allows the parallel operation of inverters with repetitive and droop control, the topology of which there is no background in the literature up to the best knowledge of the authors.

5 Experimental verification

The difference equations of multi-loop controllers, the O-HRC and the proposed virtual output impedance were implemented in discrete-time in a 32 bits – 150 MIPS floating point Digital Signal Controller (Texas Instruments TMS320F28335) with which the control of two 2 kVA inverters connected in parallel was performed. The inverters' parameters are indicated in Table 2. The experimental prototype is shown in Fig. 6.

The coefficient n_k for the droop control was obtained by (8) for a variation in the amplitude of output voltage of 1.2%. Although this value is substantially lower than the 10% that the IEC62040-3 standard admits, it provides an unfavourable scenario in terms of power-sharing and circulating current between inverters connected in parallel, with which the validity of this proposal is verified.

Owing to the sensitivity of the repetitive control to frequency variations [53], the active power control was implemented by varying the relative phase of the inverters with $\phi_k = \int m_k \cdot P_k + \int \omega \cdot dt$, being $m_k = 50 \times 10^{-6}$rad/s · W [21, 24, 37]. The determination of active and reactive powers was carried out through two second-order low-pass filters with a cut-off frequency one decade lower than the nominal frequency of the inverter and a damping factor of 0.707 [28, 37]. Both filters are implemented in discrete-time at a 20 kHz sampling frequency.

Fig. 7 shows the output voltage and current of an isolated inverter connected to a 2 kVA reference non-linear load. Fig. 8 shows the harmonic content of the output voltage and the limits of the individual harmonic content required by the IEC62040-3 standard. This verifies a correct sizing of the virtual output impedance because the individual harmonic content is lower than the limits required by the standard. The THD of the output voltage is 6.20%, which is below the 8% limit allowed by the IEC62040-3 standard and is consistent with the estimation indicated in Section 4.

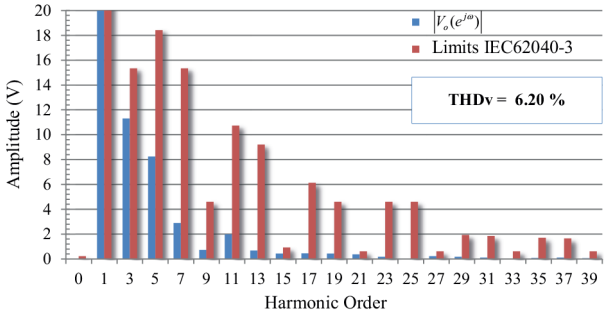

Fig. 8 *Individual harmonic content of the voltage for an isolated inverter connected to a non-linear reference load of 2 kVA (blue), and limits of individual harmonic content IEC62040-3 (red)*

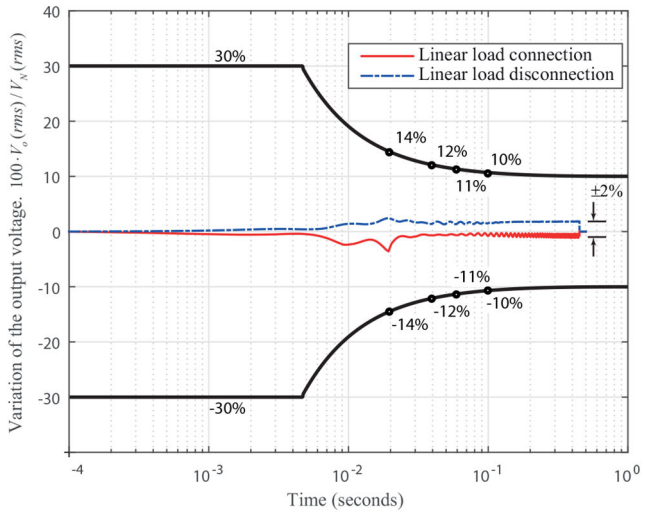

Fig. 9 *Classification 1: variation limits of the rms output voltage for a variation in the load current from 20 to 100% of the nominal power. Voltage variation for an isolated inverter*

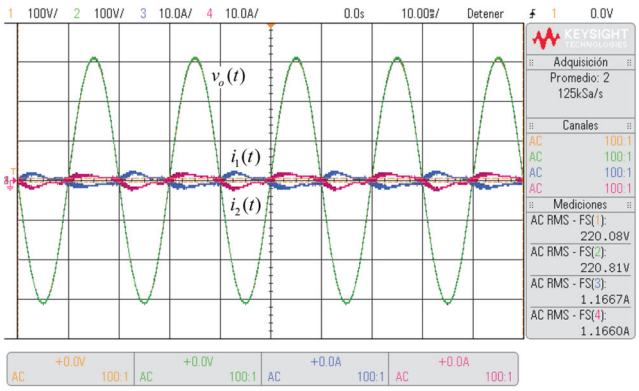

Fig. 10 *Output voltage and current of two inverters in parallel without load. Ch:1, 2 voltage (100 V/div), Ch:3, 4 current (10 A/div)*

Since the standard expresses the limits of regulation and dynamic response for variations in the load current, Fig. 9 shows the dynamic response of the output voltage of an isolated inverter for a variation of the current of a linear load from 20 to 100% of the nominal power of the inverter. The figure corresponds to an inverter operating in islanded mode because this is the worst condition in terms of the dynamic response of the output voltage. As shown in the figure, the inverter meets the limits established by IEC62040–3 for UPS classification 1, being the most demanding of the three classifications considered by the standard. In Fig. 9, the maximum voltage deviation from the rms value is ±3.5% and it shows a regulation of ±2% in steady-state as a result of the load current. These results are significantly lower than those required by the standard and constitute a slight increase with respect to the

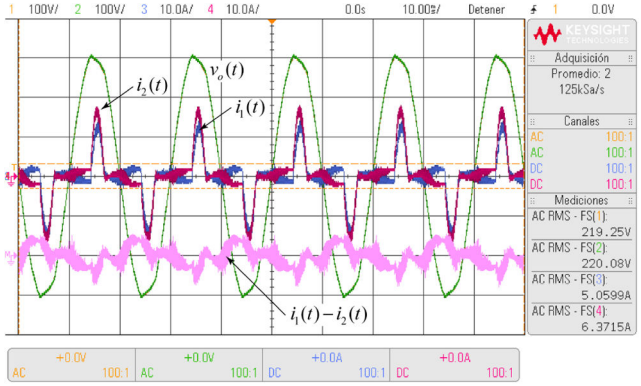

Fig. 11 *Output voltage and current of two parallel inverters connected to a reference non-linear load of 2 kVA. Ch:1, 2 voltage (100 V/div), Ch:3, 4 current (10 A/div). Math: Ch3–Ch4 (10 A/div)*

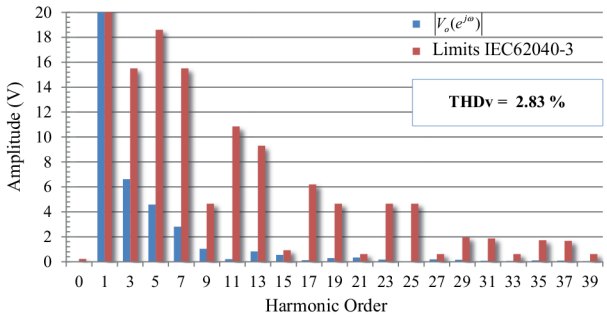

Fig. 12 *Individual harmonic content of voltage for two inverters connected in parallel with a reference non-linear load of 2 kVA (blue), and limits of individual harmonic content IEC62040-3 (red)*

values of an isolated inverter with multi-loop and O-HRC without a virtual impedance loop [16].

Fig. 10 shows the currents and voltages of the two inverters connected in parallel without load. Fig. 11 shows the same variables and also the circulating current between the inverters (Math), but for the case when the inverters supply a 2 kVA reference non-linear load. The rms value of the circulating current between inverters is 1.16 and 1.26 A when the inverters connected in parallel operate without load and with a reference non-linear load, respectively.

Fig. 12 shows the harmonic content of the output voltage and the limits of individual harmonic content required by the IEC62040-3 standard, when inverters operate in parallel (Fig. 11). The THD, in this case, is 2.83%, approximately half the value obtained for an islanded operation of the inverter (Fig. 8). This is due to the fact that the load current is distributed proportionally to the power capacity of the inverters connected in parallel, both at the fundamental frequency and at the harmonics frequencies as a result of adequate design of the output impedance profile. As shown in Fig. 12, the voltage has a harmonic content consistent with the requirements of the standard.

Fig. 13 shows the voltage and current of two inverters supplying a 2 kVA linear load. Fig. 14 shows the individual harmonic content and harmonic distortion of the output voltage where a reduced individual harmonic content is verified in terms of the requirements established by the standard.

Fig. 15 shows the current and voltage of two inverters connected in parallel with a linear load of 2 kVA together with a non-linear reference load of 2 kVA, totalling a 4 kVA power. Fig. 16 shows the individual harmonic content and harmonic distortion of the output voltage for the waveform shown in Fig. 15. As can be seen, the harmonic content is consistent with the standard requirements even under severe load conditions.

Fig. 17 shows the harmonic content of the difference between the currents of two inverters connected in parallel without load (Fig. 10) and for the different loads considered above (Figs. 11, 13, and 15). Considering the nominal power of the inverters connected in parallel, Fig. 17 shows a reduced difference between the currents

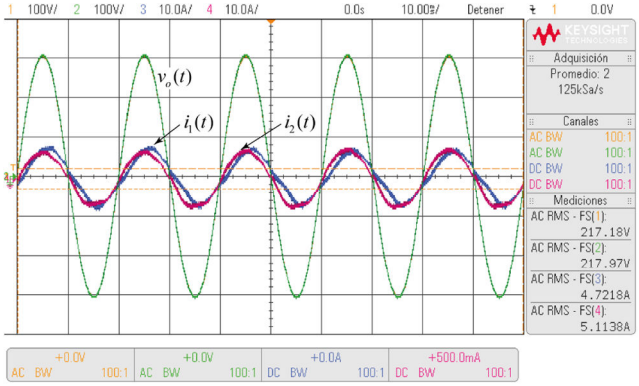

Fig. 13 *Output voltage and current of two parallel inverters connected to a linear load of 2 kVA. Ch:1, 2 voltage (100 V/div), Ch:3, 4 current (10 A/div)*

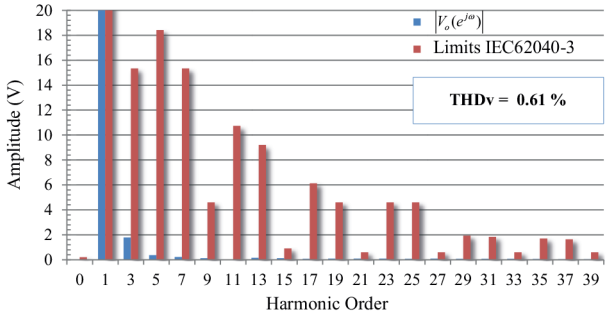

Fig. 14 *Individual harmonic content of voltage for two inverters connected in parallel with a linear load of 2 kVA (blue), and limits of individual harmonic content IEC62040-3 (red)*

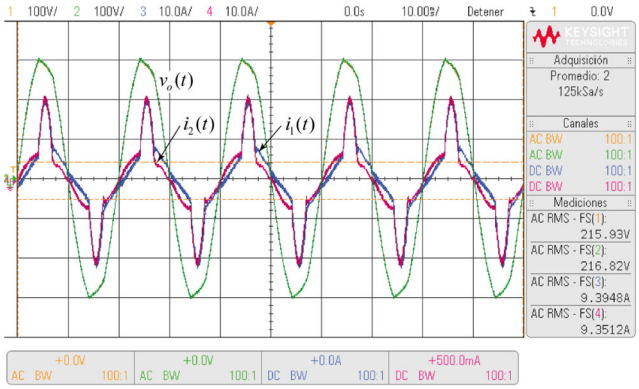

Fig. 15 *Output voltage and current of two parallel inverters connected to a linear load of 2 kVA and a reference non-linear load of 2 kVA. Ch:1, 2 voltage (100 V/div), Ch:3, 4 current (10 A/div)*

of both inverters. In particular, a reduced current difference around the fundamental frequency is the result of the adequate design of the amplitude and phase of the virtual output impedance around this frequency which allows a correct operation of the droop control.

It is important to note that, as shown in Fig. 17, a non-linear load behaviour can affect the circulating current between inverters connected in parallel. For this particular case, the harmonics of the current of a reference non-linear load increase the circulating currents' components at three, five, and seven times the fundamental frequency of the output voltage. However, harmonics three–seven have in all cases a reduced amplitude in relation to the amplitude of the fundamental component, and their effect on the output voltage meets the requirements of the IEC62040-3 standard, as previously described. The rms value of the circulating current between the inverters has the same order of magnitude for the different loading conditions. Furthermore, there are slight differences in the harmonic content of the circulating currents among the considered cases. Owing to that the inverters exhibit a

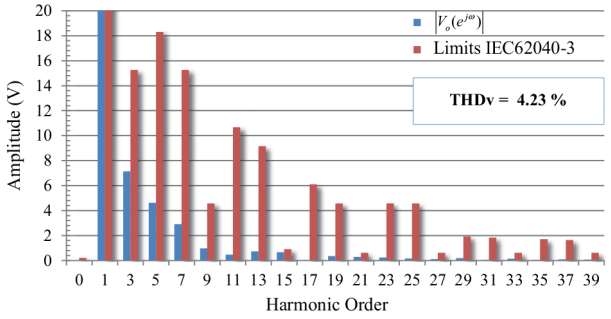

Fig. 16 *Individual harmonic content of voltage for two inverters connected in parallel with a linear and a non-linear reference load of 2 kVA (blue), and limits of individual harmonic content IEC62040-3 (red)*

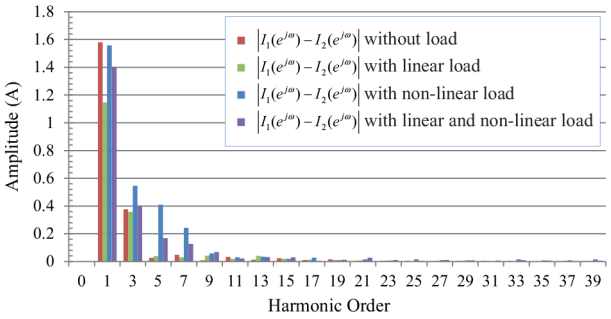

Fig. 17 *Harmonic content of the difference between the currents of both inverters for the different load conditions*

reduced sensitivity with respect to the harmonic content of the load current. Finally, from the comparison of the harmonic content of the current difference between the inverters for the different load conditions, it is concluded that the greatest current difference occurs when the inverters operate without load and with a non-linear reference load.

From the results shown in Figs. 7 to 16, it is possible to conclude that the proposal allows compliance with the requirements of the regulation, dynamic response, individual harmonic content, and harmonic distortion required by the IEC62040-3 and IEC62040-2-2 standards when inverters operate both in islanded mode and in parallel.

6 Conclusions

A strategy for implementing the output impedance in inverters connected in parallel with droop control for UPS applications was proposed, with which it is possible to establish the magnitude and phase at the fundamental frequency and harmonics of the output voltage when the voltage control of the inverters is carried out through O-HRC. The proposal allows the design of the output impedance considering the requirements of individual harmonic content and harmonic distortion established by the international quality standards IEC62040-3 and IEC61000-2-2 with reduced processing requirements and an adequate power-sharing of linear and non-linear loads between inverters connected in parallel with droop control. Experimental results show that the proposal allows us to meet the requirement of regulation, individual harmonic content, and harmonic distortion of the IEC62040-2 and IEC61000-2-2 standards when inverters operate in islanded mode and in parallel.

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