Simple Real-Time Digital PWM Implementation for Class-D Amplifiers With Distortion-Free Baseband

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***Abstract*—A real-time, digital algorithm for pulse width modulation (PWM) with distortion-free baseband is developed in this paper. The algorithm not only eliminates the intrinsic baseband distortion of digital PWM but also avoids the appearance of side-band components of the carrier in the baseband even for low switching frequencies. Previous attempts to implement digital PWM with these spectral properties required several processors due to their complexity; the proposed algorithm uses only several FIR filters and a few multiplications and additions and therefore is implemented in real time on a standard DSP. The performance of the algorithm is compared with that of uniform, double-edge PWM modulator via experimental measurements for several bandlimited modulating signals.**

***Index Terms*—Digital modulation, harmonic distortion, power amplifier, pulse width modulation (PWM), switching amplifier.**

I. Introduction

PULSE WIDTH MODULATION (PWM) is widely used to drive different types of switching converters, from dc-dc power converters [1] to class-D audio amplifiers [2] and RF transmitters [3]. Much of the recent research effort on PWM is focused on reducing the distortion introduced by digital implementations of PWM modulators. Some approaches are aimed at the elimination of certain specific harmonics produced by the modulation [4] while others are customized for multilevel ac drives applications [5] or three phase inverters [6], [7]. Some of these techniques are based on optimization methods which attempt to minimize the harmonic distortion of the output voltage [8], others on random switching PWM techniques applied to reduce the dominant harmonics [9].

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In general, all those methods developed for ac drive applications are not suited for class-D or switching amplifiers because they are designed for sinusoidal signals and not for arbitrary band-limited signals, as required by audio amplifiers. The problem with digital PWM amplifiers is that standard modulation processes [10]–[13] produce baseband distortion that cannot be eliminated by the demodulator, usually a low-pass filter. Although part of this distortion can be reduced by using very high PWM frequencies, thus reducing the efficiency, it cannot be completely removed from the output spectrum.

Click modulation [14], [15] is an interesting alternative for analog PWM as it allows the generation of low switching rate binary signals with separated baseband. The first hardware implementation of click modulation applied to switching amplifiers required three DSPs to run the algorithm and two FPGA acting as a digital pulse former [16], [17]. In a recent implementation [18], [19], a DSP and a FPGA were required to achieve a bandwidth of 12 kHz which is below the 0–20 kHz standard for consumer audio products. These implementations are not only hardware demanding but also suffer from the discrete-time approximations that are required to implement the click modulator [20]. Recently a discrete-time approach of click modulation, which avoids the aliasing problems of the discretization process, has been presented [21], but a real-time implementation has not been yet reported.

In this paper, a digital algorithm for baseband distortion-free pulse width modulation (BBDFPWM) suitable for real-time operation is developed, and its performance is evaluated via experimental measurements. The algorithm is derived in the time domain and it is based on computing the samples of the baseband content of the PWM signal as a function of the duty cycle values. A nonlinear model of the PWM process that accurately reflects the nonlinearity introduced by the modulation is derived. Patent [22] and other articles, such as [23], [24], arrived at similar mathematical descriptions following different development paths. Based on such models, distortion reduction methods with different application ranges and capabilities for reducing distortion have been proposed. In this paper, an approximate numerical inversion of this nonlinear relation is performed in real time by the proposed BBDFPWM algorithm composed by the cascade connection of equal blocks of short length FIR filters and some multiplications and additions. Hence, its implementation is straightforward in any standard DSP platform. The performance of the algorithm is proportional to the number of cascade blocks, allowing the designer to tradeoff between a required performance and computational cost.

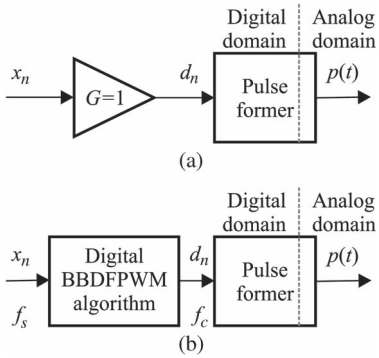

Fig. 1. Block diagrams. (a) Standard SDEUPWM and (b) proposed BBDFPWM digital algorithm.

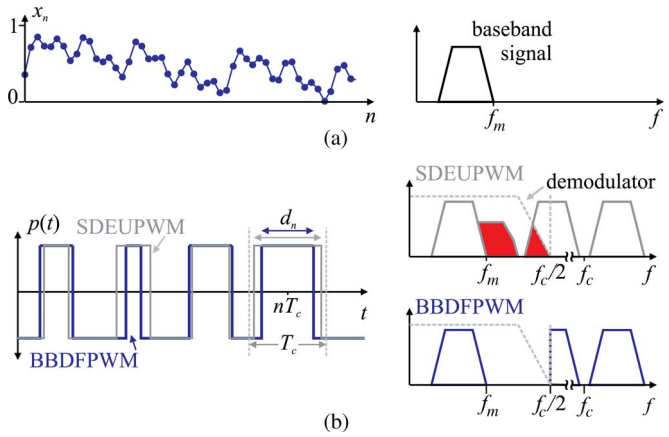

Fig. 2. Typical signals and spectral content. (a) Discrete input signal with its spectrum and (b) PWM signals with spectra.

The problem is described in Section II and the algorithm architecture is derived in Section III. Guidelines for the selection of the parameters of the algorithm, which determine its expected performance and computational complexity, are presented in Section IV. Comparisons to standard PWM methods and a previous approach in [22] are presented in Section V. In Section VI, the performance of the BBDFPWM algorithm is demonstrated with experimental measurements of real-world modulating test signals performed in the laboratory using an standard DSP. Finally, some conclusions are drawn in Section VII.

II. Problem Statement

In uniform digital PWM, the duty cycles d_n of the square-wave signal $p(t)$ are a scaled version of the sample values x_n of a modulating signal that is band-limited to f_m. In other words, if x_n and d_n are normalized, i.e., comprised within the range $(0, 1)$ the duty cycles are given by $d_n = x_n$, as shown in Fig. 1(a). A typical discrete-time modulating signal, sampled at f_s and with a maximum frequency content limited to f_m, is shown in Fig. 2(a).

Symmetrical Double Edge Uniform PWM (SDEUPWM) is one of the most common alternatives for digital PWM because of its easy implementation and good spectral behavior [10]. In SDEUPWM, the center of the pulses are evenly spaced by the carrier period $T_c = 1/f_c$ and the location of the rising and

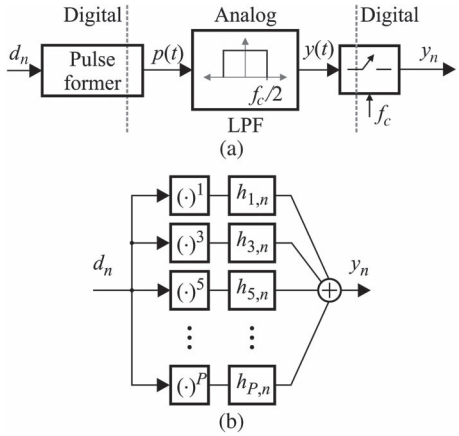

Fig. 3. Derivation of the BBDFPWM algorithm: (a) PWM modulator, ideal demodulator, and output sampling. (b) Nonlinear discrete-time model of the above.

falling edges depends on the sample value of the modulating signal x_n.

Two components contribute to the baseband distortion produced by SDEUPWM, as shown schematically in Fig. 2(b): the carrier sidebands that lie within the baseband (between 0 Hz and $f_c/2$) for low f_c/f_m ratios and the intrinsic baseband distortion that appears in the baseband independently of the f_c/f_m ratio that is dependent on the time derivatives of the modulating signal [10]; both are represented with the shaded area in the spectrum of Fig. 2(b). These distortion components cannot be eliminated by the low-pass-filter traditionally used as demodulator in most power electronics applications.

In this paper, a real-time implementation of a baseband distortion-free PWM algorithm (BBDFPWM) that has theoretically zero (and practical negligible) baseband distortion is presented. A block diagram is shown in Fig. 1(b), where the modulating signal x_n, sampled at f_s, is processed with the BBDFPWM algorithm to obtain the duty cycles d_n of the PWM signal $p(t)$ sampled at f_c (the PWM carrier frequency). The signal $p(t)$ produced by the BBDFPWM has duty cycles that are slightly different from the duty cycles of the SDEUPWM as illustrated in the PWM waveforms of Fig. 2(b). This small changes produce a very different frequency content.

The BBDFPWM ensures that the baseband spectrum of $p(t)$ is free from the intrinsic baseband distortion produced by digital PWM and also from carrier sidebands which do not appear below $f_c/2$ even for PWM switching frequencies f_c as low as $2f_m$. This characteristic allows for a greater flexibility in the selection of the carrier frequency and represents an improvement not only from other digital modulators but also from the analog or natural PWM which must use very high carrier frequencies to achieve reduced distortion levels.

III. BBDFPWM Algorithm

The objective of the BBDFPWM algorithm is to derive the duty cycles d_n from the modulating signal samples x_n such that the frequency content of the PWM signal $p(t)$ in the range $[0, f_c/2)$ is free of distortion. Its derivation can be explained with the help of Fig. 3(a). The continuous-time signal $y(t)$ is the low-pass filtered (demodulated) version of $p(t)$. Since $y(t)$

TABLE I
IMPULSE RESPONSE OF FIR FILTERS ($0 \le n < N$, $M = (N-1)/2$)

	Impulse Responses $h_{i,n}$ defined as a causal version of $c_{i,m}$: $h_{i,n} = c_{i,m}\big\vert_{m=n-M}$.	
$h_{1,n}$	$c_{1,0} = 1$	if $n = M$
	0	if $n \neq M$
$h_{3,n}$	$c_{3,0} = -\pi^2/72$	if $n = M$
	$c_{3,m} = -(-1)^m/(12m^2)\big\vert_{m=n-M}$	if $n \neq M$
$h_{5,n}$	$c_{5,0} = \pi^4/9600$	if $n = M$
	$c_{5,m} = \frac{(-1)^m}{480m^4}\left(-6+m^2\pi^2\right)\big\vert_{m=n-M}$	if $n \neq M$
$h_{7,n}$	$c_{7,0} = -\pi^6/2257920$	if $n = M$
	$c_{7,m} = -\frac{(-1)^m}{53760m^6}\left(120-20m^2\pi^2+m^4\pi^4\right)\big\vert_{m=n-M}$	if $n \neq M$
$h_{9,n}$	$c_{9,0} = \pi^8/836075520$	if $n = M$
	$c_{9,m} = \frac{(-1)^m}{11612160m^8}\left(-5040+840m^2\pi^2-42m^4\pi^4+m^6\pi^6\right)\big\vert_{m=n-M}$	if $n \neq M$
$h_{11,n}$	$c_{11,0} = -\pi^{10}/449622835200$	if $n = M$
	$c_{11,m} = -\frac{(-1)^m}{4087480320m^{10}}\left(362880-60480m^2\pi^2+3024m^4\pi^4-72m^6\pi^6+m^8\pi^8\right)\big\vert_{m=n-M}$	if $n \neq M$

has no frequency components above $f_c/2$, it can be sampled at f_c without aliasing to obtain the sample values y_n. To simplify the presentation, it will be assumed that $f_s = f_c$. In short, the objective of the BBDFPWM algorithm is to compute d_n form x_n such that $y_n = x_n$.

The development of the algorithm is based on three steps. First, a discrete-time nonlinear model of the baseband behavior of the PWM that relates d_n to y_n is obtained [23]–[25] and an approximation to the exact model is introduced for real-time operation purposes. Second, the pulse width values d_n are derived from x_n using an iterative numerical method, and third, the numerical method is translated into an architecture suitable for on-line operation using standard FIR filters and some additional mathematical operations, such as additions and multiplications.

A. Nonlinear PWM Discrete-Time Model

The two-level PWM signal $p(t)$ switching between 0 and 1 can be represented using the step function $u(t)$ as [10], [25]

$$p(t) = \sum_{n=-\infty}^{\infty}\left[u\left(t - nT_s + d_n\frac{T_s}{2}\right) - u\left(t - nT_s - d_n\frac{T_s}{2}\right)\right] \tag{1}$$

where $d_n \in (0,1)$. If $p(t)$ is filtered with an ideal low-pass filter with cutoff frequency $f_c/2$ and impulse response $h_{LP}(t) = f_c\text{sinc}(f_c t) = f_c\sin(\pi f_c t)/(\pi f_c t)$, the signal $y(t) = h_{LP}(t) * p(t)$ (where "$*$" indicates convolution) is obtained. Uniformly sampling $y(t)$ at f_c results in the discrete-time output signal [24], [25]

$$y_n = \sum_{m=-\infty}^{\infty} f_m(d_{n-m}) \tag{2}$$

with

$$f_m(d) \triangleq \frac{\left(\text{Si}\left[m\pi + d\left(\frac{\pi}{2}\right)\right] - \text{Si}\left[m\pi - d\left(\frac{\pi}{2}\right)\right]\right)}{\pi} \tag{3}$$

where $\text{Si}(z) = \int_0^z \sin(\tau)/\tau d\tau = \int_0^z \text{sinc}(\tau/\pi)d\tau$ is the sine integral function.

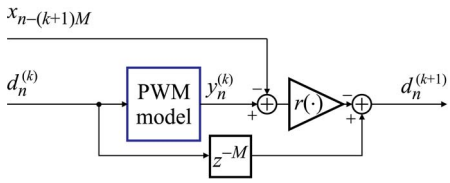

Fig. 4. Block representation of the kth iteration of (7). The block "PWM model" implements (6) [See Fig. 3(b)].

Equation (2) is a discrete-time nonlinear baseband model of the PWM modulation with the duty cycles d_n as input and the samples y_n as output. The computation of y_n using (2) requires knowing in advance the infinite set of duty cycles d_n, precluding real-time operation.

To reduce the complexity in the computation of y_n in (2) and to make a real-time implementation feasible, two simplifications are introduced: 1) the function $f_m(d)$ is approximated by its power series and 2) the infinite sum is truncated to $\pm M$ values.

The nonlinear function $f_k(d)$ can be approximated by the odd-power series

$$f_m(d) \approx \begin{cases} c_{1,0}d + c_{3,0}d^3 + \cdots + c_{P,0}d^P, & \text{if } m = 0, \\ c_{3,m}d^3 + \cdots + c_{P,m}d^P, & \text{if } m \neq 0 \end{cases} \tag{4}$$

where the coefficients $c_{i,m}$ are listed in Table I and P is the maximum power used for the approximation. Replacing (4) in (2), the output y_n can be approximated as

$$\begin{aligned} y_n \approx\, & c_{1,0}d_n + \sum_{m=-\infty}^{\infty}\left(c_{3,m}d_{n-m}^3 + \cdots + c_{P,m}d_{n-m}^P\right) \\ =\, & \cdots \quad + c_{3,-1}d_{n+1}^3 + \cdots + c_{P,-1}d_{n+1}^P \\ & + c_{1,0}d_n + c_{3,0}d_n^3 + \cdots + c_{P,0}d_n^P \\ & + c_{3,1}d_{n-1}^3 + \cdots + c_{P,1}d_{n-1}^P + \cdots . \end{aligned} \tag{5}$$

The second approximation consists in truncating the infinite summation in (5) to $m = \pm M$ values, making the current output sample value y_n dependent only on $N = 2M+1$ duty

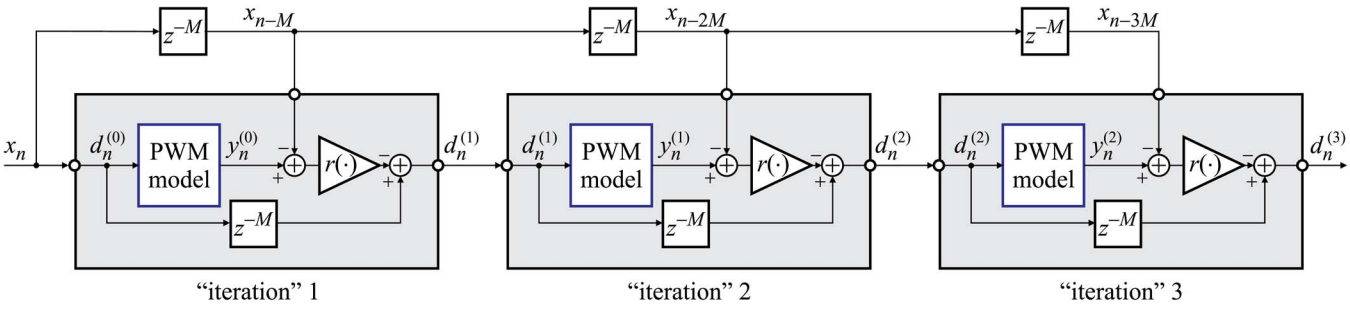

Fig. 5. Digital PWM modulator stages.

cycles d_n. Collecting the coefficients $c_{i,m}$ corresponding to the same power of d, the output sample y_n can be written as

$$y_n = \sum_{m=0}^{N-1} \sum_{i=1}^{(P+1)/2} h_{2i-1,m}(d_{n-m})^{2i-1}$$

$$= \sum_{m=0}^{N-1} \left[h_{1,m}d_{n-m} + h_{3,m}(d_{n-m})^3 + h_{5,m}(d_{n-m})^5 + \cdots + h_{P,m}(d_{n-m})^P\right]$$

that can be expressed as

$$y_n = h_{1,n} * d_n + h_{3,n} * d_n^3 + h_{5,n} * d_n^5 + \cdots + h_{P,n} * d_n^P \quad (6)$$

where "$*$" indicates discrete-time convolution and $h_{i,n}$ is a M-samples shifted version of $c_{i,n}$, i.e., $h_{i,n} = c_{i,n-M}$.

Each term of the sum in (6) represents the convolution of a filter with impulse response $h_{i,n}$ with the ith power of d_n. The impulse responses are symmetric around M, corresponding to Type I FIR filters of length $N = 2M + 1$ with constant group delay $\tau = M$. The impulses responses for powers $i = 1$ to $i = 11$ are listed in Table I.

The simplified PWM model in (6) can be represented as the block diagram of Fig. 3(b), which is generalized Hammerstein model where the ith branch is composed of a static nonlinearity $(\cdot)^i$ followed by an FIR filter with impulse response $h_{i,n}$ [26].

B. Computation of the Duty Cycles d_n

The duty cycles can be obtained numerically applying Newton's iterative method, for details see [24]. One way of approaching this solution is to use the scalar equation

$$d_n^{(k+1)} = d_n^{(k)} - r\left(d_n^{(k)}\right)\left[y_n^{(k)} - x_{n-(k+1)M}\right] \quad (7)$$

where $r(d_n) = [\mathrm{sinc}(d_n/2)]^{-1}$. Equation (7) can be represented as the block diagram shown in Fig. 4 which expresses the next iteration pulse-width value $d_n^{(k+1)}$ as the current iteration value $d_n^{(k)}$ corrected by the weighted difference between the current iteration output sample value $y_n^{(k)}$ and the input sample $x_{n-(k+1)M}$ that is delayed to take into account the constant group delay of the FIR filters in (6).

C. Algorithm Architecture

The structure of the algorithm is developed using (6) to compute the output sample y_n and (7) to compute the duty cycles $d^{(K)}$, where K is the number of iterations used in the actual implementation.

The algorithm consists of the cascade connection of certain number of blocks like the one represented in Fig. 4. The complete structure for three iterations is shown in the block diagram of Fig. 5. Because of the delay introduced by the FIR filters used in the discrete-time model of the PWM given by (6), the input sample values x_n are delayed by M samples in each iteration prior to the comparison with $y_n^{(k)}$. The first stage of the algorithm uses $d_n^{(0)} = x_n$, i.e., the duty cycles for the first iteration of the algorithm are the same values used in the SDEUPWM. The samples of the filtered output signal are computed using the generalized Hammerstein structure of the discrete-time baseband model of PWM depicted in Fig. 3(b).

The process is repeated K times: the duty cycle $d_n^{(k-1)}$ produced by the previous stage is used as the input of the following stage to compute $d_n^{(k)}$. In each stage, the magnitude $|y_n^{(k)} - x_{n-(k+1)M}|$ is reduced, diminishing the baseband distortion produced by the modulation process.

IV. Selection of Algorithm Parameters

Several parameters of the architecture developed in the previous section have to be selected for an actual DSP implementation. These parameters are: the length N of the FIR filters, the maximum odd power P used for the discrete-time nonlinear model of the PWM modulator, and the number of stages K of the iterative algorithm. Baseband distortion will be reduced for increased values of all these parameters, but the computational complexity will also be incremented. In this section, the performance of the algorithm is analyzed in terms of the total harmonic distortion plus noise (THD+N) as a function of N, P, and K.

A numerical simulation (parametric simulation) was performed for odd values of $9 \leq N \leq 99$, $3 \leq P \leq 13$, and for $1 \leq K \leq 4$. The duty cycles d_n that result from the algorithm are used as input to the PWM model of Fig. 3(b). The output samples y_n together with a delayed version of the modulating signal samples x_{n-KM} are used to compute the THD+N as the ratio between the RMS value of the error $y_n - x_{n-KM}$ and the RMS value of y_n

$$\mathrm{THD+N\ [dB]} = 20\log\left(\frac{\mathrm{RMS}\{y_n - x_{n-KM}\}}{\mathrm{RMS}\{y_n\}}\right)$$

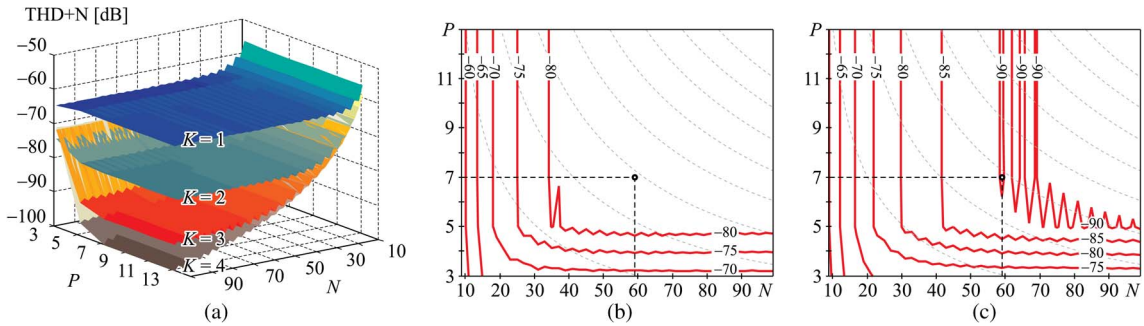

Fig. 6. Parametric simulation. (a) 3-D plot of THD + N [dB]; contour plot for $K = 3$: (b) band-limited random noise and (c) multitone signal.

which equals the logarithm of the ratio between the energy of the harmonics plus noise and the energy of the signal.

Parametric simulations were carried out for two different modulating signals x_n: a bandpass type random signal and a multitone signal. The random signal is generated by bandpass filtering Gaussian noise and the multitone signal is generated by adding nine sinusoids starting with frequency $1 \times 10^{-3} f_c$ and with each successive tone doubling its previous frequency (spaced in octaves).

Fig. 6 shows the result of the parametric simulation as a function of N, P, and K. Fig. 6(a) depicts the surfaces of THD+N in dB as a function of N and P for $K = 1, \ldots, 4$ for the random band-limited modulating signal. Although the THD+N reduces with each stage K of the algorithm, it is desirable not to increase this number, since each new stage uses the PWM model of Fig. 3(b), which requires the computation of $(P-1)/2$ FIR filters of length N.

No noticeable reduction of the distortion is achieved by increasing P above $P \approx 7$. The effect of P together with the effect of N on the THD + N [dB] can be observed more clearly on the contour plots of Fig. 6(b) and (c), which correspond to the random noise and multitone modulating signals, respectively, both for $K = 3$ stages (iterations). These pictures show the contour lines of the THD+N as a function of N and P. For both signals, a selection of N above 50 is adequate to achieve low levels of distortion with a moderated computational load.

The number of multiplications per sample $\mathcal{N}$ required to compute each duty cycle d_n as a function of N, P, and K is given by

$$\mathcal{N} = \frac{K}{4}(P-1)(N+1) + K. \tag{8}$$

For each of the K stages, $(P-1)/2$ symmetric FIR filter are computed requiring $(N+1)/2$ multiplications each. An additional multiplication is needed to weigh the difference $y_n^{(k)} - x_{n-(k+1)M}$. Fig. 6(b) and (c) also depicts, with dashed lines, the contour lines of $\mathcal{N}$ as a function of N and P and for $K = 3$ stages.

V. Comparison With Similar Approaches

The discrete-time PWM model represented by the generalized Hammerstein structure of Fig. 3(b) is similar to that presented in patent [22], but the method employed to reduce the distortion is different. Algorithm [22] is capable of a large reduction of PWM distortion with very low implementation cost if the relation between the PWM carrier frequency f_c and the maximum frequency of the modulating signal is very high $(f_c/f_m \gg 1)$. The result presented in [22, Fig. 18] achieves a reduction of ≈ 50 dB in the harmonic with higher amplitude when the ratio f_c/f_m is high. However, its efficiency decreases when the frequency ratio is reduced. Fig. 7 compares the spectra of the PWM produced with a typical SDEUPWM modulator together with those resulting from algorithm [22] and one and three stages of BBDFPWM modulators for a modulating sinusoidal signal of frequency $f_m = f_c/10$. In this case, algorithm [22] achieves a reduction of nearly 15 dB in the first harmonic. One stage of BBDFPWM achieves a slightly better reduction (20 dB), and three stages of BBDFPWM result in a dramatic reduction of the first harmonic in excess of 50 dB. The reduction is even larger for higher order harmonics.

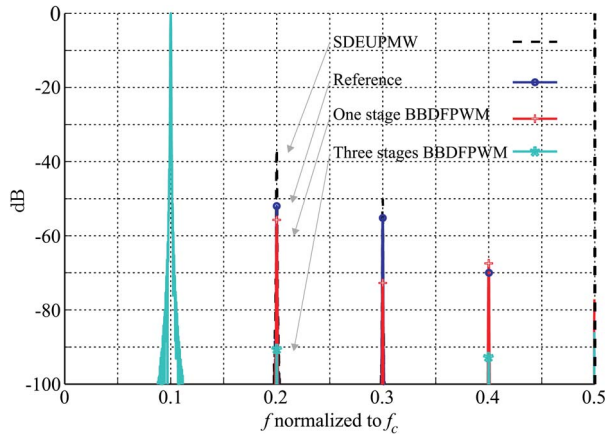

Fig. 7. Spectra of the PWM output. Comparison between BBDFPWM, SDEUPWM, and reference [22] under $f_c/f_m = 10$.

Algorithm [22], and other similar approaches [27], [28] (usually known as pseudo-natural PWM because they imitate the behavior of analog or natural PWM, which exhibits less distortion that uniform PWM) are able to reduce PWM distortion when the frequency ratio f_c/f_m is large, but their performance decreases when the frequency ratio is reduced. On the other hand, BBDFPWM achieves a uniform performance for the entire baseband $[0, f_c/2)$, with a higher implementation or computational cost. However, a higher order version of algorithm [22] "rapidly becomes complicated in terms of calculation" [22, p. 27], while the modular structure of BBDFPWM allows for easy tradeoff between performance and computational cost.

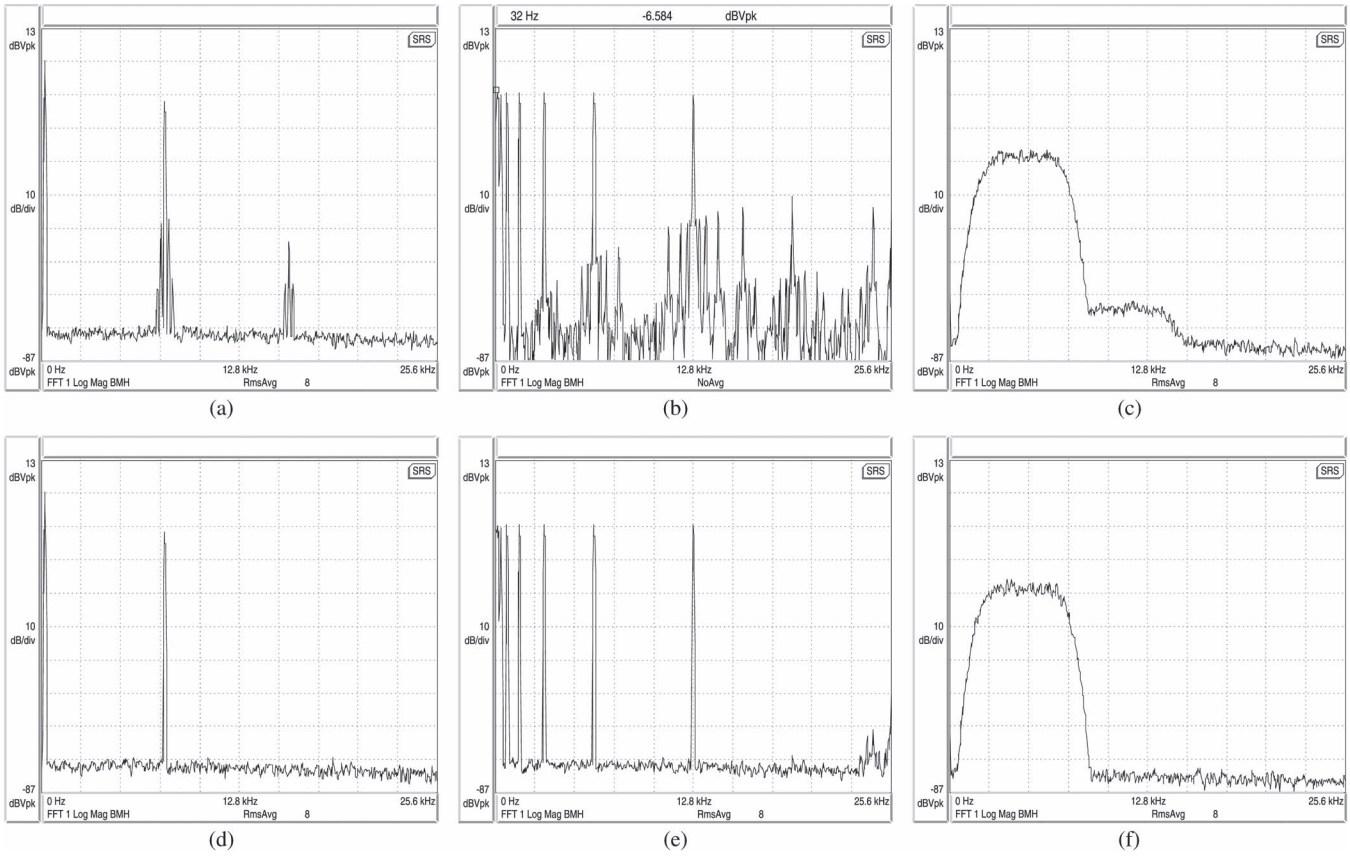

Fig. 8. Spectral measurements of (a) IMD with SDEUPWM; (b) multitone with SDEUPWM; (c) band-limited noise with SDEUPWM; (d) IMD with BBDFPWM; (e) multitone with BBDFPWM; (f) band-limited noise with BBDFPWM.

VI. DSP Implementation and Measurements

The architecture of the BBDFPWM algorithm described by the block diagrams of Figs. 3(b) and 5 was implemented on a low-cost TMS320F28335 DSP to evaluate its real-time behavior. The nonlinear function $r(d_n)$ in (7) is computed using a look-up table and the FIR filters are implemented using a library provided by the manufacturer. No other special signal processing tools are required, making the implementation of the algorithm rather straightforward.

The pulse former block in Fig. 1 is implemented with the standard PWM module of the DSP using an up/down counter at a switching frequency of $f_c = 50$ kHz that coincides with the input signal sampling frequency, $f_s = f_c$. The PWM resolution is fixed by the relation between the PWM frequency $f_c = 50$ kHz and the DSP clock frequency $f_{clk} = 150$ MHz, which results in $b = \log_2(f_{clk}/f_c) \approx 11.55$ bits. Although this resolution will limit the performance of the current implementation, it is sufficient to show the improvements produced by the modulation strategy. The PWM resolution is a typical problem of all digital implementations of PWM algorithms; although this issue is out of the scope of this work, several alternatives to increase the resolution without augmenting the clock frequency are available in the literature [29], [30]. Noise-shaping techniques, that displace the quantization noise out of the band of interest, can also be applied [31].

Based on the analysis in Section IV and taking into account the limited resolution of the PWM modulator (which introduces a THD+N of around -80 dB), the parameters of the algorithm are selected as: $K = 3$ stages, with an approximation of order $P = 7$, and FIR filters of length $N = 59$. The operating point marked with a dot in Fig. 6 results in an expected THD+N exceeding -80 dB (0.01%).

A. Spectral Measurements

Different types of band-limited signals with frequency content below $f_c/2 = 25$ kHz were used to test the performance of the algorithm. The PWM signal $p(t)$ is measured at an output pin of the DSP using an spectrum analyzer.

First, intermodulation distortion measurements (IMD) are carried out using DIN standard 45403 [32]. The modulating signal is composed of low- and high-frequency sinusoids of $f_1 = 250$ Hz and $f_2 = 8$ kHz, respectively, where the latter has an amplitude 12.04 dB lower than the former. Due to the nonlinear nature of SDEUPWM, intermodulation products will appear at frequencies $\alpha f_1 \pm \beta f_2$ (α and β integers); it is expected that BBDFPWM removes all this components within the baseband. The baseband spectra measured for SDEUPWM and for BBDFPWM are depicted in Fig. 8(a) and (d), respectively. For SDEUPWM, four sidebands of the 8 kHz tone are observed at $f_2 \pm f_1$ and $f_2 \pm 2f_1$, and a harmonic at $2f_2 = 16$ kHz and its sidebands at $2f_2 \pm f_1$ are also detected. The proposed algorithm completely removes these spurious intermodulation products. Only the noise floor 80 dB below the amplitude of the input at f_1 is observed.

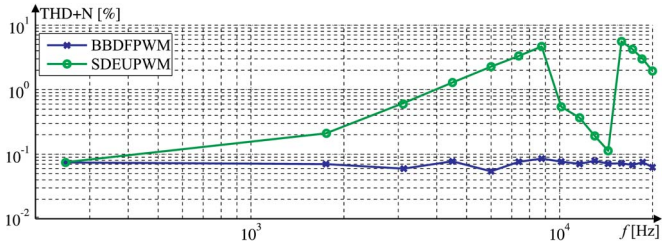

Fig. 9. THD + N measurement with the standard SDEUPWM and with BBDFPWM.

Second, a multitone signal (usually used for equipment testing [32]) composed of the sum of nine sinusoids beginning with $f = 50$ Hz and reaching 12.8 kHz spaced in octaves was also used for testing. The measured spectra are shown in Fig. 8(b) and (e) for SDEUPWM and BBDFPWM, respectively. The improvement is noteworthy since only the modulating signal tones can be observed in the output spectrum of BBDFPWM. For the SDEUPWM, several spurious tones contaminate the baseband.

The last test signal is random noise with Gaussian distribution and bandpass filtered between 200 Hz and 10 kHz. This kind of signal can be used to model an audio signal driving a class-D amplifier. The spectral measurements are shown in Fig. 8(c) (SDEUPWM) and Fig. 8(f) (BBDFPWM) revealing that the BBDFPWM algorithm eliminates the spectral regrowth that appears between 9 kHz and 15.3 kHz when SDEUPWM is used.

These experiments show that the BBDFPWM modulation algorithm is able to eliminate baseband distortion, or at least making it negligible, with a level well under the quantization noise level of the PWM resolution.

B. THD + N Measurements

For this test a spectrally pure sinusoidal signal is modulated using SDEUPWM and BBDFPWM. The frequency of the test tone is varied between 250 Hz and 20 kHz. The THD + N is measured with the spectral analyzer as the quotient between the power of the harmonics plus noise and the power of the complete signal (sinusoidal signal plus harmonics and noise).

The THD + N measurements are depicted in Fig. 9 for both modulation algorithms. It can be observed that the THD+N remains almost flat, with a value of approximately 0.07% for the entire frequency band for BBDFPWM. The irregular behavior of the THD + N curve for the SDEUPWM between 9 kHz and 15 kHz, with a maximum of 5.58%, occurs because the harmonics of the modulating signal appear outside the baseband, where the measurement is performed. For frequencies above 15 kHz, the lateral sidebands of the carrier began to appear within the baseband, increasing the THD + N. These behavior does not occur with the BBDFPWM algorithm since not only the modulating signal harmonics are eliminated but also the carrier sidebands are removed from the baseband.

The flat behavior of the THD + N measurement in an actual implementation achieved even for low switching frequencies was previously obtained only using click modulation [17], [19], [33]. Those implementations are computationally demanding requiring either more than one DSP or FPGA, reducing the usable audio frequency range or restricting their operation to offline computation. The proposed approach uses FIR filtering and does not require other advanced processing tools such as an analytic exponential modulator or zero crossing point estimation which are building blocks of click modulation. Other digital PWM methods such as the one reported in [22], reviewed in Section V, and the ones based on crossing point estimation (pseudo-natural PWM) [28] require a very high switching frequency to avoid that carrier sidebands fall into baseband and hence to guarantee low distortion in the whole audio band.

VII. Conclusion

A real-time digital PWM modulating algorithm with zero (or reduced) distortion in the baseband was developed in this paper. The residual distortion depends mainly on the number of bits of the PWM resolution. An actual DSP implementation was developed and the algorithm was tested with different band-limited signals showing that it is able to achieve the design objectives with a reduced computational load. Experimental results reveal that the BBDFPWM modulator clearly outperforms the traditional SDEUPWM. These characteristics may be of interest for high-quality, high-efficiency power converters, or class-D amplifiers.

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