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# Inadequacy of the Mott–Schottky equation in strongly pinned double Schottky barriers with no deep donors

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## Abstract

The capacitive behaviour of an intergranular double Schottky barrier in a polycrystalline semiconductor was evaluated. We found that the widely applied version of the Mott–Schottky equation can lead to significant errors. Even though we considered strong Fermi level pinning at the interface and no deep levels, the Mott–Schottky equation can be inadequate leading to huge errors due to voltage splitting at double Schottky barriers. Experiments carried out on ZnO varistors corroborated the main trends of our analysis.

(Some figures may appear in colour only in the online journal)

## 1. Introduction

Electrical properties of polycrystalline semiconductors are known to be dominated by potential barriers at the grain boundaries [1–3]. Consistently, the high resistivity exhibited at low applied voltages derives from grain boundaries since grains are very conductive. At high enough applied voltages, a breakdown of these intergranular barriers takes place. Then, the conductivity rapidly increases in a narrow range of the applied voltage. This characteristic is exploited in metal-oxide varistors, used for circuit protection [4–9]. Potential barriers are caused by intergrain states that may arise due to the presence of impurity or additive atoms, or to dislocations introduced by the crystallographic mismatch between adjacent grains, or because of an interface layer, which is another oxide. Regardless of their origin, interface states deplete carriers from surrounding grains leading to the formation of double Schottky barriers [10–12].

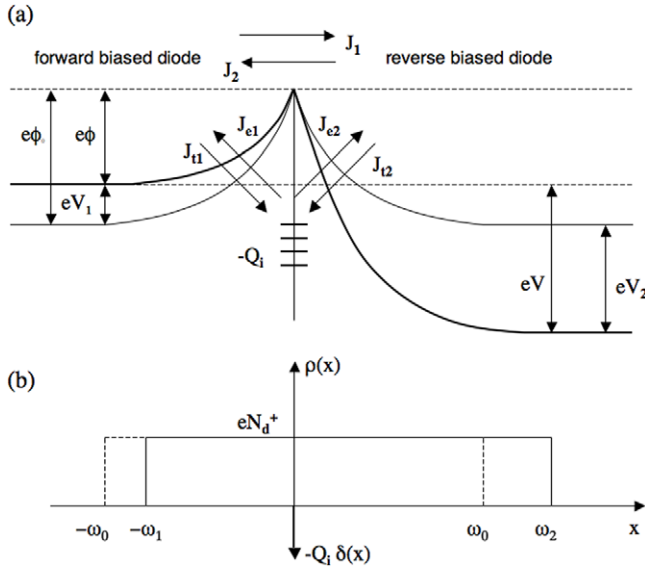
Zinc and tin oxides are intrinsic n-type semiconductors that exhibit oxygen vacancies with the behaviour of shallow donor impurities. The interfacial region is relatively thin and the depletion of majority carriers leaves ionized defects at close grains that screen the charge accumulated at the interface. The presence of charged depletion layers has been demonstrated by means of capacitance–voltage measurements that are widely used to characterize the electrical properties of the intergrains. Even though several observed complexities indicate that a simple parallel resistor–capacitor circuit is not enough to model

all the involved phenomena [13], the Mott–Schottky approach as proposed by Mukae *et al* is regularly used to determine barrier heights and donor concentrations [14].

In this work, we showed that, additionally to other complexities, the applied voltage splitting between the direct and inverse polarized barriers at intergrains can lead to significant errors. In particular, this can take place for the simplest case of strongly pinned double Schottky barriers with no deep donors. The proposed analysis leads to the observed experimental trends.

## 2. Double Schottky barrier model and Mukae's approximation

Usually, the electrical properties of polycrystalline semiconductors are described with a simple one-dimensional model representing the interface between two grains. Figure 1(a) depicts the conduction band for a double Schottky barrier model that is generally accepted [1, 15, 16]. The scheme shows an n-type semiconductor junction with and without a voltage applied across the grain boundary. In doing so, we chose to maintain the interface with the same potential; the applied voltage drops partly at the left grain,  $V_1$ , and partly at the right grain,  $V_2$ . Figure 1(b) shows the charge distribution. Charged donors at both grains generate an electric field and then band bending. Additional screening of the interface charge could be provided by deep states but we will not include them in this work. We



**Figure 1.** Energy-band diagram for the double-depletion-layer model. The diagram shows schematically the basic features of an n-type semiconductor interface when a voltage is applied (dark line) and when no voltage is applied (light line). (a) After a voltage  $V$  was applied across the grain boundary,  $V_1$  and  $V_2$  are the voltage drops at the left grain and at the right grain, respectively.  $Q_i$  is the charge trapped at the boundary. (b) Charge distribution at the double Schottky barrier.  $\omega_0$  is the width of the depletion regions when there is no applied voltage;  $\omega_1$  and  $\omega_2$  are the widths of the depletion regions when the voltage  $V$  is applied to the intergrain.

have assumed that the width of the interfacial region is very small to justify its idealization as an infinitely thin layer with a total charge  $-Q_i$ .

Figure 1 indicates that shallow donors, with density  $N_d$ , are everywhere ionized and are homogeneously distributed along the grains. As seen in figure 1(b), the free carrier concentration is assumed to be negligible within the depletion regions that are then perfectly well defined: between  $-\omega_0$  and  $\omega_0$  for the double barrier without an applied voltage and between  $-\omega_1$  and  $\omega_2$  when a voltage  $V$  is applied. The characteristics of the Schottky-type barriers at the intergrains could be inferred from the applied voltage dependence of the capacitance. This is regularly carried out using the approach of Mukae *et al*, as described below [14].

The capacitance per unit area of a Schottky barrier is given by

$$C = \left( \frac{e\epsilon N_d}{2\phi} \right)^{1/2}, \quad (1)$$

where  $e$  is the electron charge,  $\epsilon$  is the permittivity,  $N_d$  is the donor concentration and  $e\phi$ , given in eV, is the barrier height. Strictly, the Schottky barrier height should be defined as the difference between the top of the barrier and the Fermi level [17]. However, many researchers in the field define the barrier height as the band bending, i.e. the difference between the top of the barrier and the bottom of the conduction band in the bulk [11, 12, 18]. In figure 1, we adopted this second convention. In a double Schottky barrier, such as that of figure 1, the total capacitance for the intergrain results from two capacitances in series, corresponding to a forward and a

reverse biased barrier,

$$\frac{1}{C_i} = \left( \frac{2}{e\epsilon N_d} \right)^{1/2} [(\phi_0 - V_1)^{1/2} + (\phi_0 + V_2)^{1/2}], \quad (2)$$

where  $eV_1$  and  $eV_2$  are the decrease and increase of the barriers for the forward and reverse biased grains, respectively. By assuming that the forward biased barrier modification is negligible,  $V_2$  is approximately equal to  $V$ , the total applied voltage. Thus, equation (2) becomes

$$\left( \frac{1}{C_i} - \frac{1}{2C_0} \right)^2 = \frac{2}{e\epsilon N_d} (\phi_0 + V), \quad (3)$$

where

$$\frac{1}{C_0} = 2 \left( \frac{2\phi_0}{e\epsilon N_d} \right)^{1/2}. \quad (4)$$

$C_0$  is the capacitance for no applied voltage.

For  $n$  intergrains in series the total capacity is  $C = C_i/n$  and the total applied voltage is  $V_t = nV$ . Then, equation (3) becomes

$$\left[ \frac{1}{C} - \left( \frac{2n^2\phi_0}{e\epsilon N_d} \right)^{1/2} \right]^2 = \frac{2n^2}{e\epsilon N_d} (\phi_0 + V_t/n). \quad (5)$$

This equation is regularly used to determine the barrier height and the dopant concentration in polycrystalline materials. By plotting the left-hand term of equation (5) versus the applied voltage, a straight line should be obtained. Then, knowing the average number of grains between electrodes,  $N_d$  and  $\phi_0$  can be found from the slope and the intercept of the line on the voltage axis. This analysis is based on the assumption that the applied voltage drops completely at the reverse biased diode. This assumption implies that the density of states at the interface is large enough so that the quasi-Fermi level at the interface does not significantly change when the interface charge density increases (Fermi level pinning) [19]. The interface charge  $Q_i$  is determined by the density of states at the interface and the quasi-Fermi level.

Regularly it is considered that the carrier transport through the grain boundary is thermionic. If so, the electron current density from the negatively biased grain to the positively biased grain would be

$$J_1 = AT^2 \exp[-(e\phi + \xi)/kT], \quad (6)$$

where  $A$  is the Richardson constant,  $T$  is the temperature,  $k$  is the Boltzmann constant, and  $\xi$  is the difference between the conduction band minimum and the Fermi level. There is also a current density,  $J_2$ , flowing in the opposite direction of the same form as equation (1) but reduced by a factor  $\exp(-eV/kT)$ . A fraction of these currents, say  $c$ , is trapped and re-emitted by the interface states.

In steady state, the total current flowing from the grains towards the interface must cancel with the total current flowing from the interface towards the grains. Next, we will follow the analysis of [20]. For  $V = 0$ , the activation energy for transport from the interface to the grain and vice versa is  $e\phi_0$ . Thus, the emitted currents are

$$J_{e1,2} = cAT^2 \exp[-(e\phi_0 + \xi)/kT]. \quad (7)$$

The total trapped current density is

$$J_t = J_0 \exp(-e\phi/kT)[1 + \exp(-eV/kT)], \quad (8)$$

and the total re-emitted current density is  $J_e = J_{e1} + J_{e2}$

$$J_e = 2J_0 \exp(-e\phi_0/kT), \quad (9)$$

where

$$J_0 = cAT^2 \exp(-\xi/kT). \quad (10)$$

Trapped and re-emitted currents modify the interface charge  $Q_i$  when the external bias  $V$  is changed and determine the voltages  $V_1$  and  $V_2$  (see figure 1). This model predicts that  $\phi$  changes only slightly with the applied voltage. In fact, in steady state  $J_t = J_e$ :

$$J_0 \exp(-e\phi/kT)[1 + \exp(-eV/kT)] = 2J_0 \exp(-e\phi_0/kT). \quad (11)$$

Equation (11) leads to

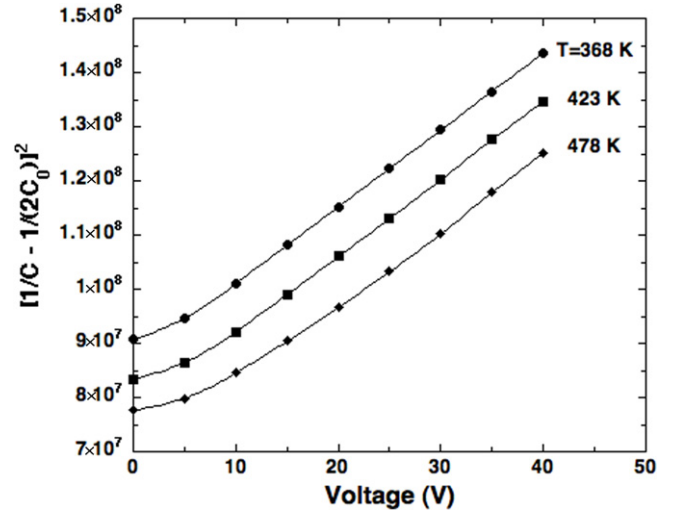
$$\exp(eV_1/kT) + \exp[-eV_2/kT] = 2. \quad (12)$$

For  $eV \gg kT$ ,  $\exp(-eV_1/kT) = 2$  and  $\phi = \phi_0 - (kT/e) \ln 2$ , independent of the applied voltage. The double Schottky barrier is very one sided, with most of the applied voltage dropping at the reversed biased diode. These calculations indicate that Mukae's approximation would be applicable.

### 3. Experiments

In this work, experimental measurements made on a commercial ZnO-based varistor GNR07D680 are reported. We found that features for varistors of the same type present varying characteristics. Then, we used the same varistor for a complete set of measurements. Capacitance measurements were carried out with a Hewlett-Packard impedance analyser model 4184A. A furnace, with a commercial temperature controller Novocontrol BDS 1200, was used for heating the sample.

Figure 2 shows the measured capacitance at 1 MHz, a typically used frequency, as a function of the applied voltage, as suggested in equation (5). The varistor thickness was measured with an optical microscope ( $\approx 1.14$  mm) and, from SEM images, the average grain size was determined to be  $\approx 35.4 \mu\text{m}$ . Thus, the average number of grains was  $n \approx 32$ . By fitting the curves of figure 2, with straight lines for an applied voltage greater than 20 V, we could determine the barrier heights from the slope and intercept of the line on the voltage axis using Mukae's method, equation (5). The barrier heights resulted to be 1.92 eV, 1.67 eV and 1.42 eV for  $T = 368$  K, 423 K and 478 K, respectively. These values are consistent with those found by other authors using the same method [21–24]. However, barrier heights determined based on sample conductivity are typically in the range 0.4–0.9 eV [25–28]. On the other hand, the barrier should not be strongly dependent on temperature as determined because we are dealing with a sealed polycrystalline sample that is not in contact with the atmosphere and then the amount of oxygen at the intergrains is not expected to change. Note



**Figure 2.** Mott-Schottky behaviour for a commercial varistor GNR07D680 at three temperatures. From these plots the barrier heights were determined: 1.92 eV, 1.67 eV and 1.42 eV for  $T = 368$  K, 423 K and 478 K, respectively.

that temperatures were kept in a range for which device degradation does not occur. The main assumption in Mukae's approximation consists in considering that the applied voltage does not modify the forward biased barrier, which has been questioned as shown below.

### 4. Barrier height dependence on applied voltage

Several researchers have proposed that the barrier height depends on the applied voltage. The barrier height has been considered to decrease with the applied voltage as [28, 29]

$$e\phi = e\phi_0 - \beta E^{1/2}, \quad (13)$$

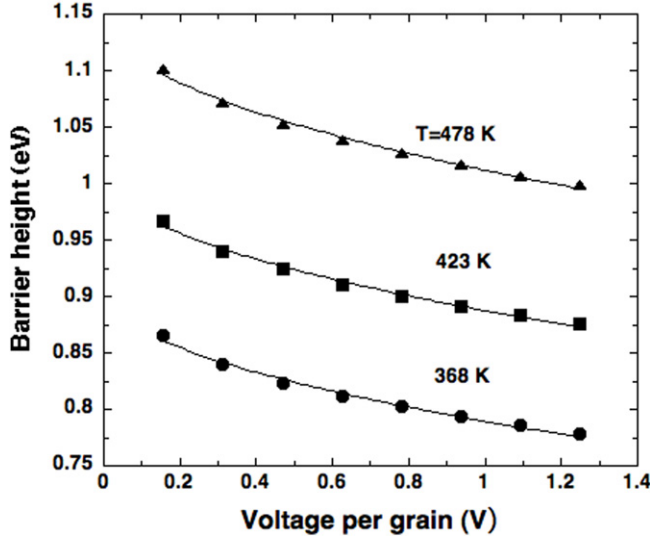
where  $E$  is the applied field.

Blatter and Greuter presented a detailed analysis of the possible dependence of the barrier height on the applied voltage as a consequence of a finite density of interface states. That is, the quasi-Fermi level at the interface can move in the gap [12]. They found that the steady-state current across a grain boundary depends significantly on the states at the intergrain. With the applied voltage, the interface charge  $Q_i$  increases as more interface states become occupied. Thus, depending on the density and energy distribution of interface states, the quasi-Fermi level at the interface would be pinned to varying degrees.

Experimentally, the reduction in barrier can be derived from the current density–voltage characteristics. The current density increase with the applied voltage implies that, according to a thermionic carrier transport, the barrier height is a decreasing function of the applied voltage. The barrier height as a function of the applied voltage can be derived from equation (6):

$$e\phi(V) = -kT \ln \frac{J}{AT^2}. \quad (14)$$

In figure 3, we present the resulting barrier heights as a function of applied voltage for  $T = 368$ , 423, and 478 K,



**Figure 3.** Barrier heights calculated from measured currents as a function of the applied voltage for  $T = 368, 423$  and  $478$  K, for a commercial varistor GNR07D680. Lines correspond to fittings using equation (14) assuming thermionic transport.

applying equation (14). Filled lines correspond to fittings using the dependence shown in equation (13). The quality of the fitting indicates that the proposed function is applicable in our experimental results.

The reduction in barrier height,  $e\Delta\phi = \beta E^{1/2}$  reflects in the capacitance of the intergrain as it affects the forward and reverse biased barriers. Accordingly, the intergrain capacitance can be expressed as

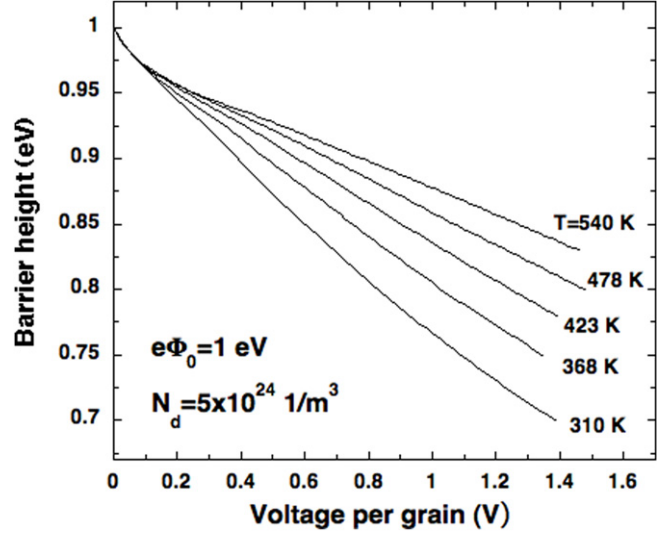
$$\frac{C_i}{C_0} = \frac{2}{\left[ \left(1 - \frac{\Delta\phi}{\phi_0}\right)^{1/2} + \left(1 + \frac{V - \Delta\phi}{\phi_0}\right)^{1/2} \right]}. \quad (15)$$

Knowing the intergrain capacitance dependence with the applied voltage, obtained with equation (15), we can apply Mukae's approach, equation (3), to derive the barrier height  $e\phi_0$ . The resulting values are 0.91 eV, 1.01 eV and 1.152 eV for  $T = 368$  K, 423 K and 478 K, respectively. These findings disagree with those determined experimentally. Even worse, the temperature dependence is wrong. These results indicate that one or more assumptions in this analysis are not correct. In the next section, we introduce a different approach considering that the barrier height  $e\phi$  reduces not due to a finite density of states at the intergrain but as a consequence of the extension of the argument given in section 2, including the thermionic-field emission contribution in the electronic transport through the intergrain barrier.

## 5. Applied voltage splitting at the double barrier

The analysis leading to equation (12) can be extended to incorporate thermionic-field emission or tunnelling contributions, which can be calculated using

$$J_{\text{tunneling}} = \frac{AT}{k} \int_0^\phi F(E)P(E) dE. \quad (16)$$



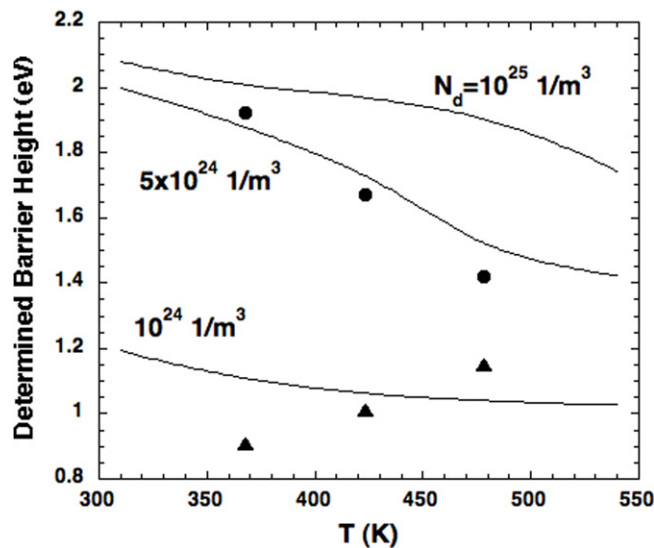
**Figure 4.** Barrier heights as a function of the applied voltage deduced by considering that the total current flowing from the grains towards the interface must cancel with the total current flowing from the interface towards the grains. Tunnelling contributions were included. The Fermi level was assumed to be pinned at the interface and deep levels were not considered.

$F(E)$  is the Fermi–Dirac distribution and  $P(E)$  is the transmission probability, which can be determined by means of the Wentzel–Krammer–Brillouin (WKB) approximation [30–32]. Similarly, as done in section 2, we can figure out the trapped and re-emitted current densities. We have performed these calculations under different values of the relevant parameters by keeping the total trapped and re-emitted current densities equal, as expected under a steady-state condition. We found that, in general, most of the applied voltage drops at the reverse biased diode. However, as tunnelling contributions increase,  $V_1$  becomes a larger fraction of the total applied voltage and then the barrier height reduces with the applied voltage. Note that in this approach we consider that the density of states at the interface is high enough to pin the quasi-Fermi level at the interface.

Figure 4 shows the resulting barrier height  $e\phi$  as a function of the applied voltage per grain with temperature as a parameter, for  $e\phi_0 = 1$  eV and a doping  $N_d = 5 \times 10^{24} \text{ m}^{-3}$ . The barrier height decreases faster at lower temperatures, a consequence of the relatively higher contributions of the tunnelling currents. The applied voltage splitting determines the capacitance of the double barrier according to equation (2). Once the capacitance as a function of the applied voltage is calculated, we can determine the barrier height using Mukae's method. Figure 5 shows those results for three different dopings (filled lines). It is interesting to note that the lower the doping, the lower the influence of the tunnelling currents. In fact, a lower doping and a higher temperature reduce the influence of the tunnelling currents and then Mukae's method works better.

In figure 5, we have also included the barrier heights obtained from the experimental results of figure 2. Given the assumptions and unknowns in our modelling, it was not our goal to find the best set of parameters to adjust those findings.





**Figure 5.** Determined barrier heights using Mukae's method as a function of temperature. Lines correspond to the model based on equating the currents flowing from the grains towards the interface with the total current flowing from the interface towards the grains, figure 4. Calculations were performed for three dopant concentrations. Filled circles correspond to the experimental results of figure 2 using a commercial varistor GNR07D680. Filled triangles correspond to the application of Mukae's method to the results of figure 3, in which the electronic transport was assumed to be thermionic.

However, it was found that the trends are reproduced well for a doping of  $N_d = 5 \times 10^{24} \text{ m}^{-3}$  and a barrier height  $e\phi_0 = 1 \text{ eV}$ , which are regularly reported values. Figure 5 also shows the barrier heights calculated assuming a thermionic current and a barrier height dependence given by equation (13). As said before, this approach leads to inconsistencies.

It is important to stress that these methods could be valid as long as the model of figure 1 is applicable. For small grains and/or low doping, grains can be completely depleted and then the voltage capacitance dependence cannot be described based on the scheme of figure 1. Even before total depletion, the one-dimensional character of the interface is lost and the current models are not valid.

## 6. Conclusions

We have shown that the widely applied version of the Mott-Schottky equation can lead to huge errors in the determination of barrier heights in polycrystalline semiconductors. We propose that voltage splitting at double Schottky barriers, a consequence of tunnelling currents, can contribute to parameter falsification in applying Mukae's method. Interestingly, strong quasi-Fermi level pinning at the interfaces does not guarantee the applicability of Mukae's method. Experiments carried out on ZnO varistors confirmed the main trends derived from the approach in which we considered tunnelling contributions to electronic transport and that the density of states at the interface is high enough to pin the quasi-Fermi level at the interface.

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## References

- [1] Seitz M, Hampton F and Richmond W 1983 *Advanced in Ceramics* vol 7, ed M F Yan and A H Heuer (Columbus, OH: The American Ceramic Society Inc) pp 60–70
- [2] Madou M J and Morrison R 1989 *Chemical Sensing with Solid State Devices* (San Diego, CA: Academic)
- [3] Moseley P T 1992 *Meas. Sci. Technol.* **8** 223
- [4] Levinson L M and Philipp H R 1986 *Am. Ceram. Soc. Bull.* **65** 639
- [5] Gupta T K 1990 *J. Am. Ceram. Soc.* **73** 1818
- [6] Bui A, Nguyen H T and Loubiere A 1995 *J. Phys. D: Appl. Phys.* **28** 774
- [7] Ramirez M A, Cilense M, Bueno P R, Longo E and Varela J A 2009 *J. Phys. D: Appl. Phys.* **42** 015503
- [8] Parra R, Ponce M A, Aldao C M and Castro M S 2007 *J. Eur. Ceram. Soc.* **27** 3907
- [9] Lu Z Y, Glot A B, Ivon A I and Zhou Z Y 2012 *J. Eur. Ceram. Soc.* **32** 3801
- [10] Seager C H and Pike G E 1980 *Appl. Phys. Lett.* **37** 747
- [11] Pike G E 1984 *Phys. Rev. B* **30** 795
- [12] Blatter G and Greuter F 1986 *Phys. Rev. B* **33** 3952
- [13] Ponce M A, Castro M S and Aldao C M 2009 *J. Mater. Sci.: Mater. Electron.* **20** 25
- [14] Mukae K, Tsuda K and Nagasawa I 1979 *J. Appl. Phys.* **50** 4475
- [15] Barsan N and Weimar U 2001 *J. Electroceram.* **7** 143
- [16] Barsan N, Koziej D and Weimar U 2007 *Sensors Actuators B* **121** 18
- [17] Sze S M 1981 *Physics of Semiconductor Devices* (New York: Wiley) chapter 5
- [18] Fernández-Hevia D, de Frutos D J, Caballero A C and Fernández J F 2002 *J. Appl. Phys.* **92** 2890
- [19] Maffei T G G, Owen G T, Malagù C, Martinell G, Kennedy M K, Kruis F E and Wilks S P 2004 *Surf. Sci.* **550** 21
- [20] Aldao C M, Mirabella D A, Ponce M A, Giberti A and Malagù C 2011 *J. Appl. Phys.* **109** 063723
- [21] Fan J and Freer R 1995 *J. Appl. Phys.* **77** 4795
- [22] Bueno P R, Oliveira M M, Bacelar-Junior W K, Leite E R, Longo E, García-Belmonte G and Bisquert J 2002 *J. Appl. Phys.* **91** 6007
- [23] Vasconcelos J S, Vasconcelos N S L S, Orlandi M O, Bueno P R, Varela J A, Longo E, Barrado C M and Leite E R 2006 *Appl. Phys. Lett.* **89** 152102
- [24] Bernik S and Daneu N 2001 *J. Eur. Ceram. Soc.* **21** 1879
- [25] Levinson L M 1989 *Ceramic Transactions, Advances in Varistor Technology* vol 3 (Westerville, OH: The American Ceramic Society, Inc)
- [26] Mahan G D, Levinson L M and Philipp H R 1979 *J. Appl. Phys.* **50** 2799
- [27] Dhage S R, Choube V and Ravi V 2004 *Mater. Sci. Eng. B* **110** 168
- [28] Antunes A C, Antunes S R M, Pianaro S A, Longo E, Leite E R and Varela J A 2001 *J. Mater. Sci.: Mater. Electron.* **12** 69
- [29] Ramírez M A, Simões A Z, Márquez M A, Maniette Y, Vavalheiro A A and Varela J A 2007 *Mater. Res. Bull.* **42** 1159
- [30] Crowell C R and Rideout V L 1969 *Solid State Electron.* **12** 89
- [31] Castro M S and Aldao C M 1993 *Appl. Phys. Lett.* **63** 1077
- [32] Malagù C, Carotta M C, Giberti A, Guidi V, Martinelli G, Ponce M A, Castro M S and Aldao C M 2009 *Sensors Actuators B* **136** 230