Experimental results for cascadable micropower time delay estimator

P. Julián, F.N. Martin Pirchio and A.G. Andreou

Experimental results of a micropower integrated circuit (IC) for the measurement of the relative time delay between two signals are presented. A complete experimental characterisation shows that the IC achieves an accuracy of 3 μs in the whole measurement range with a power consumption of 12 μW. This improves on all low-power designs previously reported in the literature.

Introduction: This Letter presents experimental results of a micropower integrated circuit (IC) for the measurement of the relative time delay between two signals. The IC was developed in the context of a project for the localisation of an acoustic sound source in a network of energy aware sensors. Accordingly, an extended useful life was desirable. This led to a minimum power consumption design. The approach is inspired by the discrete time correlation [1] method, but uses the derivative of the correlation function to minimise the activity of the circuitry (see [2, 3]). Other approaches with IC realisations exist in the literature, like the gradient flow method [4] and the neuromorphic approaches described in [5–7]. In particular, the approaches [3–5] have been evaluated in a common framework in [2], and the feasibility of achieving an accuracy close to one degree under normal levels of outdoor noise has been shown.

This Letter presents a complete experimental characterisation that shows that the IC achieves an accuracy of less than 3 μs in the whole measurement range (using an internal bi-phase clock of 200 kHz) and a power consumption of 12 μW. This is lower than the result reported in [4] for a similar accuracy.

Circuit description: The IC is a modified and improved version of a previously presented design [2], which had 10 bits precision, a built-in state machine, a fixed range of measurement (104 delay stages) and a fixed calculation time of 1 s. The new design has a clock distribution tree optimised for power consumption, one more bit precision (11 bits), and a total of 64 delay stages. There is a main clock buffer to drive the flip–flop (FF) chains, and every row has also a block that drives the 11 bit up/down counter (see Fig. 1). The calculation time is set externally, and control and data signals have been added to drive a similar unit. Therefore, several units can be cascaded to achieve an extended measurement range.

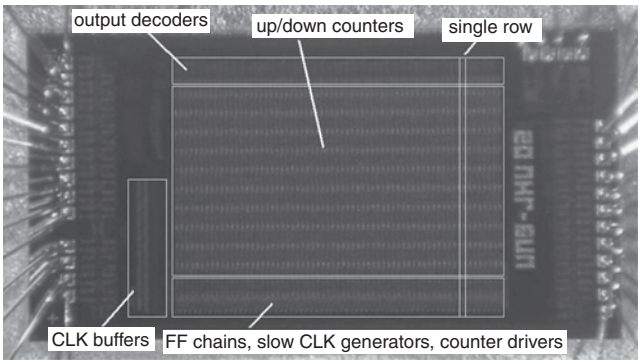

Fig. 1 *Chip photograph*

The IC was fabricated through the MOSIS service in a 0.5 μm standard CMOS process and occupies 1.5 × 3 mm (including pads). At 3.3 V power supply and 200 kHz internal clock, the IC has a total power consumption of 45 μW, which results in a power consumption per delay stage of 703 nW. At 2 V power supply and 200 kHz internal clock, the IC operates correctly and has a power consumption of 12 μW, which results in a power consumption per delay stage of 187.5 nW.

Experimental results: For the experiments, a 400 kHz ceramic resonator based oscillator was used to produce the IC clock signal (an internal clock generator produces a 200 kHz bi-phase clock) and the two input signals were generated using an independent (not synchronised) signal generator of 100 Hz. An acquisition board PMD1608FS was programmed to sample the data bus once every 0.1 s, reset the IC and repeat this cycle 100 times for every value of reference delay. In the first experiment, the delay between input signals was varied from 50 to 60 μs in steps of 1 μs. Fig. 2 shows mean and standard deviation of the measured values. The measurement mean coincides with the reference for integer multiples of the clock period, and the difference is maximum halfway between clock periods. This effect can be clearly appreciated in Fig. 2.

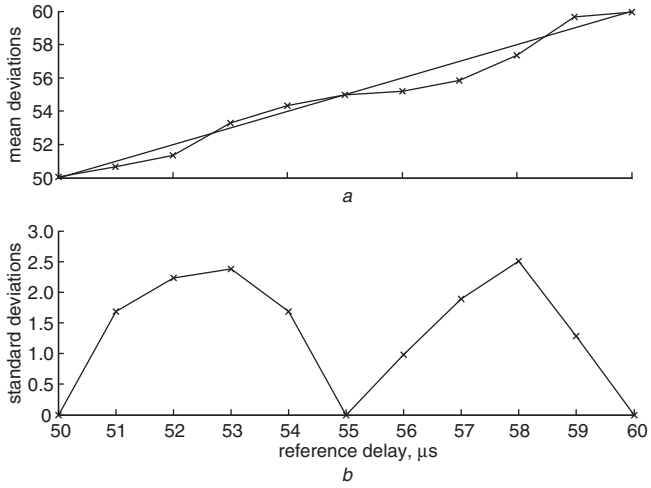

Fig. 2 *Mean and standard deviation for input signals with reference delay from 50 to 60 μs in steps of 1 μs*

a Mean deviations
– – – – reference delay
——— measured delay
× measured delay

b Standard deviations
——— standard deviation measurement delay
× standard deviation measurement delay

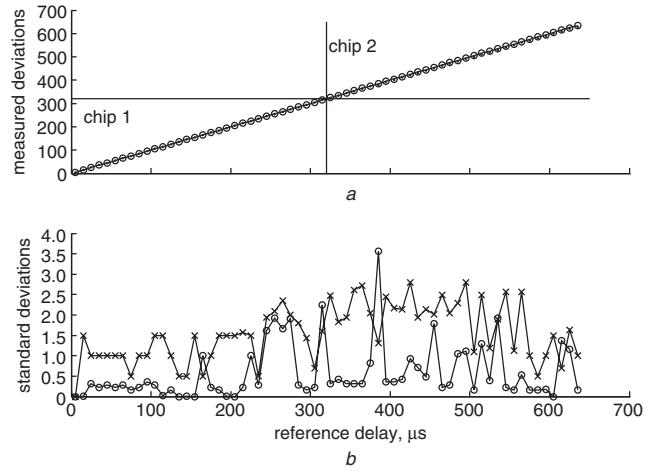

Fig. 3 *Measurement means, reference values and standard deviations, for both values of power supply (3.3 and 2 V)*

a Measured deviations
—— reference values
• V_{dd} = 2.0 V measurement mean delay
○ V_{dd} = 3.3 V measurement mean delay

b Standard deviations
× V_{dd} = 2.0 V standard deviation measurement delay
○ V_{dd} = 3.3 V standard deviation measurement delay

To evaluate the behaviour in the full range of values, two ICs were cascaded and the reference delay was varied between 5 and 640 μs in steps of 10 μs, for values of power supply of 3.3 and 2 V. For every value of reference delay, 100 values were acquired. Fig. 3 shows the measurement means, the reference values (with an indication to which one of the two ICs produced the output) and also the standard deviations, for both values of power supply (3.3 and 2 V). Note that the standard deviation never exceeds 3 μs. Fig. 1 shows a photograph of the chip.

Table 1: Comparison of reported systems

Unit	Power (μW)	Technology (μm)	Area	Accuracy
Neuromorphic sound localiser [5]	1850	0.50	5 × 5 mm	N/A
Micropower gradient flow [4]	32	0.50	3 × 3 mm	2 μs
Cross-correlator [3]	594	0.35	2 × 2.4 mm	5 μs
This work	12	0.50	1.5 × 3 mm	3 μs

Conclusions: Experimental results of a micropower IC for the measurement of the delay between two signals have been presented. The tests were conducted in the full range of measurement of two cascaded ICs, and the standard deviation never exceeded 3 μs. The unit was fabricated in a 0.5 μm technology and occupies 1.5 × 3 mm. It has a total power consumption of 45 μW at 3.3 V and 12 μW at 2 V, giving a power consumption per delay stage of 0.77 μW and 187.5 nW, respectively. As evidenced in Table 1, this improves on all low-power designs previously reported in the literature [3–5].

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P. Julián and F.N. Martin Pirchio (*Departamento de Ingeniería Eléctrica y Computadoras, Universidad Nacional del Sur, Av. Alem 1253, Bahía Blanca (8000), Argentina*)

E-mail: pjulian@ieee.org

A.G. Andreou (*Electrical and Computer Engineering Computer Science Whitaker Biomedical Engineering Institute and Center for Language and Speech Processing, Johns Hopkins University, 120 Stieff Building, 3400 N. Charles Street, Baltimore, MD 21218, USA*)

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