# High-Performance Control of a DC-DC Z-Source Converter used for an Excitation Field Driver

Santiago J. Amodeo, Héctor G. Chiacchiarini and Alejandro R. Oliva

***Abstract*—The electromechanical interface is a Synchronous Machine because its field winding permits direct management of the magnetization during speed variations. For systems with a common dc-link for the drive and excitation converters, the efficiency is increased if the excitation drive has boosting capability. It is shown that with the proposed control strategy the Z-source converter is suitable for this application, becoming a better alternative than the typically used *buck* converter. The Z-source converter in combination with the proposed multi-loop control law can achieve the desired voltage reference swing and high-performance tracking. An analytical comparison between the dominant losses of the *buck* topology, typically used in FESS, and the Z-source converter shows that the latter has higher efficiency for this application. The parameters of the converter prototype were experimentally identified and used to implement the proposed controller. The control strategy uses the two duty cycles as manipulated variables, one to allow tracking fast changes in the reference signal and the other to adapt the system to the slow changes. The combined action on both inputs contribute to the compensation of the non-minimum phase response of the Z-converter. Experimental results show the potential of the controller for tracking typical FESS application waveforms.**

***Index Terms*—DC-DC power conversion, Z-source converter, Flywheels, AC generator excitation, Synchronous machines.**

## I. Introduction

Due to the present trend of seeking improvements in the efficient use of the natural resources, an important research effort has been focused on temporary energy storage systems. On this track, the Flywheel Energy Storage System (FESS) has significant possibilities in power quality, frequency regulation of power systems and short-term storage applications [1]–[4]. The electromechanical interface of the FESS is an electrical machine whose rotor stores kinetic energy. A motor/generator operation of this electrical machine produces the charging/discharging of the FESS. Different kinds of electric machines are used for this application. The most common types are Permanent Magnet Synchronous Machines (PMSM), Induction Machines (IM) and Homopolar Synchronous Machines (HSM) [5]. The rotor of the HSM is more robust because it can be constructed out of a one-piece solid ferromagnetic material. The field winding disposition provides low rotor losses and enhances the mechanical reliability. In addition to its high efficiency, the HSM is a very suitable machine for FESS applications. Since the FW operates at high frequency and power, a pulse width modulation (PWM) strategy is not adequate, as it would need to operate the drive at extremely high switching frequency, thus producing high driver losses and also increasing critical rotor losses. Therefore, a pulse amplitude modulation technique (PAM) is more appropriate [6]; however, it restricts the amplitude of the armature space vector voltage to be constant. In normal operation, an instantaneous power flow has associated some rotor speed variation rate; therefore proper adjustment of the magnetic flux of the machine is required. In the case of the HSM, this could be done by adequately controlling the field winding current [5]. The use of a hybrid excitation scheme is also an attractive alternative for this high rotational speed application [7], where the permanent magnets are designed to provide the necessary base magnetization for the highest speed operation and the field winding produces the incremental magnetization during the charging and discharging operations. For all these excitation schemes, the operation of the field-winding converter conditions the global power control performance.

This paper is focused on the dc-dc stage of Fig. 1 which has to apply the field reference voltage ($v^{\star}_{fd}$) generated by a global FESS power controller [8]. The main objective of this controller is to achieve a high performance command of the active power of the FESS, as well as the regulation of a null reactive power. Typically, FESS are used in applications that require fast responses, therefore the generated references have highly demanding characteristics, which have to be synthesized by the HSM drivers. The voltage reference waveform

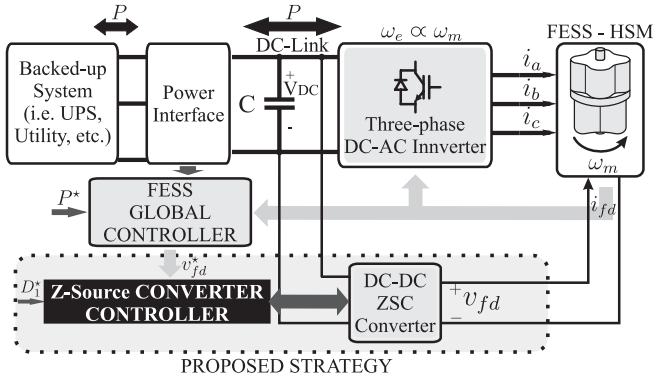


Fig. 1. FESS main scheme with the proposed ZSC excitation system.

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Santiago J. Amodeo (email:samodeo@uns.edu.ar), Héctor G. Chiacchiarini (email:hgch@uns.edu.ar), Alejandro R. Oliva (email: aoliva@uns.edu.ar).
The authors are with the Departamento de Ingeniería Eléctrica y de Computadoras of the Universidad Nacional del Sur, and with the Instituto de Investigaciones en Ingeniería Eléctrica "Alfredo Desages" of the Universidad Nacional del Sur and CONICET, Av. Alem 1253, (B8000CPB) Bahía Blanca, Argentina.

$v_{fd}^{\star}$ can be divided in two different frequency bands. One band (the low frequency components) is associated with the mentioned adjustment of the magnetization as the rotational speed and the stored energy change. The other band (high frequency components) is associated with the changes in the power-flow between the flywheel (FW) and the system. As the FESS active and reactive power controller is tuned to achieve faster responses, the generated reference has more challenging high frequency components. In most of the applications, FESS operate in a stand-by condition at full charge, which also corresponds to the highest rotational speed and the lowest field current. While the FESS is discharged, the excitation driver compensates this speed variation increasing the field current. Typically, a FESS has a rotational speed range of $1:2$ from low to full-stored energy, and an excitation driver based on the *buck* topology is used [5]. Therefore, the highest value of $v_{fd}$ that could be achieved is limited to the common dc-link voltage available ($V_{DC}$). At full charge, the FW is at its highest operational speed so the necessary applied $v_{fd}$ is minimum and, as the FW is discharged, $v_{fd}$ must be increased almost linearly following the speed variation. Consequently, the field winding has to be designed considering the worst case, where the minimum voltage is applied, including also a safety margin for the transients produced due to the power flow changes. A large flux excursion is required to achieve the desired performance in the active and reactive power control. The magneto-motive force (MMF) corresponding to this flux could be produced with different product combinations of the field current and the number of turns of the field winding. The power losses in the excitation driver are dominated mainly by the conduction losses. Therefore, as it will be analyzed in Section II, a reduction in the field current could produce an important decrease of the power losses of this stage. To design a field winding with the lowest possible current keeping the same MMF and the same average power, it is necessary to maximize the number of turns and also the field voltage. The common dc-link FESS driver scheme using a *buck* topology for the dc-dc excitation stage restrains the field winding voltage to the one available in the common dc-link. This results in field windings with lower number of turns and higher current than others designed without this voltage restriction. In this way, when the FW is discharged, the excitation system converter should necessarily provide the maximum possible voltage, and it would be desirable to have boosting capability as well as enough tracking performance to reproduce the high frequency reference components. Both requirements are challenging for *buck-boost* converters because of their typical non-minimum phase characteristics.

The Z-source converter (ZSC) topology (presented in [9]) is capable of producing an output voltage higher or lower than the input voltage. The ZSC has a characteristic impedance (Z) network between the input voltage source and the switching devices. The switching network can be configured with two active switches, one commands the conventional bucking effect and the other commands the boosting effect by the use of a shoot-through state that has to be applied within the zero state. The dynamic behavior of this converter was analyzed in [10] for the case where the shoot-through state totally overlaps the zero state. It was proved that, like other buck-boost converters, its output voltage also shows a non-minimum phase behavior. The shoot-through state introduces an extra control input which provides unique dynamic advantages among other buck-boost converters. In this article, both system inputs are used independently, but both accomplishing their duty cycle cross-restrictions, to compensate the non-minimum phase response, turning the ZSC into a fast buck-boost converter. Research on ZSC has focused mainly on dc/ac inverters and ac/ac converters although they can be designed also for dc output. The boosting capacity of Z-source inverters can be further enhanced using switched-inductance networks instead of normal inductances [11] or more complex networks such as a distributed impedance network, which was experimentally validated in [12]. Also three- and five-level Z-source converters with low count of components were analyzed in the literature [13]–[15] for different applications. The Z-network has also been applied at the input stage of nine-switch inverters used to control simultaneously two ac outputs in voltage and frequency [16] thus providing boosting capability and compensating the naturally lower ouptut voltage of the two outputs. Even for matrix converters the inclusion of a Z-network can provide advantages. In [17] an ac-ac matrix converter with an impedance network is proposed, which can buck and boost with step-changed frequency, and employs a safe-commutation strategy to conduct along a continuous current path, eliminating voltage spikes on the switches without the need for a snubber circuit. To overcome certain limitations of the classical Z-source ac-ac inverter, a derived topology called quasi-Z Source inverter (qZSI) was developed [18], which in general imposes a lower voltage stress on capacitors. The qZSI are further analyzed in [19] where switched inductors are included to provide continuous input current. Additional advantages of qZSI are a common ground with the dc source, reduced passive component count, lower *shoot-through* current, and lower current stress on inductors and diodes. In addition, it can suppress inrush current at startup, which might destroy the devices. In [20] the work is focused on ac-ac converters in quasi-Z topology, where the proposed converter operates in the continuous current mode. In [21] a discontinuous-current qZSI inverter is used as the basic topology to extend the boosting capability, and several other topological variations are examined, which show higher boost and lower voltage stress across the capacitors compared to those of traditional ZSI.

In previous works [22], [23], the use of the ZSC was proposed for FESS application, while a high-performance behavior (that does not show non-minimum phase response) was obtained based on a control strategy that used the two available control inputs to achieve the desired tracking behavior, reporting preliminary experimental results. The proposed controller utilized a dynamic linkage between the available inputs of the converter. The manipulated input of the converter $D_1$ (the duty cycle of the PWM) was used via a wide-band loop for an almost perfect output voltage tracking within the desired bandwidth. The other manipulated input, $D_{st}$ (the *shoot-through* duty cycle), was used for the regulation of this previous input $D_1$ to an established reference value ($D_1^{\star}$) using

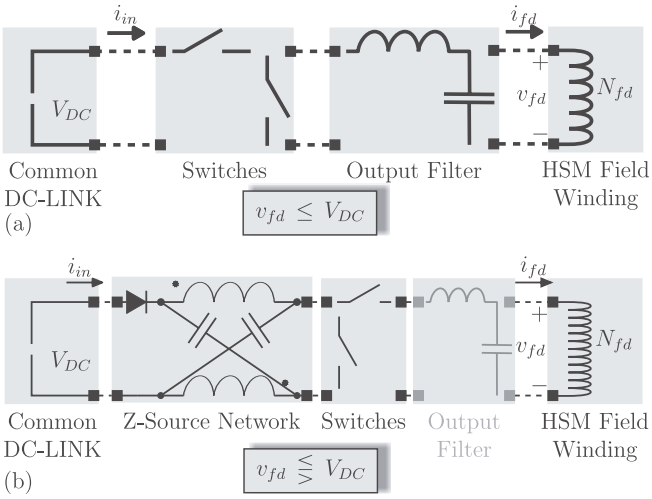


Fig. 2. Excitation Topologies a) *buck* based and b) ZSC based.

a slower cascade loop. Decoupling laws were used to cancel the interactions between those loops.

Figure 2 a) shows the *buck*-based excitation system and b) shows the proposed ZSC based counterpart. Although the ZSC is more complex and has more passive components, the switches handle lower currents; thus, the efficiency could be improved. Also, the output filter could be eliminated because the higher number of turns of the field winding results in an increased magnetization inductance, which could be used to smooth-out the output current. The ZSC achieves a high performance response due to the explicit utilization of the *shoot-through* state.

This paper presents the complete analysis with an analytical comparison between the losses of a traditional excitation system and the proposed one. Experimental validation of the converter averaged model and its parameters identification are also included, with closed-loop control experimental results. The control algorithm [23] was modified to overcome some implementation aspects. A snubber circuit was included in the prototype to improve the switching waveforms and to protect the semiconductor devices. The inclusion of this dissipative circuit deteriorated the efficiency of the converter, so its effect was incorporated into the model-based controller. Additionally, in order to reduce the computational burden for a DSP-based controller implementation, a simplification of the slower cascade loop of the original control algorithm was made.

The ultimate objective of this paper is to show that the Z-source converter is suitable for driving the excitation stage of a FESS system, providing a more advantageus alternative than the classical *buck* converter typically used for that case. The proposed topology leads to a more efficient scheme than the classical *buck* driver, showing a high-performance tracking response due to the proposed control strategy.

This work is organized as follows. Section II presents the field winding design equations and Section III includes the description of the topology and the non-linear state-space-averaged model of the converter. The comparison of the losses of the ZSC and the *buck* converter topologies is carried out in Section IV. Section V includes the control strategy, Section VI presents the experimental model identification, Section VII discusses some implementation aspects and describes the discrete implementation of the controller and Section VIII summarizes the experimental results. Finally, Section IX presents the conclusions.

## II. Field Winding Design Equations

The design equation of the field winding of the HSM based on the geometrical and material parameters and the available source voltage could be expressed as

$$I_{fd} = \frac{K_W\, A_W}{\rho_{cu}\, L_m} \phi_{fd}^2\, \Re_{fd} \frac{1}{V_{fd}}, \tag{1}$$

where $I_{fd}$ is the maximal field current which corresponds also with the maximal flux amplitude, $\phi_{fd}$. This flux amplitude occurs when the rotor is operating at the minimal rotational speed, hence at minimal stored energy. The geometric, electric and magnetic parameters of the core and winding window are: $K_W$, the winding window utilization factor; $A_W$, the winding window area; $l_m$, the mean length per turn; $\rho_{cu}$, is the cooper resistivity at nominal temperature; and $\Re_{fd}$ is the magnetic reluctance. All these parameters could be replaced with a global core parameter, $K_{nu}$, where its definition derives directly from

$$I_{fd} = \frac{K_{nu}}{K_X\, V_{DC}}. \tag{2}$$

Here, $K_X$, is the dc-dc converter input-output voltage relation ($V_{fd} = K_X\, V_{DC}$); where $X$ will be used to represent $B$ (for *buck* topology) or $Z$ (for *ZSC* topology), respectively. Therefore, for the *buck* converter $K_B < 1$ while for the ZSC the voltage relation is $K_Z \gtrless 1$. Therefore, as $K_Z$ could be higher than $K_B$, to produce the same flux amplitude, the field current corresponding to the ZSC is lower than the one that results using a *buck* converter. The number of turns of the field winding also depends on the available source voltage and it could be determined from

$$N_{fd} = \frac{K_X\, V_{DC}}{K_d\, \phi_{fd}}, \tag{3}$$

where $K_d = \rho_{cu}\, L_m / K_W\, A_W$. The maximum average power dissipated in the field winding is

$$P_{fd} = I_{fd}\, V_{fd} = K_d\, \phi_{max}^2\, \Re_{fd}. \tag{4}$$

This expression clearly shows that $P_{fd}$ is independent of the source voltage; therefore results equal in both converter topologies. However, in the case of the ZSC topology, as the nominal field current is lower than the one associated with the *buck* converter, its efficiency could be improved. A first order comparison of the main losses of both topologies is discussed in Section IV.

## III. Z-Source Converter

The ZSC introduces a particular LC network between the dc-link and the switches of a standard voltage source inverter (VSI). This passive network allows the converter to make use of the *shoot-through* mode to boost the output voltage [9]. The reliability of the inverter is improved because this

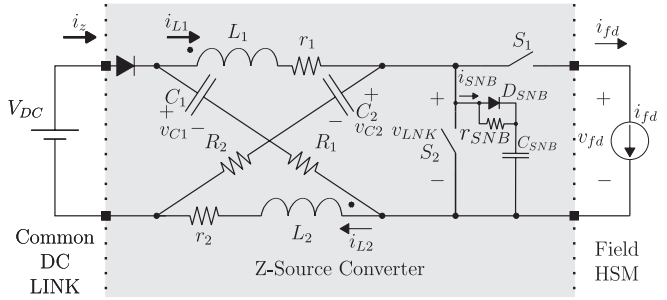


Fig. 3. Dc-dc Z-source Converter Topology.

mode does not compromise the circuit integrity. The converter is loaded with the HSM field winding, which is a highly-inductive load and could be considered as a current source for the ZSC dynamics. In this application only the first-quadrant operation of the converter is used. The implemented converter topology is shown in Fig. 3. The ZSC was designed to ensure the continuous conduction operation (CCO) [24], [25] for the entire application range. As was mentioned previously, a RCD snubber circuit was used to solve experimental aspects, and this auxiliary circuit will be incorporated in the model at the end of this Section.

### A. CCO of the ZSC

The ZSC presents three modes of operation in CCO [25]. Fig. 4 shows the equivalent circuits for each CCO mode. The active mode (MODE 1) corresponds to a), the null mode (MODE 0) to b) and the *shoot-through* mode (MODE ST) to c). Usually, only two modes are considered for CCO [26] because the *shoot-through* mode is applied during the entire null mode. In this work, the portion of the null mode where the *shoot-through* mode is applied is also used as an input variable. The state-space vector of the converter is $\mathbf{x} = \left[\begin{array}{cccc} i_{L1} & i_{L2} & v_{C1} & v_{C2} \end{array}\right]^T$ and $\mathbf{u} = \left[\begin{array}{cc} V_{DC} & I_{fd} \end{array}\right]^T$ is the external perturbations input vector, where each of these variables are indicated in Fig. 4. Then, the state-space dynamic model is obtained as

$$\dot{\mathbf{x}}_\mathbf{i} = \mathbf{A}_\mathbf{i}\mathbf{x}_\mathbf{i} + \mathbf{B}_\mathbf{i}\mathbf{u}, \tag{5}$$

and the output voltage is

$$v_{fd\,\mathbf{i}} = \mathbf{C}_\mathbf{i}\mathbf{x} + \mathbf{D}_\mathbf{i}\mathbf{u}, \tag{6}$$

where the subscript $\mathbf{i}$ will be used to denote each of the three operating modes (i.e., 1, ST and 0) . The fractions of $T_s$ that the converter is operating in each mode are the manipulated inputs to the system. Because the sum of these intervals must be equal to $T_s$, the forced state of the switches results in two independent controlled intervals. Here, the standard duty cycle $D_1 = T_1/T_s$ and the *shoot-through* duty cycle $D_{st} = T_{st}/T_s$ are used. The following inductances and capacitances matrix will be used to obtain the system and input matrix corresponding to each mode

$$\mathbf{P} = \left[\begin{array}{cccc} L_1 & M & 0 & 0 \\ M & L_2 & 0 & 0 \\ 0 & 0 & C_1 & 0 \\ 0 & 0 & 0 & C_2 \end{array}\right]. \tag{7}$$

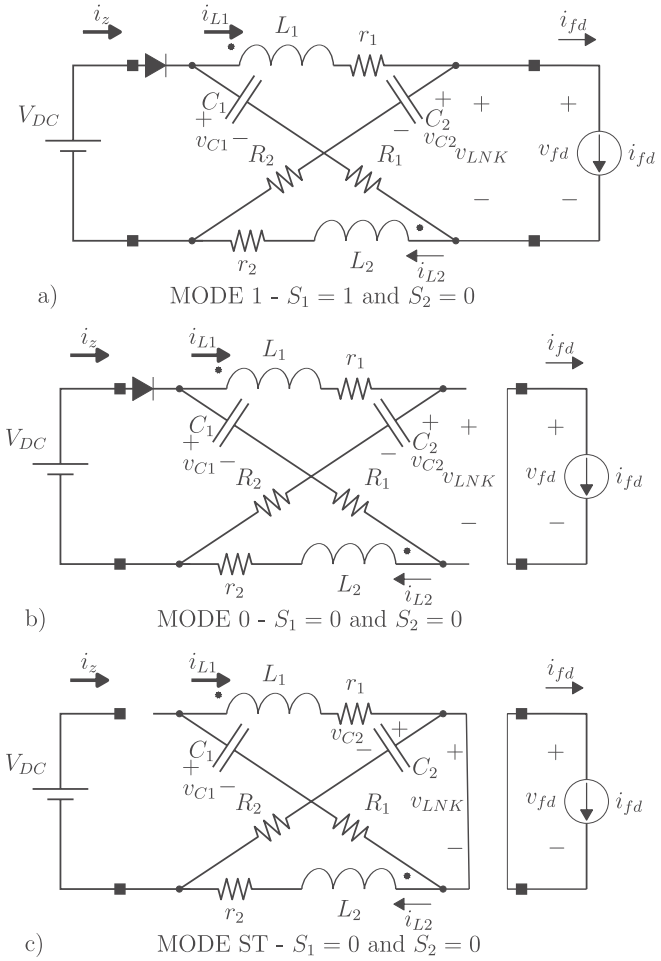


Fig. 4. Dc-dc Z-source modes of operation: a) MODE 1; b) MODE 0; c) MODE ST.

*1) MODE 1:* The Z-network design ensures that $i_{L1} + i_{L2} > I_{fd}$; then, the input current $i_z = i_{L1} + i_{L2} - I_{fd} > 0$ and the input diode is forward biased. During MODE 1 the currents of both inductors decrease almost linearly. Its duration is $D_1\,T_S$ and its equivalent circuit is shown in Fig. 4 a). The corresponding model matrices for this mode are

$$\mathbf{A}_1 = \mathbf{P}^{-1}\left[\begin{array}{cccc} -(R_2 + r_1) & 0 & 0 & -1 \\ 0 & -(R_1 + r_2) & -1 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{array}\right], \tag{8}$$

$$\mathbf{B}_1 = \mathbf{P}^{-1}\left[\begin{array}{cc} 1 & R_2 \\ 1 & R_1 \\ 0 & -1 \\ 0 & -1 \end{array}\right], \tag{9}$$

$$\mathbf{C}_1 = \left[\begin{array}{cccc} R_2 & R_1 & 1 & 1 \end{array}\right], \tag{10}$$

and

$$\mathbf{D}_1 = \left[\begin{array}{cc} -V & -(R_1 + R_2) \end{array}\right]. \tag{11}$$

*2) MODE ST:* When switch $S_2$ is turned on the converter starts the *shoot-through* mode. The equivalent circuit for this mode is shown in Fig. 4 b). Its duration is $D_{st}\,T_s$ and during

this period the input diode is reverse biased; therefore, the capacitors charge the inductors. The model matrices for this mode are

$$\mathbf{A}_{st} = P^{-1} \begin{bmatrix} -(R_1+r_1) & 0 & 1 & 0 \\ 0 & -(R_2+r_2) & 0 & 1 \\ -1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix}, \quad (12)$$

$$\mathbf{B}_{st} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}, \quad (13)$$

$$\mathbf{C}_{st} = \begin{bmatrix} 0 & 0 & 0 & 0 \end{bmatrix}, \quad (14)$$

and

$$\mathbf{D}_{st} = \begin{bmatrix} 0 & 0 \end{bmatrix}. \quad (15)$$

*3) MODE 0:* Mode 0 is applied for the remaining of the period until $T_s$ is completed. The equivalent circuit during mode 0 is shown in Fig. 4 c). The following system matrices correspond to this mode

$$\mathbf{A}_0 = \mathbf{A}_1, \quad (16)$$

$$\mathbf{B}_0 = \mathbf{P}^{-1} \begin{bmatrix} 1 & 0 \\ 1 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}, \quad (17)$$

$$\mathbf{C}_0 = \mathbf{C}_{st}, \quad (18)$$

$$\mathbf{D}_0 = \mathbf{D}_{st}. \quad (19)$$

### B. Z-SOURCE STATE-SPACE-AVERAGED MODEL

Evaluating (5) to obtain the state-space model for each mode and using their corresponding duty cycles, the state-space-averaged model can be calculated as

$$\mathbf{x} = \mathbf{x}_1 D_1 + \mathbf{x}_0 (1 - D_1 - D_{st}) + \mathbf{x}_{st} D_{st}, \quad (20)$$

and the average output voltage as

$$v_{fd} = v_{fd\,1} D_1 + v_{fd\,0} (1 - D_1 - D_{st}) + v_{fd\,st} D_{st}. \quad (21)$$

Taking into account the symmetries of the circuit, the system equations are reduced to the following second order system

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_C \end{bmatrix} = \begin{bmatrix} -X(r+R) & -X(1-2D_{st}) \\ C^{-1}(1-2D_{st}) & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} X(1-D_{st}) & X\,D_1 R \\ 0 & -C^{-1} D_1 \end{bmatrix} \begin{bmatrix} V_{DC} \\ I_{fd} \end{bmatrix}, \quad (22)$$

whose parameters are indicated in Fig. 3, $X = (L+M)^{-1}$ and inputs $D_1$ and $D_{st}$, as was previously mentioned, are the standard duty cycle and the *shoot-through* duty cycle, respectively. The output voltage (21) can be obtained for the reduced-order system as

$$v_{fd} = D_1\, v_1 \quad (23)$$

where $v_1$ is defined as an equivalent boosted dc-link and is given by

$$v_1 := 2R\, i_L + 2\, v_C - V_{DC} - 2R\, I_{fd}. \quad (24)$$

Because the *shoot-through* must be produced within mode 0: $S_1$=open and $S_2$=open (see [3,7]), the duty cycle $D_{st}$ is restricted to

$$0 < D_{st} < 1 - D_1. \quad (25)$$

If the parasitic resistors are neglected, the steady-state output voltage results

$$v_{fd}^{ss} = \frac{D_1}{1 - 2D_{st}} V_{DC}, \quad (26)$$

where it is evident that the $D_{st}$ input could be used to boost the dc-link voltage and produce the desired output voltage in combination with the appropriated $D_1$ input. Of course, this is possible as long as the restriction for $D_{st}$ (25) and the standard restriction for $D_1$ ($0 \leq D_1 \leq 1$) are satisfied.

As the controller is highly dependent of the converter model and the snubber circuit was neglected in the averaged-states model, the controller performance could be highly compromised. Then, the average effect of this circuit is incorporated with an equivalent resistance which consumes the same average power. This resistance is calculated considering that the energy stored in the snubber capacitor is dissipated within each commutation cycle. Hence, it is obtained using

$$R_{SNB} = \frac{2}{f_s\, C_{SNB}} \quad (27)$$

and the snubber current, using directly the voltage $v_1$ as

$$i_{SNB} = \frac{v_1}{R_{SNB}}. \quad (28)$$

Note that this resistance is not equal to the real $r_{SNB}$ of the snubber circuit. Therefore the average effect of this snubber circuit could be simply introduced in the model, considering that the previously introduced output current of the converter without snubber ($I_{fd}$) is the addition of the real output current and this average snubber circuit current.

## IV. LOSSES OF THE *buck* CONVERTER AND THE ZSC

At the power and switching frequency operation range for the considered FESS application the converter losses are mainly determined by the conductive losses. This Section includes a first order analytical comparison between the conductive losses produced by both topologies. The input-output voltage relation of the ZSC is obtained from (26) as

$$K_Z = \frac{D_{1Z}}{1 - 2\,D_{st}}. \quad (29)$$

In the case of the *buck* converter this voltage relation is directly $K_B = D_{1B}$. A subscript $Z$ or $B$ was added to identify the standard duty cycle of each topology.

### A. Conduction Losses of the Switches

The conduction losses of the switches are obtained by the averaged current circulating on each switch of the topology using the guidelines presented in [27]. The conduction losses of the switches of the ZSC could be determined considering the contribution of each device as

$$P_{onZ} = P_{onS1} + P_{onS2} + P_{onS3}. \quad (30)$$

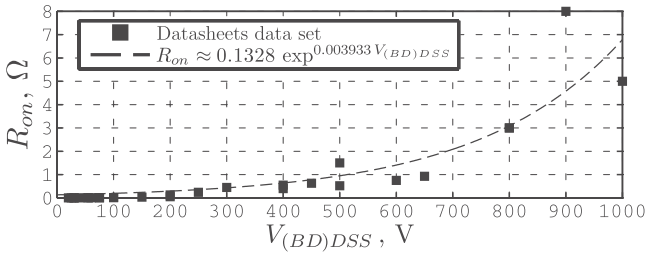


Fig. 5. MOSFETs $R_{on}$ vs. $V_{(BD)DSS}$ fitting data results.

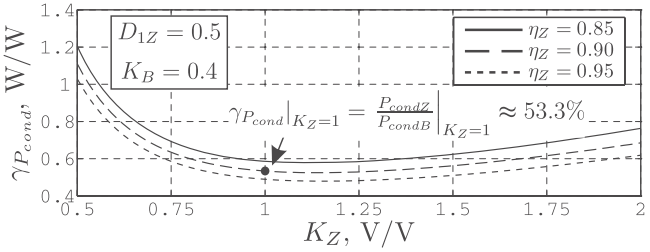


Fig. 6. Comparison of switches conduction losses between topologies.

The topology shown in Fig. 3 includes only two switches, but to simplify the losses analysis the diode $D_1$ was replaced by an equivalent switch. By this way, and also considering a ZSC converter efficiency, $\eta_Z$, and the resistance of the switches, $R_{onZ}$, the conduction losses of the switches of the ZSC as a function of $K_Z$ are

$$P_{onZ} = R_{onZ}\left(\frac{K_{nu}}{K_Z\,V_{DC}}\right)^2 . \cdot\left(D_{1Z} + \frac{2\,K_Z\,(K_Z - D_{1Z})}{\eta_Z^2} + \frac{(K_Z + D_{1Z})}{2\,K_Z\,\eta_Z^2}\right). \quad (31)$$

The conduction losses of the switches of the *buck* topology are

$$P_{onB} = R_{onB}\,I_{fdB}^2 = R_{onB}\left(\frac{K_{nu}}{K_B\,V_{DC}}\right)^2 . \quad (32)$$

Therefore, the relation of the conduction losses of the switches of both topologies is,

$$\gamma_{P_{on}} = \frac{P_{onZ}}{P_{onB}} = \frac{R_{onZ}}{R_{onB}}\left(\frac{K_B}{K_Z}\right)^2 . \left(D_{1Z} + \frac{2\,K_Z\,(K_Z - D_{1Z})}{\eta_Z^2} + \frac{(K_Z + D_{1Z})}{2\,K_Z\,\eta_Z^2}\right). \quad (33)$$

Due to the boosting capabilities of the ZSC, the "on" resistance of both topologies should be specified taking into account the different Drain to Source Breakdown Voltage $V_{(BD)DSS}$. Based on a set of data obtained from the datasheets of commercial MOSFETs, the relation between $R_{on}$ and $V_{(BD)DSS}$ was approximated with the following expression

$$R_{on} = 0.1328\ \exp^{0.003933\,V_{(BD)DSS}} . \quad (34)$$

These fitting results are presented in Fig. 5. Using this last equation in (33) with the $V_{(BD)DSS}$ corresponding for each topology yields,

$$\gamma_{P_{on}} = e^{0.0047196\,V_{DC}\left(\frac{K_Z}{D_{1Z}} - 1\right)}\left(\frac{K_B}{K_Z}\right)^2 . \cdot\left(D_{1Z} + \frac{2\,K_Z\,(K_Z - D_{1Z})}{\eta_Z^2} + \frac{(K_Z + D_{1Z})}{2\,K_Z\,\eta_Z^2}\right) \quad (35)$$

This expression is evaluated considering that the FW system is on standby condition, hence the field current is at its lower value. Therefore in average, $K_B = 0.4$ for the *buck* converter and $D_{1Z} = 0.5$, as will be explained in Section VIII. Fig. 6 depicts this law as a function of the ZSC voltage relation $K_Z$: at $K_Z = 1$ the conduction losses of the ZSC represents the $53.3\%$ of the *buck* converter conduction losses that would produce the same MMF.

### B. Conduction Losses of the Inductors

At first glance, the ZSC topology uses two inductors in the passive network but, because the flux in both inductors has the same behavior, instead it is possible to use only one split inductor. For the model comparison it is considered that both topologies utilize inductors constructed with the same core material and dimensions and the same winding window geometry. Also it is considered that both topologies have equal relations between the ripple amplitude of inductor current and its mean value, i.e. $r\,I_{fdB} = r\,\frac{I_{fdZ}}{\eta_Z}$ with $r$ the relation factor. Therefore, the relative inductor ripple current of the ZSC could be obtained from

$$r\Delta i_{l,z} = \frac{\Delta i_{l,z}}{I_{L,Z}} = \frac{(K_Z^2 - D_{1Z}^2)\,T_s}{4\,D_{1Z}\,K_Z\,L_Z}\,\frac{V_{DC}^2\,\eta_Z}{K_{nu}} \quad (36)$$

and for the *buck* converter from

$$r\Delta i_{l,b} = \frac{\left(K_B - K_B^2\right)\,K_B\,V_{DC}^2\,T_S}{L_B\,K_{nu}} . \quad (37)$$

The conduction power losses in the inductors is approximated as

$$P_{LX} = \underbrace{R_{LX}\,I_{LX}^2}_{DC} + \underbrace{r_{LX}\,i_{LX}^2}_{AC} = R_{LX}\,\left(I_{LX}^2 + F_R\,i_{lX}^2\right), \quad (38)$$

where $F_R$ is the resistance frequency variation factor. Consequently the inductor conduction losses ratio between both topologies is

$$\gamma_{P_L} = \frac{P_{LZ}}{P_{LB}}\left(\frac{I_{fdZ}}{I_{fdB}}\right)^2\frac{R_{LZ}}{R_{LB}} = \left(\frac{K_B}{\eta_Z\,K_Z}\right)^2\frac{R_{LZ}}{R_{LB}} . \quad (39)$$

Using (36) and (37) the relations between the inductance could be obtained as

$$\gamma_L = \frac{L_Z}{L_B} = \frac{(D_{1Z} + K_Z)\,(K_Z - D_{1Z})\,\eta_Z}{4\,D_{1Z}\,(1 - K_B)\,K_B^2} . \quad (40)$$

As was mentioned, as a comparative criteria, both topologies used the same core and winding dimensions hence $\frac{R_{LZ}}{R_{LB}} = \frac{L_{LZ}}{L_{LB}}$. Combining (39) and (40) the conduction inductor losses ratio yields,

$$\gamma_{P_L} = \frac{(K_Z^2 - D_{1Z}^2)}{4\,D_{1Z}\,K_Z\,\eta_Z\,(1 - K_B)} . \quad (41)$$

This expression is plotted for the same parameters that were previously used in the comparison of the conduction losses of the switches and the results are shown in Fig. 7. A possible reduction of the conduction losses of the inductor of nearly $69,5\%$ could be obtained. These results support the proposal of using ZSC for the excitation drive in FESS.

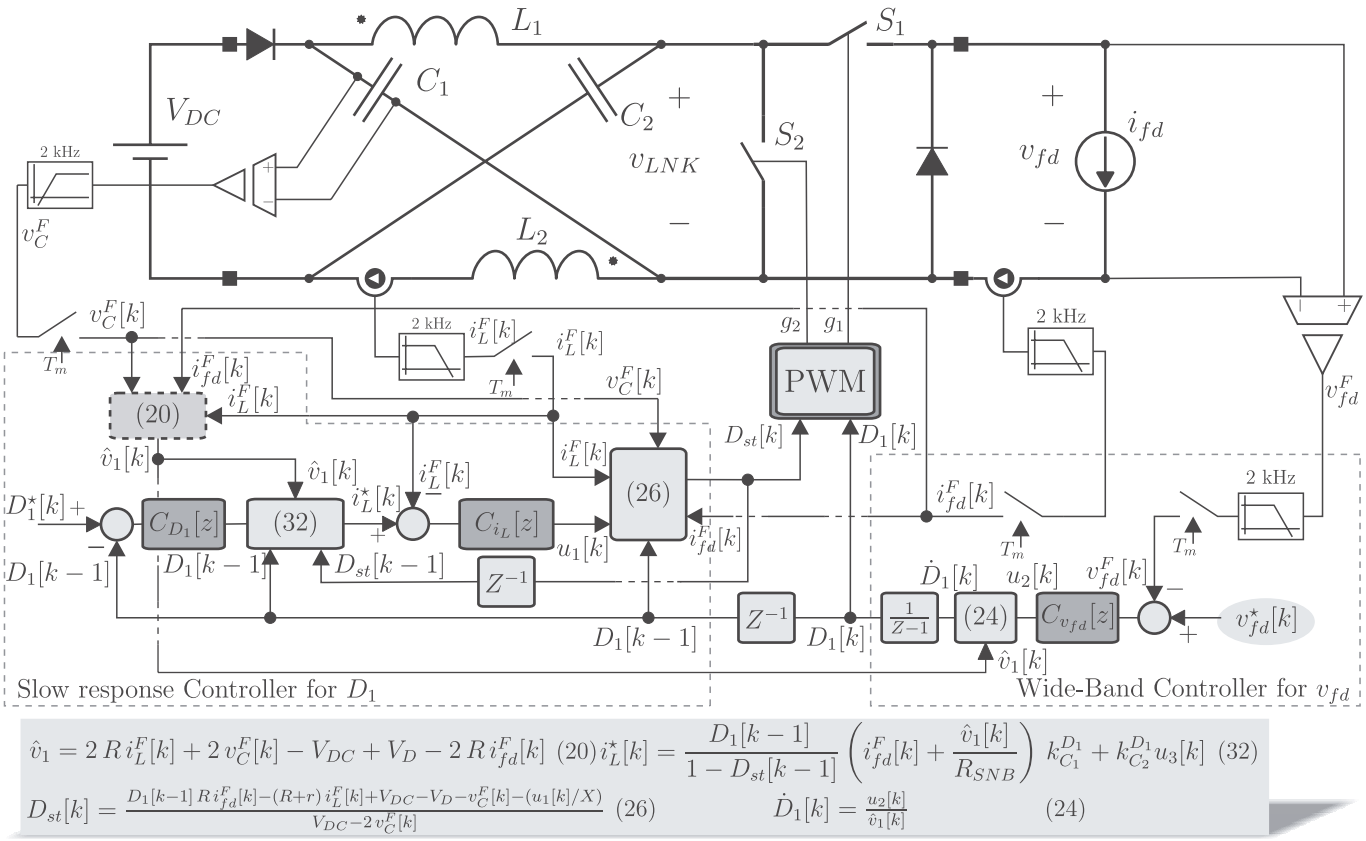


Fig. 8. Dc-dc Z-source Converter Control Scheme.

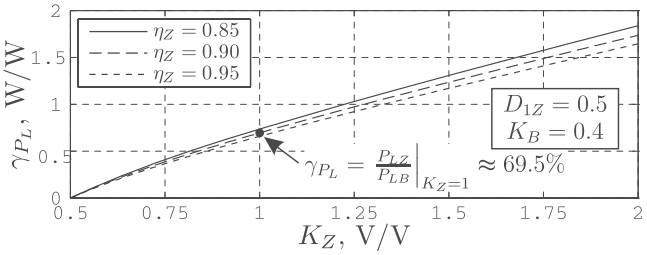


Fig. 7. Comparison of inductors conduction losses between topologies.

## V. Control Strategy

The control strategy shown in Fig. 8 is composed of two loops. The first loop is a wide-band control scheme of the output voltage $v_{fd}$ using $D_1$ as the manipulated variable. The other one is much slower and stabilizes $D_1$ to the desired stationary reference, while allowing it to react to the high frequency demands of the first loop controller. This is achieved by adjusting the voltage $v_1$ by means of a cascade control through $i_L$ using the $D_{st}$ input. This last control loop utilizes a nonlinear feedback linearization law to decouple it from the first loop.

### A. Controller for $v_{fd}$

Differentiating (23) it is obtained

$$\dot{v}_{fd} = \dot{D}_1\, v_1 + \cancel{D_1\, \dot{v}_1}. \tag{42}$$

The second term of the right hand side can be neglected since $v_1$ will be slow-varying so that a new variable can be defined as

$$u_2 = \dot{D}_1 v_1. \tag{43}$$

If the output voltage is controlled with a linear controller $C_{v_{fd}}$ through input $u_2$ and then $D_1$ could be obtained as

$$D_1 = \int \frac{u_2}{v_1} dt. \tag{44}$$

This loop is tuned to obtain the desired output voltage bandwidth.

### B. Controller for $D_1$

The objective of this second loop is the regulation of $D_1$ to a desired reference value $D_1^\star$ as its value is modified by the previous loop. This is achieved by a cascade controller that indirectly adapts $v_1$ to the slower tendencies of the reference.

*1) Inner loop - Controller for $i_L$:* Using the following input transformation in (22)

$$\begin{aligned} D_{st} \;=\; & (-u_1 - X\,(r+R)\,i_L - X\,v_C \\ & + X\,V_{DC} + R\,X\,D_1 I_{fd})\,/\,(X\,(V - 2\,v_C)) \end{aligned} \tag{45}$$

it results in $\dot{i}_L = u_1$. Then, the inductor current can be controlled to its reference value $i_L^\star$ with a linear controller $C_{i_L}$ using this auxiliary input $u_1$.

*2) Outer loop - Controller for $D_1$:* This outer loop controller generates the reference $i_L^*$ to the previous inner controller. Because this is the slowest tuned loop, it is considered that $v_{fd}$ has been stabilized to its reference value $v_{fd}^\star$. Then, differentiating (23) yields

$$\dot{D}_1 = \frac{\dot{v}_{fd}^\star\, v_1 - v_{fd}^\star\, \dot{v}_1}{v_1^2} \approx -\frac{v_{fd}^\star}{v_1^2}\dot{v}_1 = -\frac{D_1}{v_1}\dot{v}_1\,. \qquad (46)$$

This last derivative could be approximated by the main terms of the equation obtained from differentiating (24), resulting in $\dot{v}_1 = 2\,\dot{v}_C$. Replacing $\dot{v}_C$ from the system (22) it results in

$$\dot{v}_1 = 2\,\dot{v}_C = 2\left(\frac{1-2\,D_{st}}{C} i_L - \frac{D_1}{C}\,I_{fd}\right). \qquad (47)$$

If the inner-loop reference, $i_L^\star$, is given by this law

$$i_L^\star = \frac{D_1}{(1-2\,D_{st})} I_{fd} - \frac{C\,v_1}{2\,(1-2\,D_{st})\,D_1}\,u_3, \qquad (48)$$

the result obtained is $\dot{D}_1 \approx u_3$. This can be verified by replacing (48) in (47), and the resulting equation in (46). Then, a slower-tuned linear controller $C_{D_1}$ is implemented to regulate $D_1$ to its desired value $D_1^\star$ using the auxiliary input $u_3$.

## VI. ZSC Model Identification

The controller laws developed in the previous Section are based on the averaged model of the ZSC. Therefore, an experimental validation of the ZSC model and its parameters identification is crucial for the implementation of the controller algorithms. Based on the dynamic averaged model developed in Section III, the steady-state laws of the states and measured outputs are obtained. The laws corresponding to the averaged system states are

$$I_L = \frac{D_1\,(R_{fd} + D_1\,R_{SNB})\,V_{DC}}{Den}, \qquad (49)$$

and

$$V_C = \frac{\left(D_1^2\,(r - 2\,R + 4\,D_{st}\,R)\,R_{SNB}\right)V_{DC} + \left(1 - 3\,D_{st} + 2\,D_{st}^2\right)\,R_{fd}\,(R + R_{SNB})\,V_{DC} + D_1\,(r\,R_{fd} - (1-2\,D_{st})\,R\,(2\,R_{fd} - (1-D_{st})\,R_{SNB}))}{Den}\,\frac{V_{DC}}{}. \qquad (50)$$

where,

$$\begin{aligned} Den = {} & 2\,D_1\,(r + (4\,D_{st} - 1)\,R)\,R_{fd} + \\ & D_1\,(1-2\,D_{st})^2\,R\,R_{SNB} + \\ & +2\,D_1^2\,(r + (4\,D_{st} - 1)\,R)\,R_{SNB} + \\ & +(1-2\,D_{st})^2\,R_{fd}\,(R + R_{SNB})\,. \end{aligned}$$

The output expressions are

$$V_{fd} = \frac{D_1\,(1-2\,D_{st})\,R_{fd}\,R_{SNB}\,V_{DC}}{Den}, \qquad (51)$$

and

$$I_{fd} = \frac{V_{fd}}{R_{fd}}. \qquad (52)$$

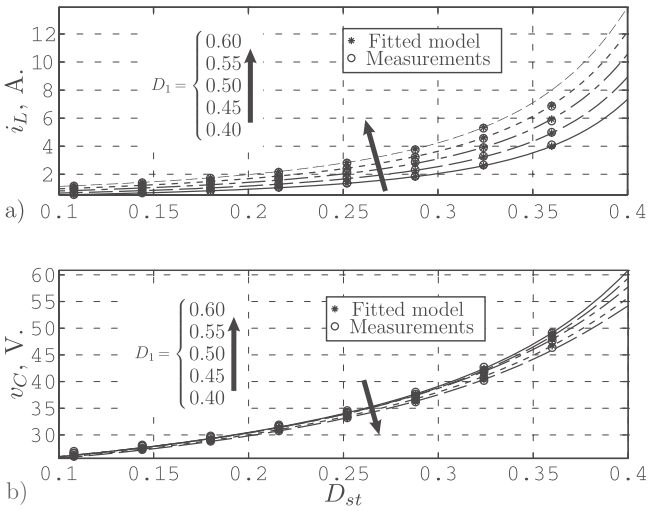


Fig. 9. Static parameter identification of system states a) Current $i_L$; b) Voltage $v_C$.

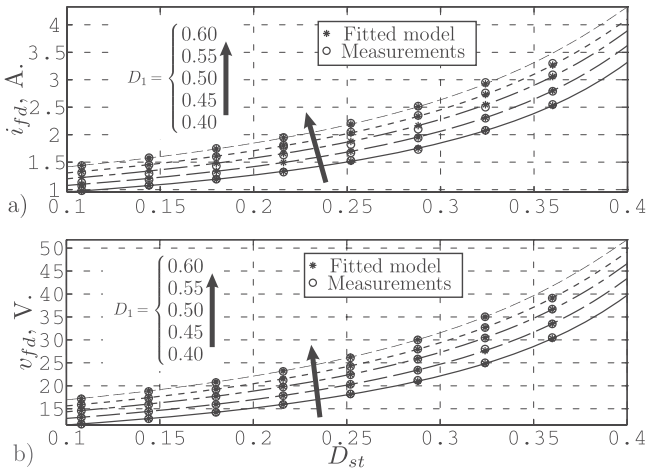


Fig. 10. Static parameter identification of system outputs a) Current $i_{fd}$; b) Voltage $v_{fd}$.

The states and outputs were measured and a set of experimental data was obtained by sweeping the inputs within the operating range of the converter. Using a static nonlinear parameter identification algorithm the static parameters of the converter were obtained. Fig. 9 and 10 show the results. The dynamical parameters of the converter where obtained using a dynamical parameter identification algorithm from a set of input step system responses. In Fig. 11 the obtained adjustment of a step transient response is presented. The parameters obtained from the fitting process are presented in Table I. The close agreement of these laws, evaluated with the identified parameters, and the experimental data brings an important validation of the model used to develope the control laws of Section V.

## VII. Implementation Aspects

A dc-dc Z-source converter prototype has been designed and built. The purpose of this first prototype was mainly the validation and the analysis of the control strategy, and the converter efficiency was not the main design priority. The

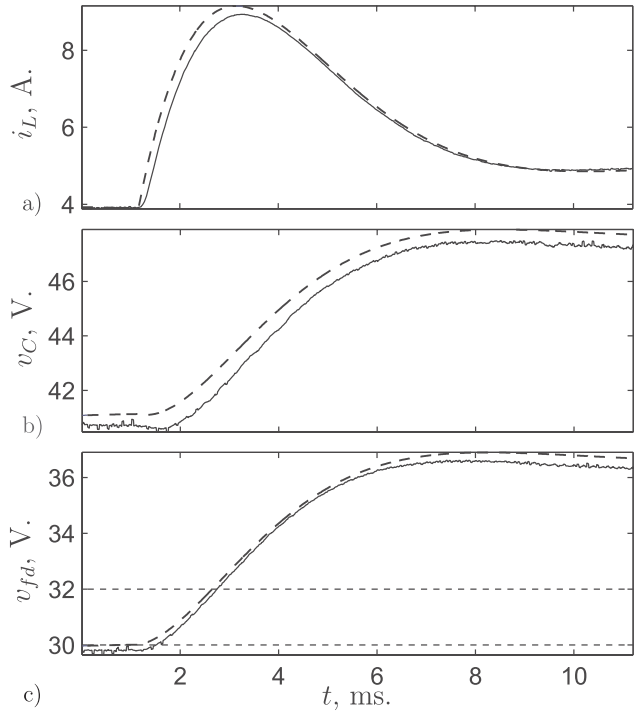


Fig. 11. Dynamical parameter identification from system step response a) Current $i_L$; b) Voltage $v_C$; c) Voltage $v_{fd}$.

| Parameter | Value | Unit |
|---|---|---|
| $X$ | 2956.6 | $H^{-1}$ |
| $C$ | 656 | $\mu F$ |
| $r$ | 171.5 | $m\Omega$ |
| $R$ | 299.9 | $m\Omega$ |
| $R_{SNB}$ | 279.18 | $\Omega$ |
| $V_{DC}$ | 23.7 | $V$ |
| $f_s$ | 20 | $kHz$ |
| $T_m$ | 50 | $\mu s$ |

TABLE I
IDENTIFIED PARAMETERS OF THE CONVERTER MODEL.

proposed control algorithm, which is shown in Fig. 5, was embedded in a DSP (TI-TMS320F28335). The average value of the converter variables $x^F$, with $x$ being the states or outputs variables, were measured through analog fifth-order Low Pass Filters (LPFs). Also, components protection and auxiliary circuits were developed. The control algorithm was discretized with a sample time equal to the commutation period. The transformation laws (43), (45) and (48) were evaluated using the sampled values of the filtered variables $x^F$. For the evaluation of the manipulated variables $D_1$ and $Dst$, their previous sampled time values were used in that equations. The snubber circuit effect was incorporated following the procedure presented in Section III. The discrete implementation of (48) was performed by linearizing the second term with respect to $u_3$ and the $k_{C_1}^{D_1}$ gain was added to the first term, to fine tune the controller loop, as it is shown as follows

$$i_L^\star[k] = \frac{D_1[k-1]}{1-D_{st}[k-1]}\left(i_{fd}^F[k] + \frac{\hat{v}_1[k]}{R_{SNB}}\right)k_{C_1}^{D_1} + k_{C_2}^{D_1}u_3[k]. \quad (53)$$

The factor $k_{C_2}^{D_1}$ corresponds to the highest expected value given by the above mentioned linearization. Both modifications allow the outer controller to have a simpler implementation when it is tuned with the slowest response. The linear controllers $C_{v_{fd}}$ and $C_{i_L}$ are a combination of a PI controller with additional LEAD compensators, to improve the low phase-margin due to the contribution of the LPFs at the desired bandwidth frequency. The $C_{D_1}$ controller is a PI controller. Since $v_1$ is not a direct measurable variable (it is not exactly equal to the average of the $v_{LNK}$ in Fig. 4), it is calculated from (24) using the known variables and parameters. This open-loop estimation $\hat{v}_1$ is used in (53) and (44). The converter was loaded with an inductor with similar characteristics to that of the HSM.

## VIII. EXPERIMENTAL RESULTS

To make an experimental validation of the proposed control strategy, the developed prototype was tested by tracking references which have similar waveforms to those of the final application. This reference is composed of two triangular waveforms added together. One is slowly varying (period of 40 s and 10-V of peak-to-peak amplitude) and is associated with the low frequency components due to the rotational speed variations of the machine during typical charge/discharge cycles. The other is a triangular waveform with a period of 20 ms and a peak-to-peak amplitude of 5 V, which accounts for the high-frequency variations due to the active power transitions of the FESS tuned to respond within the fundamental period in a 50-Hz utility system. Therefore, the controller was tuned for a generic application specification. The objective of these tests is to demonstrate the proposed controller performance, mainly how the controller used both available inputs of the converter to achieve the tracking task. Table I summarizes all used converter parameters including the sample time and the switching frequency. The measured $v_{fd}^F$ and $D_1$ variables are shown in Fig. 12. It can be seen how the controller synthesized the $v_{fd}$ reference keeping $D_1$ equal to its desired reference value ($D_1^\star = 0.5$). For the same reference the measured $i_L^F$, controlled by the inner loop, and the input $D_{st}$ are shown in Fig. 13. Note that, due to the sensing interface of the dynamics states and the outputs, except for the inputs variables, all the positive y-axis directions are pointed downwards. The second experiment was performed with a reference $v_{fd}^\star$ which is a combination of the reference used in the previous experiment added to a higher-frequency triangular waveform of lower amplitude, which can be associated with the fast power-flow changes of the FW. The resulting waveform was a more challenging task for the controller. For this case the measured $v_{fd}^F$ and $D_1$ variables are shown if Fig. 14, where two magnified views for the lowest and highest $v_{fd}$ levels are included. Notice how the controller uses $D_1$ to track the high-frequency components, but keeping its mean value at $D_1^\star$. The behavior of the variables $i_L^F$ and $D_{st}$ for this last experiment are shown in Fig. 15.

## IX. CONCLUSIONS

The boosting capability of the Z-source converter allows designing the field winding of the HSM with a nominal voltage

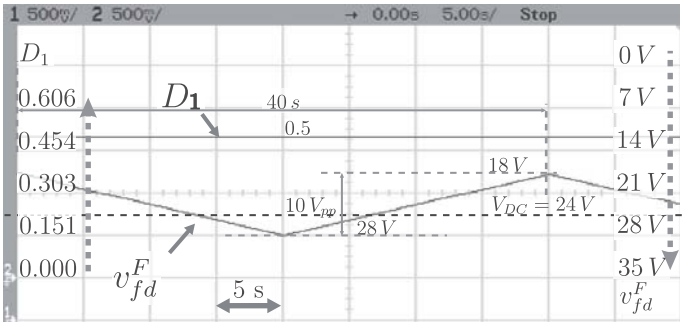


Fig. 12. Signals $v_{fd}$ and $D_1$ for the experiment of tracking the slowly varying reference.

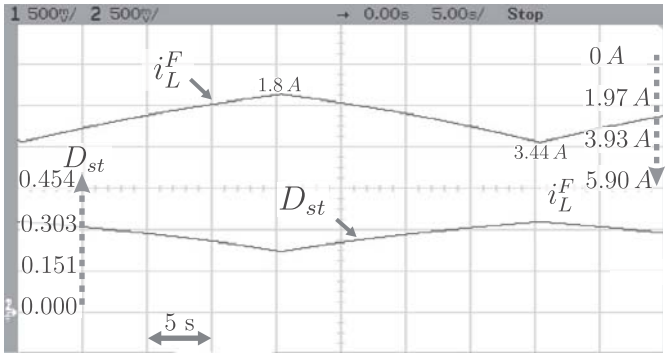


Fig. 13. Signals $i_L^F$ and $D_{st}$ for the experiment of tracking the slowly varying reference.

larger than $V_{DC}$. This leads to a more efficient excitation system because it has to drive a smaller field current. By manipulating the two control inputs using two cascaded control loops, the ZSC can achieve high performance tracking and boosting without showing the typical non-minimum phase response of *buck-boost* converters. The laboratory results validate the proposed control strategy. The performance attained in the experiments satisfies the requirements of the typical application. The proposed control strategy allows the user to select the reference value for $D_1^\star$ following any specified criteria, even as result of an optimization algorithm wich could be the objective of future work.

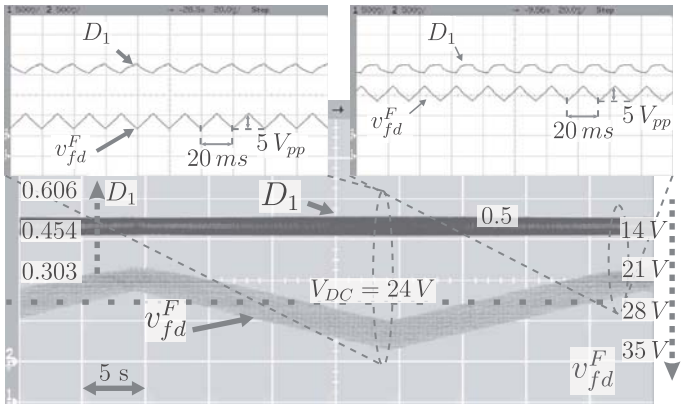


Fig. 14. Tracking the slowly varying reference with the high frequency component added, $v_{fd}^F$ and $D_1$ are shown.

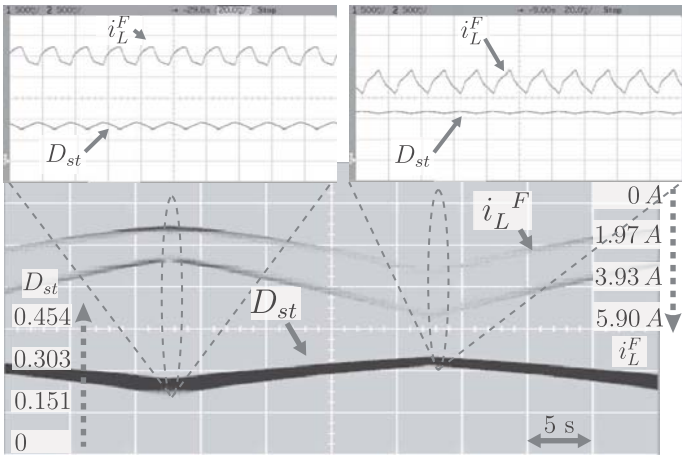


Fig. 15. Tracking the slowly varying reference with the high frequency component added, $i_L^F$ and $D_{st}$ are shown.

## ACKNOWLEDGMENT

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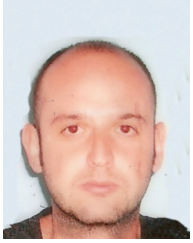

**Santiago J. Amodeo** is a Teaching Assistant and posgraduate student at the Electrical Engineering Department of the Universidad Nacional del Sur, Bahía Blanca, Argentina, since 2006. He received his BSEE degree from the Universidad Nacional del Sur, Bahía Blanca, Argentina, in 2005. His main research interests are Electric Machines and Electric Machines Drives.

**Héctor Gerardo Chiacchiarini** was born in Villa Regina, Argentina, in 1964. He received the B.Sc. degree in electronics engineering from the Universidad Nacional del Sur, Bahía Blanca, Argentina, in 1990. He received the Ph.D. degree in control systems in 1996, also from the Universidad Nacional del Sur. In 2001 stayed as visiting scholar the ETH Zurich, Switzerland, and in 2004 the University of Arkansas, USA. He is a Professor at the Departamento de Ingeniería Eléctrica y de Computadoras, Universidad Nacional del Sur, teaching power electronics and industrial robotics. He is a Researcher, since 1999, at the Instituto de Investigaciones en Ingeniería Eléctrica "Alfredo Desages" (UNS-CONICET). He has over 80 co-authored papers published in journals and conferences, and participated in more than 20 research projects being director of 10 of them. His main research interests are power electronics, robotics, mechatronics, motor drives, and control systems.

**Alejandro R. Oliva** is a Professor at the Electrical Engineering Department of the Universidad Nacional del Sur, Bahía Blanca, Argentina, since 1999. Since 2005 he is a member of CONICET. He received his BSEE degree from the Universidad Nacional del Sur, Bahía Blanca, Argentina, in 1987, his MSEE degree (1996) and his Ph.D. degree (2004) in electrical engineering from the University of Arkansas at Fayetteville, Arkansas, USA. He has published a book and more than 50 journals and proceedings. His main research interests are Power electronics and Power management.