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Modeling tunneling and generation mechanisms governing the nonequilibrium transient in pulsed metal-oxide-semiconductor diodes

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The transient behavior of tunnel metal-oxide-semiconductor structures, pulsed into inversion, is quantitatively described. A simple model for the measured transient currents is proposed, based on the integral form of the continuity equation, leading to an uncoupled solution of the Continuity and Poisson equations. Experimental results for structures with p-type or n-type substrates and different oxide thicknesses are fitted. A map showing the different behavior patterns in terms of surface generation velocity and oxide thickness is given. © 2000 American Institute of Physics. [S0021-8979(00)09522-0]

INTRODUCTION

Tunneling and related phenomena in metal-oxidesemiconductor (MOS) devices are of renewed interest, because of reduced gate oxide thicknesses (<10 nm) due to increased integration density. Tunneling in reverse biased MOS has been investigated with regard to the controversial issue of tunneling carrier type, to establish criteria for strong surface inversion, and in connection with possible simple bistable devices.¹⁻³ Transients in MOS structure relaxing from deep depletion towards equilibrium were previously investigated in connection with the characterization of minority carrier generation mechanisms, and most recently associated to a technological application, namely charge coupled devices.^{4,5} In both cases, it is assumed that the transient leads to the state of thermal equilibrium. The presence of tunneling currents alters this behavior, modifying the transient to yield a steady state distinct from thermal equilibrium.⁶

An exact formulation of the addressed problem requires coupling the Poisson equation, continuity equations for holes and electrons, and complete expressions for the pair generation process, tunneling, and impact ionization. An integral treatment for the continuity equations, as used in this work, leads to a single differential equation describing the evolution towards equilibrium.

The method was implemented and used to analyze three qualitatively different behavior patterns exhibited by:

- (i) *p*-type substrate samples and very thin oxide *n*-type substrate samples, for which minority carriers seem to dominate the tunneling current.
- (ii) Intermediate oxide thickness (3-6 nm) on n substrates, for which majority carriers dominate the tunneling current, but the whole current is limited by the generation of minority carriers.

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(iii) Thicker oxides on *n* substrates, for which the impact ionization mechanism removes the limit imposed to the current by supplying minority carriers.⁶

The model was tested reproducing experimental results in the three regimes, and was used to analyze the dependence of each type of behavior on the thickness and generation parameters.

THEORY AND MODEL

The current flowing through the external circuit, after driving the MOS tunnel diode into deep depletion by a voltage pulse, is obtained from considerations on charge conservation within each of the closed surfaces shown in Fig. 1, for an n-type MOS structure. The rate of change of the gate charge Q_M equals the net current flowing through the surface Σ_1

$$\frac{dQ_M}{dt} = J_{tp} + J_{tn} - J_m, \qquad (1)$$

where J_{tp} is an inward hole current tunneling from the inversion layer, J_{tn} is an inward electron current tunneling to the semiconductor, and J_m is the outward measured current. In a similar way, it is obtained for the inversion charge Q_{inv} enclosed by Σ_2 ,

$$\frac{dQ_{\text{inv}}}{dt} = J_g - J_{tp}, \qquad (2)$$

where J_g is an inward current of holes, generated in the semiconductor space charge region, which are swept into the inversion layer by the electric field. The diffusion current can be neglected as will be shown later (see Discussion).

For the last surface $\boldsymbol{\Sigma}_3$ enclosing the depletion region, charge conservation yields

$$\frac{dQ_{\text{dep}}}{dt} = J_m - J_{tn} - J_g, \qquad (3)$$

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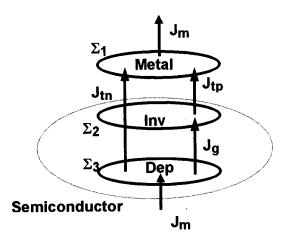


FIG. 1. Schematic representation of the surfaces enclosing the metal (Metal), the inversion layer (Inv) and the depletion region (Dep), considered for continuity Eqs. (1)–(3).

where J_m accounts for the electrons leaving the depletion region towards the substrate which, in turn, equals the measured current. Equations (1)–(3) satisfy overall charge neutrality, i.e., $Q_M + Q_{\text{inv}} + Q_{\text{dep}} = 0$.

The time dependence of all the terms appearing in Eqs. (1)–(3), in particular the measured current J_m , will be calculated as expressions of V_s , the voltage drop in the semi-conductor. The evolution of V_s itself $V_s(t)$ will be obtained by numerical solution of the differential Eq. (2).

THE DIFFERENTIAL EQUATION FOR V_s

An easy way to uncouple the Poisson and continuity equations was proposed by Green and Shewchum⁷ for a non-degenerate semiconductor and diode currents less than $10^4 \, \text{A/m}^2$. The electric field at the semiconductor surface F_s is

$$F_s^2 = \left[\frac{2kT}{\epsilon_s} p_s + \frac{2qN}{\epsilon_s} \left(|V_s| - \frac{kT}{q} \right) \right],\tag{4}$$

where k is the Boltzmann constant, T is the temperature, ϵ_s is the semiconductor dielectric permittivity, N is the dopant concentration, q is the electron charge, p_s is the hole density (cm⁻³) at the semiconductor surface, even in a nonequilibrium condition, and V_s is the semiconductor voltage drop. The conservation of the electric displacement vector yields for F_s as

$$|F_s| = |V_g - V_s - \phi_{\text{ms}}| \frac{\epsilon_{\text{ox}}}{\epsilon_s d},$$
 (5)

where V_g is the applied voltage, d is the oxide thickness and $\phi_{\rm ms}$ is the work-function difference between the metal and the semiconductor and p_s can be expressed as a function of V_s as

$$p_{s} = \frac{(V_{g} - V_{s} - \phi_{\text{ms}})}{2kT\epsilon_{s}} \left(\frac{\epsilon_{\text{ox}}}{d}\right)^{2} - \frac{qN}{kT} \left(|V_{s}| - \frac{kT}{q}\right).$$
 (6)

The inversion layer charge takes the form

$$Q_{\text{inv}} = |V_g - V_s - \phi_{\text{ms}}| \frac{\epsilon_{\text{ox}}}{d} - qNW, \tag{7}$$

where the first term is the semiconductor charge and the second is the depletion region charge. The depletion width, as a function of $V_{\rm c}$, is

$$W = \sqrt{\frac{2\epsilon_s}{qN}|V_s|}. (8)$$

From Eqs. (7) and (8), the variation of $Q_{\rm inv}$ with time in terms of variations of V_s results in

$$\frac{dQ_{\text{inv}}}{dt} = \left[\frac{\epsilon_{\text{ox}}}{d} + \frac{\epsilon_{s}}{W(V_{s})}\right] \frac{dV_{s}}{dt}.$$
 (9)

In the case of samples with oxide layers thinner than 10 nm, as is our case, which are much smaller than typical depletion widths (1 μ m, approximately), the second term in the bracket of Eq. (9) could be neglected. Replacing in Eq. (2), we obtain the differential equation for V_s

$$\frac{dV_s}{dt} = \frac{J_g - J_{tp}}{\left[C_{\text{ox}} + \frac{\epsilon_s}{W}\right]}.$$
 (10)

THE GENERATION CURRENT

The thermal generation current can be divided into two contributions: one due to bulk generation, characterized by a generation lifetime τ_g , proportional to the depletion width, and another one, due to the surface generation, characterized by a velocity S^8

$$J_g = q n_i \frac{W}{2\tau_o} + q n_i S, \tag{11}$$

where n_i is the intrinsic carrier density. The parameters τ_g and S are those obtained using the Zerbst method. Actually, S is not a constant velocity; it starts at a value S_0 , when the surface is depleted immediately after the pulse, falls to an almost constant value S_i , when the surface is inverted, and goes to zero at equilibrium.

The total generation current is thus written as

$$J_g = q n_i \left[\frac{W}{2 \tau_g} + S_i + \frac{S_0}{\left(1 + \frac{p_s}{2n_c}\right)} \right] \times \left[1 - \exp\left(\frac{q V_D}{2kT}\right)\right]. \tag{12}$$

The first square bracket has three terms: the first for bulk generation, proportional to depletion width, the second is a modification of the known expressions to include the generation at the inverted surface, and the last term accounts for the depleted region generation as described in Ref. 9. The second bracket models the approach to equilibrium as in a reverse biased junction, according the Shockley–Hall–Read model, $^{10}\ V_D$ is the difference between the metal Fermi level and the minority carrier quasi-Fermi level (see Fig. 2). As will be seen subsequently, with this simple model of thermal generation, very good fitting of experimental curves is obtained, avoiding the use of more complicated expressions, 11,12 which were intended for experiments with excess carriers, rather than a minority carrier population below the equilibrium value, as in our case.

Considering that, in equilibrium, the product pn equal n_i^2, V_D is written as

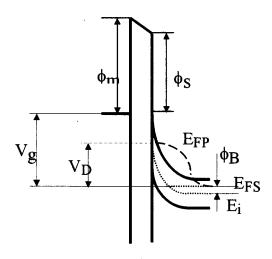


FIG. 2. Nonequilibrium band diagram of the metal-oxide-semiconductor structure.

$$V_D = \frac{kT}{q} \ln \left(\frac{p_s n_B}{n_i^2} \right) + V_s. \tag{13}$$

From Eqs. (12) and (13), the effective generation starts at a value $qn_i(W/2\tau_g+S_i+S_0)$, levels at $qn_i(W/2\tau_g+S_i)$, and finally goes to zero, when the diode reaches equilibrium.

IMPACT IONIZATION

Impact ionization occurs, if the electrons reach the semi-conductor with an energy greater than the threshold value $E_{\rm imp}$ which is approximately $\frac{3}{2}E_g$, 13,14 where E_g is the semi-conductor energy band gap. Electrons tunneling from the metal Fermi level in the semiconductor will have an energy

$$E = qV_{\text{ox}} + q\phi_B - \frac{E_g}{2},$$

where ϕ_B is the bulk electrostatic potential defined in Fig. 2. Thus, the threshold oxide voltage for impact ionization is

$$V_{\rm imp} = \frac{E_g}{q} - \phi_B. \tag{14}$$

Impact ionization is characterized by a parameter α , which expresses the number of ionized pairs per unit distance. If J_{tn}/q is the number of electrons reaching the semiconductor per unit time and area, the number of pairs generated in the space charge region is

$$J_{gi} = \alpha W J_{tn} \,. \tag{15}$$

This is the contribution of impact ionization to the whole generation current, and must be introduced in the first term of Eq. (12), when the oxide voltage drop is greater than the threshold voltage obtained from Eq. (14). It is worth noting that, in case of absence of impact ionization, electron tunneling will affect the measured current but not the evolution of the inversion layer charge towards equilibrium.

THE TUNNELING CURRENTS

For majority carrier tunneling, the following expressions for metal to semiconductor electron tunneling were used ¹⁵ Direct tunneling, $\phi_{ms} < |V_{ox}| < \phi_m$,

$$J_{tn} = C_n \exp(-\alpha_n \phi_s) \exp(-2k_0 d) \times \frac{1}{\alpha_n^2}$$
$$\times \{ \exp[\alpha_n q(|V_{ox}| - \phi_{ms})] - 1 \}$$
(16)

Fowler-Nordheim tunneling $|V_{ox}| > \phi_m$,

$$J_{tn} = C_n \times \left\{ \left(\frac{q |V_{\text{ox}}|}{2k_0 d} \right)^2 \times \exp\left(-2k_0 d \frac{\phi_M}{|V_{\text{ox}}|} \right) - \exp(-2k_0 d) \left[\left(\frac{q \phi_m}{2k_0 d} \right)^2 - \frac{1}{\alpha_n^2} \right] \right\}, \tag{17}$$

where C_n , $\alpha_n y k_0$ are numerical constants, ϕ_m and ϕ_s are the potential barriers from the metal and the semiconductor, respectively.

The extraction of minority carriers by tunneling was modeled with the following expression

$$J_{tp} = (C_p V_T^2 Q_{\text{inv}} + J_g) \times \exp(-2k_0 d) \times \exp(\alpha_p q |V_{\text{ox}}|), \quad (18)$$

where C_p , α_p are numerical constants for the hole tunneling, retaining the exponential dependence of the current on the oxide voltage drop ($V_{\rm ox} = V_g - V_s$) reported in the direct tunneling regime. The preexponential factor represents the total supply of carriers with velocity normal to the barrier. This current is composed of carriers in the inversion layer, accounted by the first term proportional to $Q_{\rm inv}$, and carriers generated and driven to the surface (J_g), which must be introduced, if one expects to analyze the case of ultrathin oxides. Such structures behave, in the limit, like a Schottky diode, in which no inversion layer forms, $Q_{\rm inv} \approx 0$. The main supply of tunneling carriers is, thus, the generation current J_g . For p-type substrates, Eq. (18) applies to electron tunneling, with the sole change of subindex p by n.

Replacing Eqs. (12)–(18) in Eq. (10), a differential equation for V_s , as a function of time is obtained. This is an ordinary first order nonlinear equation, which must be solved numerically.

FITTING EXPERIMENTAL TRANSIENTS CURRENTS

The transient currents of an MOS diode, pulsed into depletion, can be classified, as was shown recently,⁶ in three different behavior patterns, namely:

- (a) Dominated by minority carrier tunneling current.
- (b) Presence of both types of carriers tunneling, with the current limited by the generation of minority carriers.
- (c) Presence of both types of carriers tunneling, without limitation by the minority carrier generation, which is enhanced by impact ionization.

Case a is observed in the *p*-type substrate capacitors or in *n*-type, with very thin insulators (up to about 3 nm). In *n*-type substrate samples, with oxide thickness between 3 and 6 nm, impact ionization may occur but it is insufficient for

TABLE I. Summary of values used in the calculations. Constants in the table refer to accepted values in the literature. Values of the fitting parameters were chosen to reproduce the experimental results.

Sample		<i>p</i> 5	n3	G11
Measured device parameters	d (nm)	4.5	3.7	6.3
	$A(10^{-4} \text{ cm}^2)$ $N(\text{cm}^{-3})$	3.24 2.5×10^{15}	$3.24 \\ 2.5 \times 10^{15}$	5 2.5×10^{15}
Tunneling constants	$\phi_m(V)$ $\phi_s(V)$ $k_0 \text{ (cm}^{-1})$	3.2 3.06 3.76×10^7	3.2 3.06 3.76×10^7	3.2 3.06 3.76×10^{7}
Tunneling fitting parameters	$C_p(s^{-1} V^{-2})$ $\alpha_p (V^{-1})$	2.88×10^{5}	3.2×10^{10} 3.3	3.2×10^{10} 3.3
	$C_n(A V^{-2} cm^{-2})$ $\alpha_n (V^{-1})$		2.42×10^{8}	7.1×10^7
Generation fitting	$ au_g \ (\mu ext{s})$	10	60	1.7
parameters	S_0 (cm/s) S_i (cm/s)	50 150	1 0.9	200 10
Impact ionization	α (1/cm)		0	10 000
fitting parameters	$V_{\text{imp}}\left(\mathbf{V}\right)$	•••	-1.8	-1.8

removing the generation limitation (case b). Case c occurs for *n*-type substrate samples, with oxides thicker than approximately 6 nm.

Figures 3–5 show a family of experimental curves, pertaining to each one of the described cases, fitted with the proposed model above. Details of the experimental work are given in Ref. 6. All the parameters used in the calculations are given in Table I.

Figure 3 shows the current versus time curves for a *p*-type diode with a 4.5 nm oxide thickness, for several gate voltage pulse amplitudes. The curves are representative of the behavior of *p*-type samples in general, and *n*-type samples driven with low voltage pulses. Curves for voltages lower than 2 V are typical of structures for which tunneling can be neglected. After the initial decaying contribution of

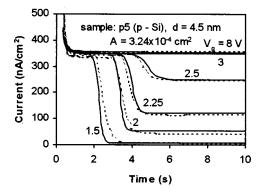


FIG. 3. Experimental (dotted) and modeled (solid) current vs time curves for a *p*-type diode with 4.5 nm oxide thickness (*p*5), for several gate voltage pulse amplitudes. These curves are representative of the behavior of *p*-type samples in general, and *n*-type samples driven with low voltage pulses.

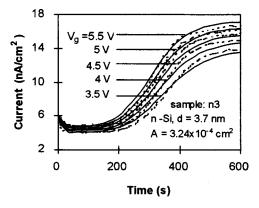


FIG. 4. Experimental (dotted) and modeled (solid) current vs time curves for a n-type sample with 3.7 nm oxide thickness (n3), for several gate voltage pulse amplitudes. The measured increasing current is a mixture of majority and minority carrier contributions.

the depleted surface, the curve has a very slight negative slope corresponding to both bulk and inverted surface contribution, which disappear at equilibrium. Curves for *n*-type samples with very thin oxide thicknesses would look like those shown in this figure for 3 and 8 V, provided the stationary state is achieved immediately after the pulse is applied. This case is modeled with thermal generation and direct tunneling of only minority carriers.

Case b is represented by a 3.7 nm oxide on a *n*-substrate diode with transient currents as shown in Fig. 4. In the first 200 s, the diode exhibits a similar pattern to that of p-type substrate; after that, the increasing oxide voltage is sufficient for the majority carrier (electrons) tunneling current to dominate the measured current. Even if the composition of the observed current is a mixture of majority and minority carriers, the evolution and the final state are controlled by the balance between thermal generation and extraction of holes from the inversion layer by tunneling, 6 i.e., the current is generation limited. This behavior pattern was modeled neglecting impact ionization ($\alpha = 0$). Minority and majority carrier tunneling are in the direct tunnel regime. For the current to be in the Fowler-Nordheim regime, the oxide voltage should be greater than the barrier height (3.2 V, approximately), which is a voltage higher than the threshold for impact ionization. Thus, the beginning of impact ionization would be expected before the change of tunneling regime.

Figure 5 is for a 6.3 nm oxide on a *n*-substrate structure. In this sample, impact ionization begins during the relaxation process. The wider spread of the curves is due to the additional generation by impact ionization, which supplies enough carriers to keep the population of the inversion layer close to the equilibrium value, thus preventing the current to be generation limited. Hence, almost all the applied voltage will drop in the insulator allowing Fowler–Nordheim tunneling to occur.

BEHAVIOR PATTERN MAP

In contrast to *p*-type substrate samples, in which a unique kind of transient response is observed, in *n*-type substrate samples, the behavior pattern is determined by oxide thickness and minority carrier generation parameters. An ef-

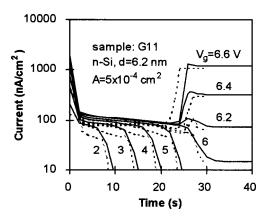


FIG. 5. Experimental (dotted) and modeled (solid) current vs time curves for a *n*-type sample with 6.3 nm oxide thickness (G11), for several gate voltage pulse amplitudes. Impact ionization begins during the relaxation process.

fective velocity $S_{\rm eff}$ equal to the main component of the generation current density J_g , divided by qn_i , will be used to characterize this generation. $S_{\rm eff}$ takes the values S_0 , S_i , or $W_{\rm inv}/2 au_g$, the last when the bulk dominates the generation rate. W_{inv} is the depletion width for $p_s = N$ obtained from Eqs. (6) and (8). A map for the different behaviors can therefore be constructed on a plane with coordinates of effective velocity and oxide thickness (Fig. 6). This plot is divided into four regions corresponding to the Schottky diode-like behavior, and the three patterns shown in Figs. 3-5, i.e., minority carrier dominated tunneling, majority carrier dominated tunneling, and impact ionization assisted tunneling. The boundaries between those regions, can be determined as follows: in the stationary state, the generation current must be equal to the hole tunnel current, J_{tp} . Thus, for the steady state the generation current is

$$J_g = q n_i S_{\text{eff}} = J_{tp}(V_{\text{ox}}, d). \tag{19}$$

Substituting Eq. (18) into Eq. (19) results in

$$S_{\rm eff} = \frac{C_p V_T^2 Q_{\rm inv}(V_{\rm ox}, d)}{q n_i} \left[\exp(2k_0 d) \exp(-\alpha_p q |V_{\rm ox}|) - 1 \right]^{-1}. \tag{20} \label{eq:Seff}$$

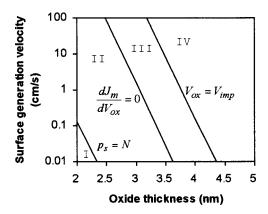


FIG. 6. Behavior pattern map. Region I: Schottky diode-like behavior, region II: minority carrier dominated tunneling, region III: majority carrier dominated tunneling, region IV: impact ionization assisted tunneling.

The boundary curves in the planar coordinates, $S_{\rm eff}$ and d, are obtained from Eq. (20), by replacing $V_{\rm ox}$ with the appropriate values at the corresponding boundaries as follows:

Boundary I–II: The difference between behavior type I and type II is due to the existence of the inversion layer in the latter, whereas no inversion layer forms in the Schottky diode-like behavior of the former. Thus, the value for p_s delimiting both regions is $p_s = N$, which, once replaced in Eq. (6), yields

$$V_{\text{ox}}^{I-II} = qN\epsilon_s \left(\frac{d}{\epsilon_{\text{ox}}}\right)^2 \left[1 - \sqrt{1 + \frac{2|Vg|}{qN\epsilon_s} \left(\frac{\epsilon_{\text{ox}}}{d}\right)^2}\right]. \tag{21}$$

Using this value in Eqs. (7) and (20), the limit between regions I and II is obtained.

Boundary II-III: If increasing currents along the relaxation transient (region III) are observed, the measured current has a minimum for an oxide voltage lower than the stationary value. This minimum occurs [cf. Eq. (3)] neglecting the contribution of the depletion region reduction when

$$\left| \frac{dJ_g}{dV_{\text{ox}}} \right| = \left| \frac{dJ_{tn}}{dV_{\text{ox}}} \right| \tag{22a}$$

because the thermal generation current, as a function of oxide voltage always has a negative slope and the majority carrier tunneling current is a monotonic increasing function of $V_{\rm ox}$.

The oxide voltage obtained from Eq. (22a) is a function of τ_g and S_i . The values for both parameters are obtained from the following two equations:

$$J_{\varrho} = J_{tp} \,, \tag{22b}$$

which is the limiting case of $J_{tp} < J_g$. A second condition for the observation of the minimum to be observed, i.e., its occurrence before the stationary state [Eq. (22b)] attained is

$$J_{g} = J_{tn}, \qquad (22c)$$

which is necessary in order to observe the increasing current. Substituting Eqs. (12) and (16)–(18) into (22a)–(22c) we obtain

$$J_{tn}(V_{\text{ox}}) = \frac{C_p V_T^2 Q_{\text{inv}}(V_{\text{ox}}, d)}{\left(\frac{qNW^2 \alpha_n}{2\epsilon_s} + 1\right) \left[\exp(2k_0 d) \times \exp(\alpha_p q V_{\text{ox}}) - 1\right]},$$
(23)

which yields the stationary oxide voltage for which the minimum occurs. This value, replaced in Eq. (20), yields the limit between regions II and III.

Finally, substituting the threshold for impact ionization ($V_{\rm imp}$ = 1.8 V approx.) for the stationary $V_{\rm ox}$ in Eq. (20), the limit between regions III and IV is obtained.

DISCUSSION

A thorough treatment of the MOS structure to simulate its relaxation towards thermal equilibrium should include the numerical solution of the coupled Poisson and Boltzmann transport equations. The present model uses known phenomenological expressions with slight modifications, to describe

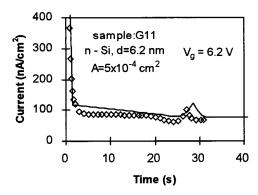


FIG. 7. Experimental (symbol) and modeled (solid) current vs time curves for the 6.3 nm oxide thickness *n*-type sample (G11), with 6.2 V applied to the gate.

quantitatively the physical mechanisms giving rise to different observed behavior patterns, which had been already analyzed qualitatively.⁶

Despite the phenomenological approach, the model can reproduce features with great detail. See, for instance, the singular case in Fig. 7: a curve for the 6.3 nm *n*-type sample, with 6.2 V applied to the gate, for which a peak in current appears at approximately 30 s, closed matched by the theoretical curve and can be associated to the onset of impact ionization. Probably the greatest inaccuracies of the model are encountered in the time evolution of the surface generation. The usual characterization of the phenomenon through parameters such as generation lifetime and generation velocities apparently leads to an oversimplification, which results in slight deviations from the experimental curves in the approach to equilibrium, as can be observed in Fig. 3, or in the beginning of impact ionization in Fig. 5.

Equation (2) neglects the diffusion current, i.e., all the minority carriers generated in the depletion region are driven towards the surface, so the hole current in the semiconductor bulk is zero. This assumption is valid for Si at room temperature.²⁰

The map in Fig. 6 may help in dealing with a number of different issues: (i) Previous contributions^{5,21,22} have addressed the question of how thin MOS structures should be to behave as Schottky diodes. Calculations by Wang *et al.*² established a 3 nm critical oxide thickness, for which the structure cannot be inverted if minority carriers are not supplied externally. Figure 6 provides an explicit answer to this problem, in terms of oxide thickness and generation parameters. For typical generation parameter values, the oxide thickness for Schottky diode-like behavior compares well with those previously reported.

- (ii) The issue of the dominant tunneling carrier type. The map shows that whereas for usual generation velocities, in the thinnest structures, the measured current is minority carrier dominated (behaviors I and II); for thicker oxides, in region III, the dominant type of carrier switches from minority to majority with increasing reverse bias voltage, as has been previously reported in the literature. 1,22,23
- (iii) Finally, a brief comment about the bistable MOS tunnel diode, a device described by Lai *et al.*, ²⁴ with characteristic curves shown in Fig. 8. The behavior pattern of this

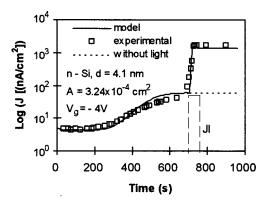


FIG. 8. Bistable MOS tunnel diode behavior. This behavior can be interpreted as a shift of the structure from region III to region IV, caused by the illumination related generation (J1), and locked there by impact ionization.

n-type substrate sample corresponds to region III for times shorter than 700 s. The diode would remain in this stationary state if no perturbation were applied. At 700 s, the structure receives a pulse of light, which produces an additional supply of minority carriers to the inversion layer. The oxide voltage grows, triggering impact ionization, and the structure jumps to a higher current state. After the light is switched off, impact ionization maintains the structure in this high current state. In terms of the proposed behavior pattern map, this process can be interpreted as a shift of the structure from region III to region IV, caused by the addition of an illumination related generation term, altering the value of $S_{\rm eff}$, followed by the locking of the structure in region IV, due to impact ionization triggered in this new condition, which sustains the high value of $S_{\rm eff}$, after the illumination is removed. Whereas the first step occurs for any thin oxide, the sample must be near the border of regions III-IV, for the process to be completed and the bistable behavior to be observed.

The applied voltage does not substantially alter the map shown in Fig. 6, for values below 300 V. At higher applied voltages, impact ionization can start immediately after the structure is biased, which is the typical behavior of diodes with oxides thicker than those used here.

CONCLUSION

The transient behavior of a metal-oxide-semiconductor tunnel diode, pulsed into inversion, was simulated with a simple model, based on the integral form of the Continuity and Poisson equations. The model takes into account several minority carrier generation mechanisms, such as thermal generation, impact ionization, and illumination, as well as tunneling effects; and fairly reproduces the experimental results. A map, with planar coordinates of oxide thickness and effective generation velocity, determines the kind of transient observed. The map seems to be a useful tool for the analysis of tunneling induced out of equilibrium phenomena.

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