A New SST Topology Comprising Boost Three-Level AC/DC Converters for Applications in Electric Power Distribution Systems

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***Abstract*—The growing interest in integrating distributed generation (DG) into the existing power distribution grid, the increase in the penetration levels of renewables, as well as the need to achieve a more efficient, reliable and sustainable grid, are leading to the development of new grid-interfaced power converters such as the solid-state transformer (SST). As current and voltage ratings of commercially available power semiconductor devices are normally below power ratings required in distribution systems (e.g., 13.8 kVrms), multiple modules must be connected in cascade configuration at the high-voltage side to reach higher voltage ratings as well as in parallel at the low-voltage side to achieve high current levels.**

A new SST topology consisting of modular boost-based three-level ac-dc converters, medium-frequency transformers with two secondary windings, and four-leg ac-dc converters is presented in this paper. When compared to similar approaches, the proposed topology comprises fewer power conversion stages, lower voltage across the semiconductor devices on the high-voltage side, and lower current flowing through each device on the low-voltage side. These characteristics reduce the number of series-connected modules in the high-voltage side and parallel-connected devices in the low-voltage side. The feasibility of the proposed topology is experimentally validated on a 500 W, 120 Vac/ 48 Vdc scaled-down prototype.

***Index Terms*— Boost-based topology, four-leg dc-ac converter, multi-winding solid-state transformer (SST), three-level dc-ac converter.**

I. Introduction

During the last decades, factors such as changes in the power grid structure, the increase of penetration levels of renewables, the implementation of dc grids, and the need to offer premium power quality to customers have motivated utilities to implement new power electronic interfaces (PEI) to modernize the conventional power distribution system. One of the most helpful and promising PEI in future power grids is the so-called solid-state transformer (SST), which has been proposed to replace the bulky fundamental-frequency transformers for several applications [1]–[7]. In addition to the functionalities of conventional transformers (e.g., galvanic isolation between networks and voltage matching between two voltage levels), the SST is capable of controlling the power flow between networks, limiting fault currents, integrating energy storage units, compensating for reactive power, improving power quality, and many others. These assets make the SST a promising technology in future smart grids at any voltage and power level [3]–[5].

There have been several topologies suggested for SSTs [8]–[10]. However, the three-stage approach consisting of an ac-dc front-end side, a dual active bridge (DAB) with a high- or medium-frequency transformer (HF- or MF-XFMR) to step down or up the input voltage [11], [12], and a back-end side incorporating dc-ac or dc-dc converters for 50/60 Hz or dc loads, respectively, have been the most evaluated. To interface directly with a distribution system (from 2.3 kV to 35 kV single-phase feeders), several converters are connected in a cascaded H-bridge multilevel configuration at the front-end or high-voltage (HV) side [8], [9]. This configuration allows the use of commercially available power semiconductor devices with medium breakdown voltages (e.g., 4.5 kV and 6.5 kV IGBT) and has less current harmonic distortion at the ac side, which in turn reduces filter requirements at the system connecting point. Complex voltage balancing control methods are required to keep the dc-link voltage in the H-bridges constant [13], [14]. At the back-end side or low-voltage (LV) side several modules are connected in parallel to achieve the current rating imposed by the load. The dc bus can potentially be used to connect a dc distribution system involving distributed generation (DG) units (e.g., photovoltaic panels, energy storage, etc.) and dc loads (e.g., dc buildings, data centers, battery-charging stations, etc.). Depending on the output voltage and power level, Si and SiC MOSFETs or IGBTs are used for the LV side bridge.

Usually, dc loads are fed from three-phase power factor correction (PFC) rectifiers connected to the power grid though a medium-to-low voltage, fundamental-frequency transformer.

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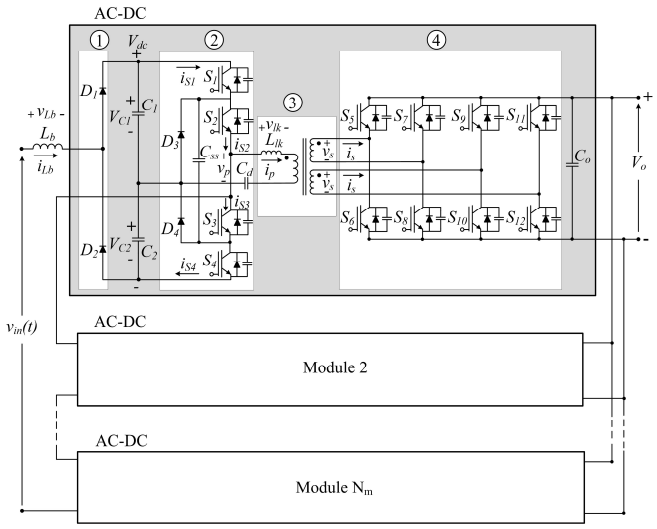

Fig. 1. Boost-based three-level SST topology with high-voltage ac input (e.g., 7.2 kV) and a low-voltage dc output (e.g., 400 V).

However, single-phase SST topologies connected to the medium-voltage grid and composed of a rectifier stage and a DAB stage are used for dc applications to eliminate the use of the low-frequency transformers [15]. The DAB stage is commonly implemented with full-bridges on primary and secondary sides [12], [16]; half-bridges on primary and secondary sides [6], or a half-bridge on primary (HV) side and a full-bridge on the secondary (LV) side [9]. To reduce the required number of conversion stages, a unidirectional SST topology based on a boost converter PFC stage [17], [18] requiring reduced number of devices by combining the rectifier stage with the primary side bridge of the DAB was presented in [9]. However, it is not suitable for applications with variable output power since it is required to operate the primary side of the DAB with a fixed 50% duty cycle. This means that a fixed 50% duty cycle will be applied to a boost inductor operating at discontinuous conduction mode (DCM), which sets a limit for the minimum output power delivered. A three-phase, three-level, unidirectional, boost-based ac-dc converter that combines a three-phase PFC rectifier stage with the primary side of a three-level isolated converter with a diode bridge at the output was presented in [19]. The three-level waveform at the primary side of the DAB transformer allows the user to set the desired duty cycle for the PFC boost inductor operating at DCM, so the input power can be controlled. The problem with this topology is that it is not possible to control the intermediate primary side voltage and the output voltage at the same time. Therefore, the bus voltage will fluctuate depending on load conditions from a low value defined by the limit of continuous conduction (CCM) of the boost inductor to a much higher voltage at light loads. This requires the overrating of the active devices, which is not suitable for HV applications.

To solve the issues of the previous mentioned topologies, this paper presents a new SST topology with a reduced number of series-connected stages on the front-end side [20]. The proposed topology, illustrated in Fig. 1, is suitable for applications where power flows in one direction, such as dc buildings and server farms, while keeping other functionalities of a fully-featured SST. As shown, it comprises a boost-based three-level converter stage, a high-frequency (HF) or medium-frequency (MF) transformer with two secondary windings, and a four-leg full-bridge rectifier. The use of the two secondary windings makes the new topology suitable for LV and high-power applications such as information technology applications. This topology allows to fully control the primary-side dc link as well as the output voltages with the possibility to operate the converter with zero-voltage switching (ZVS) and quasi-zero-current switching (quasi-ZCS) for the whole operating power range.

The paper is organized as follows: An analysis of the proposed topology including the new topology general description, component sizing, and steady-state operating intervals is presented in Section II. Then, soft-switching operation, selection of duty cycles, phase-shift and control strategy is shown in Section III. The design procedure is presented in Section IV; and lastly, the feasibility of the proposed solution is validated through experimental results in Section V.

II. Analysis of the Boost Topology

A. SST Topology General Description

The single-phase boost-based three-level SST topology illustrated in Fig. 1 comprises four stages for converting a higher ac voltage into a lower dc voltage. The input boost inductor L_b is designed to operate in the discontinuous conduction mode (DCM). The fact that the inductor's peak current is proportional to the input voltage allows for a high power factor at the input [21], [22]. At the front-end, a cascaded multilevel ac-dc converter is adopted (①) to accomplish high input voltage levels. A three-level neutral-point-clamped dc-ac converter (②) is used to interface with the primary side of the HF- or MF-XFMR (③). The power semiconductor devices sustain only half of the module dc link voltage due to the three-level half-bridge configuration [23], facilitating the selection of devices having lower breakdown voltages which can operate at higher switching frequencies. The transformer is designed to have two secondary windings, which reduces the current stresses on the secondary side devices. Each secondary of the transformer is connected to a full-bridge ac-dc converter (④). A single secondary and conventional full-bridge may be used, however, the four-leg full-bridge configuration enables the use of devices with lower rated currents. Furthermore, several modules are connected in parallel to the LV dc link. The use of a full-bridge transistor configuration instead of a full-bridge diode rectifier allows to fully control dc link voltage V_{dc}, which otherwise changes depending on load conditions.

The modulation scheme for the three-level dc-ac converter is presented in Fig. 2. This scheme allows for two different three-level voltages; one applied to the primary side (v_p) and the other to the secondary side (v_s) of the transformer [24], [25]. The phase-shift between v_p and v_s is defined as ϕT_{hs},

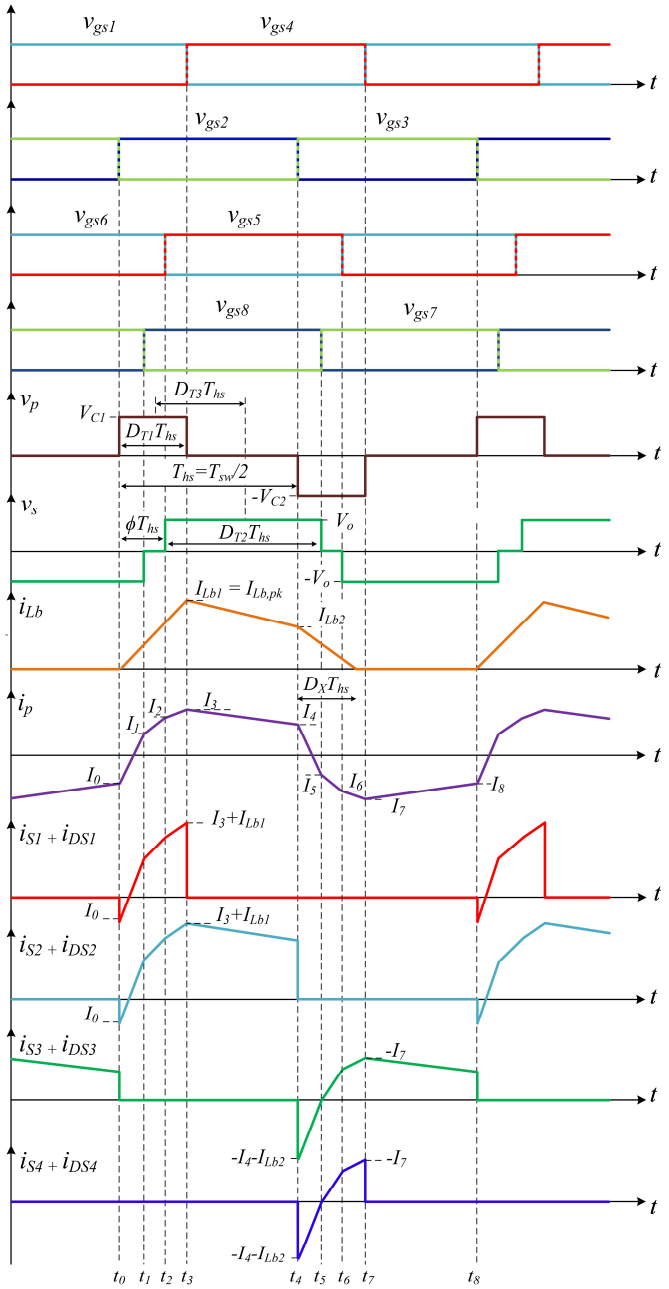

Fig. 2. Theoretical waveforms of the proposed topology.

where T_{hs} corresponds to half a switching period ($T_{sw}/2$).

The phase-shift between the fundamental components of v_p and v_s is $D_{T3}T_{hs}$ which can be expressed in terms of the duty cycles and the phase-shift ϕ as:

$$D_{T3} = \phi + \frac{D_{T2}}{2} - \frac{D_{T1}}{2}. \quad (1)$$

The time instant where the primary and secondary voltages are not equal to zero are defined as $D_{T1}T_{hs}$ and $D_{T2}T_{hs}$, respectively. As explained later, the duty cycles D_{T1} and D_{T2} and the fundamental phase-shift D_{T3} are used to control the dc link voltage (V_{dc}) and output voltage (V_o). The duty cycles D_{T1} and D_{T2} can vary from 0 to 1 while the phase-shift D_{T3} can change from 0 to 0.5. With this modulation scheme, it is possible to obtain eight commutation intervals during a switching cycle, as illustrated in Fig. 3.

As shown in Fig 2, the boost inductor L_b is charged during $D_{T1}T_{hs}$ when both S_1 and S_2 are on (for $v_{in}(t) > 0$). The switches S_3 and S_4 facilitate the inductor charging process when $v_{in}(t) < 0$. For the sake of the analysis, only the positive cycle of the 60 Hz input grid voltage is considered.

In the case of series connected primaries and parallel connected secondaries, ideally all converters will operate the exact same way as a single converter. Any voltage variance among the primary dc buses would need to be corrected by modifying the power output of each separate converter using the phase-shift control.

B. Steady-State Operating Intervals

Interval 1 [$t_0 - t_1$]: Initially, the transformer primary side current (i_p) is negative and flows through the capacitor C_1 and the antiparallel diodes of S_1 and S_2. When S_1 and S_2 are both on, the boost inductor current (i_{Lb}) increases linearly in time at a rate of $v_{in}(t)/L_b$. In this interval, the capacitor voltage (v_{C1}) is applied to the primary side of the transformer. The voltage across one of the transformer's secondary windings is $-V_o$ and the current flowing through them is i_s. When this current is negative, it flows through the antiparallel diodes of S_6, S_7, S_{10} and S_{11}. When positive, it flows through the corresponding IGBTs.

Moreover, the voltage across the leakage inductance (v_{lk}) is calculated as $V_{C1} + nV_o$, where $n = N_p/N_s$ is the turns ratio of the HF transformer. Because v_{lk} is positive, i_p increases with a constant slope.

During this interval, the current i_p is

$$i_p(t) = I_0 + \frac{V_{C1} + nV_O}{L_{lk}}(t - t_0), \quad (2)$$

where L_{lk} is the transformer's leakage inductance and the initial condition I_o is calculated as follows:

$$I_0 = -\frac{nV_O}{4 f_{sw} L_{lk}}\left(-2 + D_{T1} + \frac{V_{C1}}{nV_O} D_{T1} + 2D_{T3}\right), \quad (3)$$

where $V_{C1} = V_{C2} = V_C = V_{dc}/2$. A constant m is defined as the voltage conversion ratio $m = nV_o/V_C$. When $m > 1$, the converter is operating in boost mode and when $m < 1$, the converter operation is in buck mode. In this paper, the buck mode of operation is of interest.

From Fig. 2, the duration of *interval 1* is given by:

$$t_1 - t_0 = \left(\frac{D_{T1}}{2} + \frac{D_{T2}}{2} + D_{T3} - 1\right) T_{hs}. \quad (4)$$

Interval 2 [$t_1 - t_2$]: At t_1, switches S_7 and S_{11} turn completely off and the antiparallel diodes of the switches S_8 and S_{12} become forward biased, bringing v_s to zero. This interval defines the zero for the three-level secondary voltage whose duration is $(1 - D_{T2})T_{hs}$. The current flowing through the upper secondary winding is conducted by S_6 and the antiparallel diode of S_8, whereas the current flowing through the lower secondary winding is conducted by S_{10} and the antiparallel diode of S_{12}. The voltage v_{lk} is equal to V_{C1}, thus i_p is:

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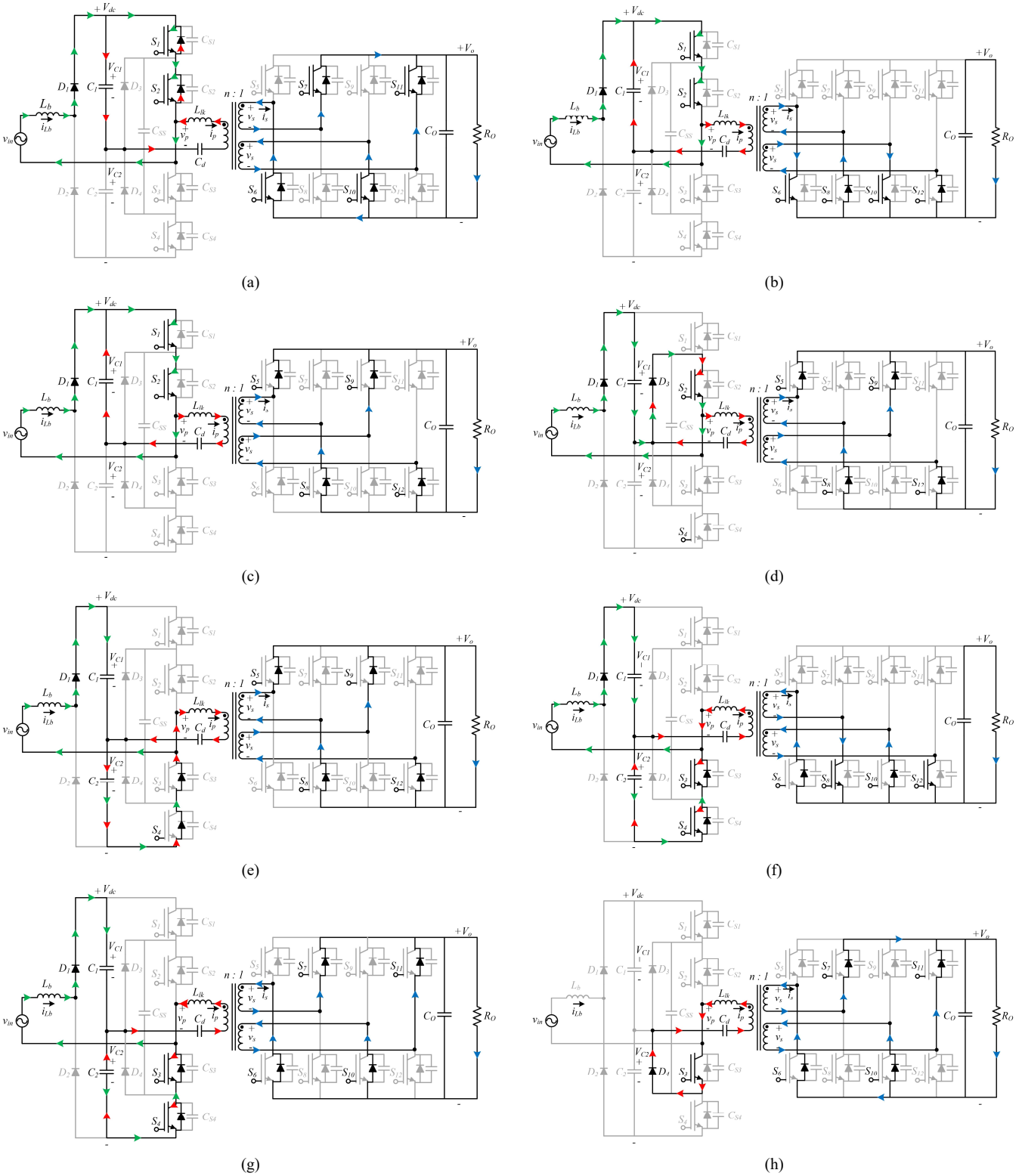

Fig. 3. Equivalent circuits for: *interval 1* [$t_0 - t_1$] (a), *interval 2* [$t_1 - t_2$] (b), *interval 3* [$t_2 - t_3$] (c), *interval 4* [$t_3 - t_4$] (d), *interval 5* [$t_4 - t_5$] (e), *interval 6* [$t_5 - t_6$] (f), *interval 7* [$t_6 - t_7$] (g), *interval 8* [$t_7 - t_8$] (h).

$$i_p(t) = I_1 + \frac{V_{C1}}{L_{lk}}(t - t_1), \tag{5}$$

where the initial condition I_1 is calculated as:

$$I_1 = -\frac{nV_O}{4 f_{sw} L_{lk}} \left(\frac{V_{C1}}{nV_O}(2 - D_{T2} - 2D_{T3}) - D_{T2} \right). \tag{6}$$

Interval 3 [$t_2 - t_3$]: The switches S_6 and S_{10} turn off at t_2 and

i_s is conducted by the antiparallel diodes of S_5, S_8, S_9 and S_{12}. The output voltage is applied to the secondary windings of the transformer, thus v_{lk} is equal to $V_{C1} - nV_o$. For the theoretical waveforms presented in Fig. 2, V_{C1} is larger than nV_o and i_p keeps increasing as:

$$i_p(t) = I_2 + \frac{V_{C1} - nV_O}{L_{lk}}(t - t_2), \tag{7}$$

where the initial condition I_2 is equal to:

$$I_2 = -\frac{nV_O}{4 f_{sw} L_{lk}}\left(\frac{V_{C1}}{nV_O}(D_{T2} - 2D_{T3}) - D_{T2}\right). \tag{8}$$

The duration of this interval can be determined as:

$$t_3 - t_2 = (D_{T1} - \varphi)T_{hs} = \left(D_{T1} - \frac{D_{T2}}{2} + D_{T3}\right)T_{hs}. \tag{9}$$

Interval 4 [$t_3 - t_4$]: This interval determines the duration for the zero state of the transformer primary side, $(1 - D_{T1})T_{hs}$. After S_1 turns off, the current flowing through the free-wheeling diode D_3 is equal to i_p plus the current of the boost inductor, which gets discharged through C_1. The voltage applied to the leakage inductance is negative and i_p decreases as:

$$i_p(t) = I_3 - \frac{nV_O}{L_{lk}}(t - t_3), \tag{10}$$

where the initial condition I_3 is calculated as:

$$I_3 = \frac{nV_O}{4 f_{sw} L_{lk}}\left(\frac{V_{C1}}{nV_O} D_{T1} - D_{T1} + 2D_{T3}\right). \tag{11}$$

At the end of this interval $t = T_{sw}/2$.

Interval 5 [$t_4 - t_5$]: After S_2 is turned off, the currents i_p and i_{Lb} flow through the antiparallel diodes of S_3 and S_4. The energy stored in the boost inductor L_b is transferred to capacitors C_1 and C_2 and the voltage applied to the primary side of the transformer is $-V_{C2}$. Thus, the primary current is:

$$i_p(t) = I_4 - \frac{V_{C2} + nV_O}{L_{lk}}(t - t_4), \tag{12}$$

where I_4 is equal to $-I_0$. If during this interval, the transformer current changes its polarity, the current is conducted through S_3 and S_4 in the primary side and through S_5, S_8, S_9 and S_{12}, in the secondary side, respectively.

Interval 6 [$t_5 - t_6$]: This interval takes place after S_5 and S_9 turn off. The voltage v_s is equal to zero and the upper winding current i_s flows through the antiparallel diode of S_6 and the switch S_8, whereas the lower winding current flows through the antiparallel diode of S_{10} and the switch S_{12}. In this interval, the boost inductor keeps discharging through the capacitors C_1 and C_2. The primary winding current is calculated as:

$$i_p(t) = I_5 - \frac{V_{C2}}{L_{lk}}(t - t_5), \tag{13}$$

where I_5 is equal to $-I_1$.

Interval 7 [$t_6 - t_7$]: The switches S_8 and S_{12} turn off and the antiparallel diodes of S_6 and S_7 conduct i_s for the upper winding whereas the antiparallel diodes of S_{10} and S_{11} conduct the currents for the lower winding. In this interval, the boost inductor current goes to zero and the primary current is calculated as:

$$i_p(t) = I_6 + \frac{-V_{C2} + nV_o}{L_{lk}}(t - t_6), \tag{14}$$

where I_6 is equal to $-I_2$.

Interval 8 [$t_7 - t_8$]: After S_4 turns off, the current i_p free-wheels through S_3 and D_4 while i_s is conducted by the diodes of S_6, S_7, and S_{10}, S_{11} for the upper and lower windings, respectively. The primary current is then given by:

$$i_p(t) = I_7 + \frac{nV_o}{L_{lk}}(t - t_0), \tag{15}$$

where I_7 is equal to $-I_3$.

TABLE I
PEAK AND RMS CURRENTS

Boost Inductor Current
$I_{Lb,rms} = \frac{V_{C1}}{\sqrt{8\pi} L_b f_{sw}} \sqrt{\int_0^{\phi_{cn}} \left(\frac{D_{T1}^2 \sin\omega t}{g - 2\sin\omega t}\right)^2 d\omega t + \int_{\phi_{cn}}^{\pi/2} \left(\frac{2(D_{T1}^2+1)\sin\omega t - g(D_{T1}-1)^2}{4(g - \sin\omega t)}\right)^2 d\omega t}$
$I_{Lb,pk} = \frac{V_{pk} T_{sw}}{2L_b}$
Rectifier Diode Current
$I_{D1,RMS} = I_{D2,RMS} = \frac{I_{Lb,RMS}}{\sqrt{2}}$
$I_{D1,pk} = I_{D2,pk} = I_{Lb,pk}$
Switch Current
$I_{S1,RMS} = I_{S4,RMS} \cong \frac{I_3 D_{T1}}{2\sqrt{2}} + \frac{V_{pk} D_{T1}^2}{16 L_b f_{sw}}$
$I_{S2,RMS} = I_{S3,RMS} \cong \frac{I_{Lb,RMS}}{2} + \frac{I_3}{2\sqrt{2}}$
$I_{S1,pk} = I_{S2,pk} = I_{S3,pk} = I_{S4,pk} = I_3 + I_{Lb,pk}$
$I_{S5,pk} = I_{S6,pk} = I_{S7,pk} = I_{S8,pk} = I_{S9,pk} = I_{S10,pk} = I_{S11,pk} = I_{S12,pk} = \frac{nI_3}{2}$
Free-Wheeling Diode Current
$I_{D3,RMS} = I_{D4,RMS} = I_3\sqrt{\frac{1 + D_{T1}^2}{32}}$
$I_{D3,pk} = I_{D4,pk} = I_3 + I_{Lb,pk}$

C. Efficiency Model

Table I summarizes the expressions for the peak and RMS currents of the semiconductors.

D. Power Factor (PF) Calculation

When the input current is discontinuous, the peak of the inductor current follows the ac input voltage waveform. However, when the boost inductor discharges, there is a distortion introduced by the modulation of the off time [22]. In the case of the proposed converter, the inductor current will discharge with one or two slopes depending on the applied level of the ac input voltage and the duty cycle D_{T1}, as shown

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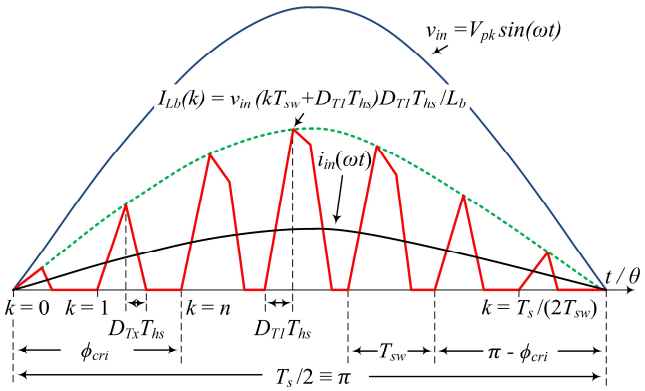

Fig. 4. Graphical representation of the input boost inductor current.

in Fig. 4. The critical angle ϕ_{cri}, which defines the limit between the operations with one or two slopes, is calculated as [19]:

$$\phi_{cri} = \sin^{-1}\left[\frac{g}{2}(1 - D_{T1})\right], \tag{16}$$

where $g = V_{dc}/V_{pk}$.

The average boost inductor current is calculated considering the intervals where the current has one or two slopes:

$$i_{in}(\omega t) = \begin{cases} i_{in1}(\omega t) & 0 < \theta < \phi_{cri} \quad and \quad \pi - \phi_{cri} < \theta < \pi \\ i_{in2}(\omega t) & \phi_{cri} < \theta < \pi - \phi_{cri} \end{cases},$$

where:

$$i_{in1}(\omega t) = \frac{D_{T1}^2 V_{C1}}{4 L_b f_{sw}} \frac{\sin \omega t}{g - \sin \omega t},$$
$$i_{in2}(\omega t) = \frac{V_{C1}}{16 L_b f_{sw}} \frac{2(D_{T1}^2 + 1)\sin \omega t - g(D_{T1} - 1)^2}{g - \sin \omega t}. \tag{17}$$

Then, the average input power is calculated as:

$$P = \frac{2}{\pi}\left[\int_0^{\phi_{cri}} v_{in}(\omega t) i_{in\_1}(\omega t) d\omega t + \int_{\phi_{cri}}^{\pi/2} v_{in}(\omega t) i_{in\_2}(\omega t) d\omega t\right],$$

$$P = \frac{V_{pk} V_{C1}}{\pi L_b f_{sw}}\left[\int_0^{\phi_{cri}} \frac{D_{T1}^2 \sin^2 \omega t}{2(g - 2\sin \omega t)} d\omega t + \int_{\phi_{cri}}^{\pi/2} \frac{2(D_{T1}^2 + 1)\sin^2 \omega t - g(D_{T1} - 1)^2 \sin \omega t}{8(g - \sin \omega t)} d\omega t\right]. \tag{18}$$

The PF is calculated as:

$$PF = \frac{P}{S},$$

where the per-phase apparent power is equals to $V_{rms}I_{rms}$. Then, the PF is expressed as:

$$PF = \frac{2}{\sqrt{\pi}} \frac{\int_0^{\phi_{cri}} \frac{D_{T1}^2 \sin^2 \omega t}{g - 2\sin \omega t} d\omega t + \int_{\phi_{cri}}^{\pi/2} \frac{2(D_{T1}^2 + 1)\sin^2 \omega t - g(D_{T1} - 1)^2 \sin \omega t}{4(g - \sin \omega t)} d\omega t}{\sqrt{\int_0^{\phi_{cri}} \left(\frac{D_{T1}^2 \sin \omega t}{g - 2\sin \omega t}\right)^2 d\omega t + \int_{\phi_{cri}}^{\pi/2} \left(\frac{2(D_{T1}^2 + 1)\sin \omega t - g(D_{T1} - 1)^2}{4(g - \sin \omega t)}\right)^2 d\omega t}}. \tag{19}$$

Fig. 5 presents the plot of the calculated and measured power factors as function of D_{T1} when g changes from 2 to 3. It is possible to see that the power factor is close to 1 when the dc link voltage V_{dc} is much higher than the peak of the input ac voltage and a large D_{T1}. Also for small duty cycles, and thus small input power, the power factor is low. It can be seen from (16) that the selection of g limits the minimum D_{T1} that the converter can operate:

$$D_{T1} > 1 - \frac{2}{g}. \tag{20}$$

IEEE Std. 519-2014 [26] limits the harmonic distortion of the current that a load takes from the utility grid at the point of common coupling (PCC). Table II in [26] sets the limits for the individual harmonic current distortion and the total demand distortion (TDD) in percent of fundamental current up to the 50th harmonic of the line frequency. Fig. 6 shows the measured input current for different values of D_{T1} where it can be seen that the current gets distorted when D_{T1} is small. TDD is evaluated at the maximum demand load current; when the SST operates under this condition the PF is larger than 0.99 and the ITHD is smaller than 14% as shown in Fig. 7. According to Table II of [26] this SST may be used at locations where I_{sc} / I_L is larger than 50. The high frequency components related to the switching frequency are considered electromagnetic interference (EMI) and should be attenuated by an EMI filter determined according IEC 61000 standard.

E. SST Topology Design Equations

1) Boost inductor design

The boost inductor is designed to operate in the DCM, which intrinsically provides a high power factor (as long as the dc bus voltage is kept larger than twice the peak of the line voltage [22]) since the instantaneous peak inductor current is proportional to the input voltage. The positive cycle of the input ac voltage and DCM operation are considered for the analysis. The inductor L_b is sized considering the worst case scenario, which occurs when the input voltage and output power are maximum and the maximum duty cycle is applied. Therefore, the case where the primary duty cycle is maximum ($D_{T1} = 1$) is considered so the zero state is eliminated and the inductor will be discharged only through the series combination of C_1 and C_2.

Thus, the dc bus capacitors are both charged to V_{pk} and the critical condition for the inductor to operate in DCM is:

$$L_{b\_critic} = \frac{V_{pk}^2}{8 f_{sw} P_{o\_max}}. \tag{21}$$

where P_{o_max} is the maximum output power. Then, L_b should be chosen to be less than L_{b_critic}.

2) HV dc link capacitor voltage

The gain from the ac input voltage to the HV dc bus capacitors can be approximated by considering that the ac input voltage has an imperceptible variation with respect to the high switching frequency and the values of C_1 and C_2 are large enough to sustain the voltage level at which they are charged. In that case, the steady-state analysis gives the following relationship where D_{T1} is the duty cycle defined as the time interval where S_1 and S_2 are on (S_3 and S_4 if $v_{in}(t)$ is in its negative cycle) and $D_{Tx}T_{hs}$ is the time that it takes for the boost

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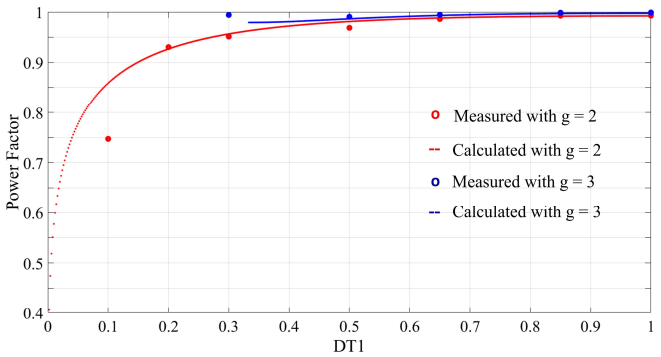

Fig. 5. Measured and calculated input power factor as function of the duty cycle D_{T1} and for different values of g.

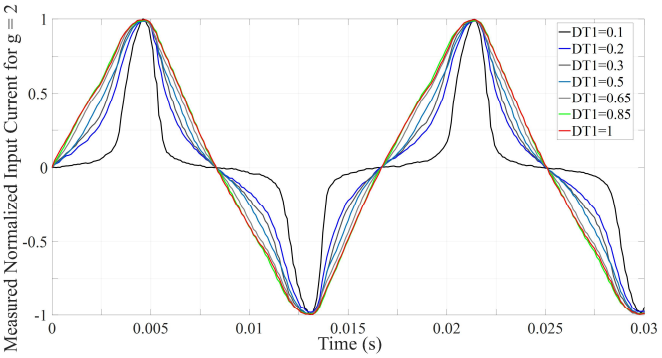

Fig. 6. Input current as function of the duty cycle D_{T1} when g equals 2.

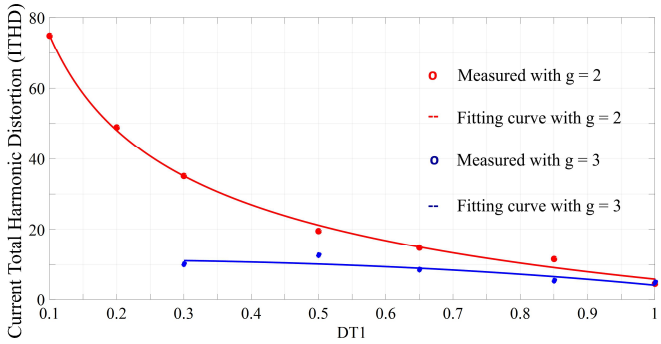

Fig. 7. Input current as function of the duty cycle D_{T1} when g equals 2.

inductor current to reach zero when S_3 and S_4 are on (S_1 and S_2 if $v_{in}(t)$ is in its negative cycle).

$$\frac{V_C}{V_{pk}} = \frac{1/2 + D_{Tx}}{1/2 - D_{T1} + 2D_{Tx}}. \tag{22}$$

From (22), the capacitor C_1 and C_2 voltage levels are at least V_{pk} when D_{Tx} equals D_{T1}. Then, $V_{dc} = V_{C1} + V_{C2} \geq 2V_{pk}$.

3) Minimum and maximum input power

g and the minimum D_{T1} are selected (see Fig. 5, 6 and 7) for the situation that determines the minimum input power for the converter to operate at DCM, based on the desired operating input power factor and current harmonic distortion. The minimum input power for the converter is derived from the calculation of the boost inductor energy over half of the fundamental-frequency period. The energy stored in the inductor at each switching interval depends on the peak inductor current which is a function of the input voltage at each switching interval and the on time. Therefore, the instantaneous peak inductor current is equal to:

$$I_{Lb}(k) = \frac{v_{in}(kT_{sw} + D_{T1}T_{hs})D_{T1}T_{hs}}{L_b}, \tag{23}$$

where $v_{in}(kT_{sw} + D_{T1}T_{hs}) = V_{pk}\sin((2\pi / T_s)(kT_{sw} + D_{T1}T_{hs}))$ and k an integer indicating the number of switching cycles that have occurred since the zero crossover point of the input voltage.

Then, the energy at each time instant is expressed as:

$$E_k = \frac{1}{2}\frac{(D_{T1}T_{hs})^2}{L_b} V_{pk}^2 \sin^2\left(\frac{2\pi}{T_s}(kT_{sw} + D_{T1}T_{hs})\right). \tag{24}$$

The total energy during half cycle of the grid voltage is equal to the summation of the energies over half a period:

$$E_{half\_cycle} = \sum_{k=0}^{T_s/2T_{sw}} \frac{(D_{T1}T_{hs}V_{pk})^2}{2L_b}\sin^2\left(\frac{2\pi}{T_s}(kT_{sw} + D_{T1}T_{hs})\right), \tag{25.a}$$

which becomes:

$$E_{half\_cycle} = \frac{(D_{T1}T_{hs}V_{pk})^2 A}{4L_b}, \tag{25.b}$$

where:

$$A = \left[\frac{T_s}{2T_{sw}} - \frac{\cos(\pi(1+4D_{T1}T_{hs}/T_s))\sin(\pi(1+2T_{sw}/T_s))}{\sin(2\pi T_{sw}/T_s)}\right]. \tag{25.c}$$

Then, the minimum input power can be calculated by dividing (25.b) by half of the input-voltage fundamental period:

$$P_{in\_min} = \frac{(D_{T1}T_{hs}V_{pk})^2}{2T_s L_b} A, \tag{26}$$

where T_s is the line period.

The maximum input power can be derived from (18) by inserting $D_{T1} = 1$, which determines $\phi_{cri} = 0$. Under those conditions, the maximum input power is approximated as:

$$\begin{aligned} P_{in\_max} &= \frac{V_{pk}V_C}{2\pi L_b f_{sw}}\left[\int_0^{\pi/2} \frac{\sin^2\omega t}{g - \sin\omega t} d\omega t\right] \\ &\cong \frac{V_{pk}V_C}{2\pi L_b f_{sw}}(35.29e^{-2.691g} + 1.153e^{-0.3885g}). \end{aligned} \tag{27}$$

4) Output power and voltage

The output power of the converter is calculated by integrating over half the switching period the product of the primary current i_p and the primary voltage v_p:

$$\begin{aligned} P_{out\_max} &= \frac{2}{T_{sw}}\int_0^{T_{sw}/2} v_p(t) i_p(t) dt \\ &= \frac{V_C n V_o}{4 f_{sw} L_{lk}}\left(D_{T1} + D_{T2} + 2D_{T3} - \frac{D_{T1}^2}{2} - \frac{D_{T2}^2}{2} - 2D_{T3}^2 - 1\right). \end{aligned} \tag{28}$$

It can be seen that the maximum power transferred occurs when $D_{T1} = D_{T2} = 1$ and the phase-shift $D_{T3} = 0.5$.

The output voltage is found by expressing the output power

as a function of the output voltage and the resistive load:

$$V_o = \frac{V_C n R_o}{4 f_{sw} L_{lk}} \left(D_{T1} + D_{T2} + 2D_{T3} - \frac{D_{T1}^2}{2} - \frac{D_{T2}^2}{2} - 2D_{T3}^2 - 1 \right), \tag{29}$$

where R_o corresponds to the load resistance.

III. Optimal Selection of Duty Cycles and Phase-Shift for Soft-Switching and Control

In this section, the optimal selection of the duty cycles and the phase-shift for the proposed converter is presented. From (26), it is clear that the input power depends on the primary side duty cycle D_{T1} while the transferred power (28) is governed by D_{T1}, D_{T2} and D_{T3}. However, D_{T3} has more of an effect in (28) than D_{T1} or D_{T2}.Therefore, D_{T1} is used to control the dc bus voltage V_{dc} controlling the input power while D_{T3} is selected to control the output voltage V_o controlling the transferred power. The selection of the secondary side duty cycles is discussed later in this section.

A. Mode Constraints

Different modes of operation arise depending if the duty cycles of the primary and secondary side voltages have partial overlaps, no overlaps or full overlaps. The mode of operation represented in Fig. 2 with partially overlapping voltage waveforms is selected because it is capable of transferring the maximum power with soft-switching operation for all devices. The restrictions that need to apply to stay in the mode shown in Fig. 2 are:

$$D_{T3} \le \frac{D_{T1}}{2} + \frac{D_{T2}}{2}, \tag{30}$$

$$D_{T2} \ge 2\left(1 - \frac{D_{T1}}{2} - D_{T3}\right), \tag{31}$$

$$D_{T2} \ge 1 - D_{T1}. \tag{32}$$

B. Soft-Switching Analysis

At turn on, zero voltage switching (ZVS) is achieved for all operating intervals if the polarity of the transformer current is correct. Moreover, the capacitors connected in parallel with the switches enable quasi-ZCS at turn off. Only the transition between *intervals 3* and *4* is analyzed in this paper because similar processes occur for other devices. The conditions for the transformer current that allows soft-switching operation in all devices are presented in Table II.

Initially, S_1 and S_2 conduct i_{Lb} and i_p (see Fig. 3(c)). The capacitor C_{ss} and the parasitic capacitors of S_3 and S_4 are charged up to $V_C = V_{C1} = V_{C2}$. As soon as S_1 turns off, the current that was flowing through S_1 conducts though C_{S1} (turning S_1 off at quasi-ZCS) and charges it. C_{S1} and C_{S4} are connected by C_{SS} whose voltage is almost constant due to its quite large value (1μF), in comparison with C_{S1} and C_{S2} (Fig. 8). Therefore, the voltage across C_{S1} increases as much as the voltage across C_{S4} decreases. When C_{S1} reaches the level of V_{C1}, V_{CS4} reaches zero and D_3 starts conducting (Fig. 3(d)). Therefore, S_4 can be turned on at any time during *interval 5* at ZVS. It is important to note that the main condition for S_1 to turn off at quasi-ZCS and S_4 to turn on at ZVS is positive transformer current. Then, in Fig. 2 at t_3, I_3 must also be positive to allow the soft-switching operation to happen.

TABLE II
ZVS and Quasi-ZCS Conditions

Before the Starting of:	Condition
$t_0 - t_1$	$I_0 < 0$
$t_1 - t_2$	$I_1 > 0$
$t_2 - t_3$	$I_2 > 0$
$t_3 - t_4$	$I_3 > 0$
$t_4 - t_5$	$I_4 > 0$
$t_5 - t_6$	$I_5 < 0$
$t_6 - t_7$	$I_6 < 0$
$t_7 - t_8$	$I_7 < 0$

From Fig. 2, if the constraints $I_o < 0$ and $I_1 > 0$ are met and the converter is operating in buck mode ($0 < m < 1$), then the next constrains $I_2 > 0$ and $I_3 > 0$ are also going to be satisfied because the transformer current will have a positive slope. Therefore, the only soft-switching conditions that need to be considered while operating with $m < 1$ are $I_0 < 0$ and $I_1 > 0$, which gives the following soft-switching restrictions:

$$D_{T1} \ge \frac{2(1 - D_{T3})}{1 + 1/m}, \tag{33}$$

$$D_{T2} \ge \frac{2(1 - D_{T3})}{1 + m}. \tag{34}$$

From (33) and (34) it is clear that for buck mode operation $D_{T2} \ge D_{T1}$. Then, the secondary side duty cycle is chosen to be equal to $D_{T2} = D_{T1}/m$. Fig. 9 presents the implemented control scheme. The PI controller implemented to control the dc bus voltage V_{dc} was designed to be 10 times slower than the one to control the output voltage V_o.

IV. Design Procedure and Example

A. Specifications

The input voltage is defined to be 120 Vrms, the rated output power 500 W, the output voltage is 48 Vdc and the system was designed to operate at an arbitrary switching frequency of 20 kHz.

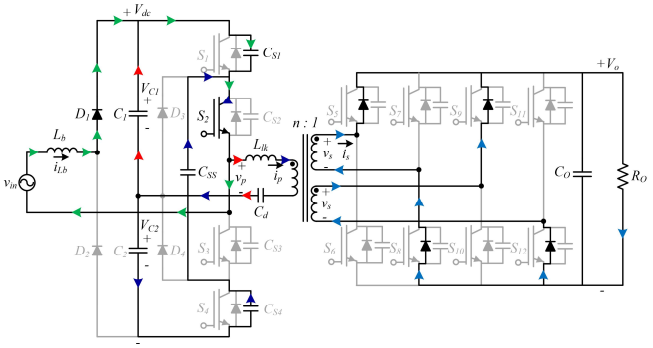

Fig. 8. Equivalent circuits for the transition from *interval 3* [$t_2 - t_3$] to *interval 4* [$t_3 - t_4$].

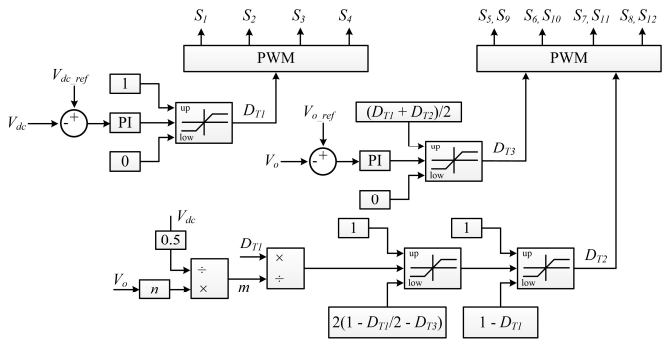

Fig. 9. Implemented control scheme for the new boost SST topology.

B. Number of Series Connected Modules and Intermediate Bus Voltage

The intermediate dc bus voltage is selected to be 400 Vdc, so $g = 400/120\sqrt{2} = 2.35$. According to Fig. 5, g could have been chosen larger, e.g. $g = 3$ to achieve a larger PF; however, this requires a larger dc bus voltage, which would have impacted in the isolation and size of some components. The number of cascaded modules N_m is selected to be 1.

C. Operating Range for D_{T1}

Based on (20), the operating range of D_{T1} is defined as: $0.1489 < D_{T1} < 1$.

D. Total and per Module Bus Voltage ($V_{dc(total)}$ and V_{dc})

$$V_{dc(total)} = 120\sqrt{2}g = 400\,\text{V},$$

$$V_{dc} = \frac{V_{dc(total)}}{N_m} = 400\,\text{V}.$$

E. Voltage Rating of the Capacitors C_1 and C_2, Primary Side Devices S_1, S_2, S_3, and S_4, Front End Diodes D_1 and D_2 and Three-Level Bridge Diodes D_3 and D_4

$$V_{C1}, V_{C2} > \frac{V_{bus(total)}}{2N_m} = 200\,\text{V},$$

$$V_{D1}, V_{D2} > \frac{V_{bus(total)}}{N_m} = 400\,\text{V},$$

$$V_{S1}, V_{S2}, V_{S3}, V_{S4} > V_{C1} = 200\,\text{V},$$

$$V_{D3}, V_{D4} > V_{C1} = 200\,\text{V}.$$

F. Boost Inductor Design

From (21), the maximum boost inductor value is obtained as: $L_b < L_{b\_critic} = 360$ µH. The exact value is obtained from (27) as $L_b = 284$ µH.

G. Transformer Design

For buck mode of operation $m < 1$:

Selecting $m = 0.8$, the turns ratio of the transformer is calculated as:

TABLE III
EXPERIMENTAL PROTOTYPE AND SPECIFICATIONS

Front-End Stage	
Si Diode	RURG5060_F085 $V_R = 600$ V, $I_D = 50$ A, $V_{FM} = 1.4$ V
$C_1 = C_2$	470 µF
DC-AC Three-Level Stage	
Si MOSFET	AOK60N30L $BV_{DSS} = 300$ V, $I_D = 40$ A, $R_{DS(ON)} = 0.056\ \Omega$
SiC Diode	GP2D020A060B $V_R = 600$ V, $I_D = 31$ A, $V_{FM} = 2$ V
C_d	1 µF
AC-DC Stage	
Si MOSFET	RFP4310ZPBF $BV_{DSS} = 100$ V, $I_D = 95$ A, $R_{DS(ON)} = 6$ mΩ
C_o	3900 µF
HF-XFMR	
Power Rating	2 kVA
Voltage Ratio	35/9 (two secondary windings)
Fundamental Frequency	20 kHz
Optimum Flux Density	0.24 T
Leakage Inductance	0.5 mH
Core Material	Amorphous, Metglas® 2605SA1, AMCC-50
Wire	259/36 served Litz wire

$$n = \frac{mV_C}{V_o} = 2.39\,.$$

The leakage inductance is designed from the transfer power equation (28) for maximum power transmission conditions $D_{T1} = 1$, $D_{T2} = 1$ and $D_{T3} = 0.5$:

$$P = \frac{2}{T_{sw}} \int_0^{T_{sw}/2} v_p(t) i_p(t) dt = \frac{V_C n V_o}{8 f_{sw} L_{lk}}\,.$$

Then, the leakage inductance is obtained as:

$$L_{lk} < \frac{V_C n V_o}{8 f_{sw} P_{in}} = 285.9\,\mu\text{H}.$$

H. Current Rating of the Switching Devices

Evaluating the equations from Table I, the current rating of the devices can be obtained.

V. EXPERIMENTAL RESULTS

To validate the functionality of the boost-based topology, a scaled-down version of the converter presented in Fig. 1 is prototyped and tested for different load conditions. The system comprises four stages: A front-end ac-dc stage with two 600 V/50 A Si diodes, a three-level dc-ac stage with 300 V/40 A, Si MOSFETs, a HF-XFMR and a four-leg ac-dc full-bridge converter with 100 V/95 A, Si MOSFETs. The maximum boost inductance to operate in DCM is calculated as 0.36 mH using (21). The transformer leakage inductance is set to 0.285 mH and the transformer efficiency is 98% and optimum flux density B_{opt} is approximately 0.24 T. The specifications of the topology's stages are listed in Table III.

The measured transformer input and output voltages and current flowing through the leakage reactance are illustrated in Figs. 10 – 12 for 100%, 80% and 40% rated power. The

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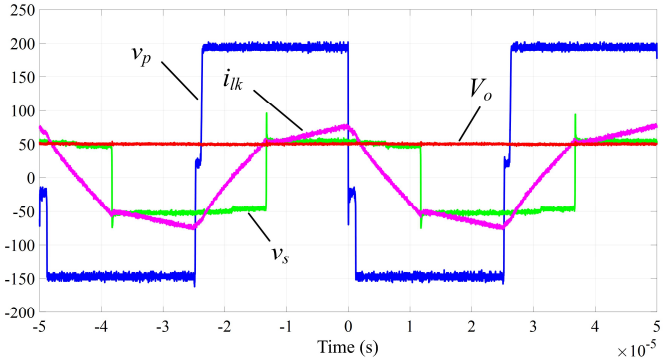

Fig. 10. Transformer primary voltage (blue) and secondary voltage (green), primary current (pink) and output voltage (red) at rated power.

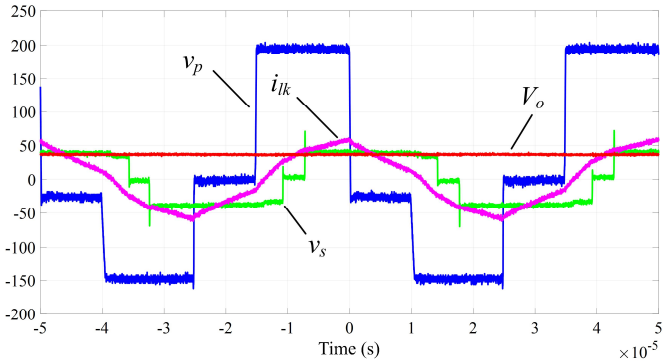

Fig. 11. Transformer primary voltage (blue) and secondary voltage (green), primary current (pink) and output voltage(red) at 80% of rated power.

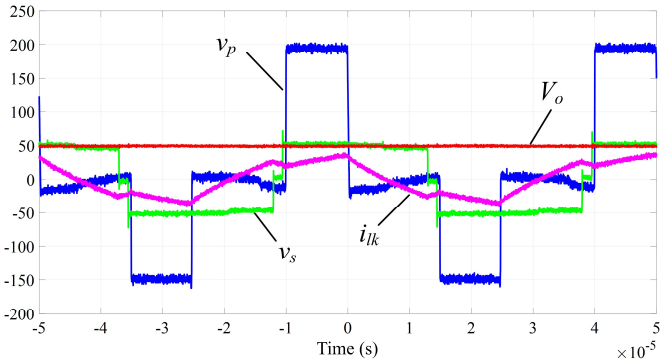

Fig. 12. Transformer primary voltage (blue) and secondary voltage (green), primary current (pink) and output voltage (red) at 40% of rated power.

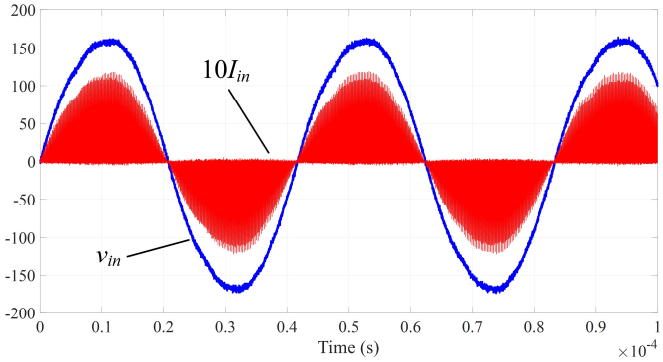

Fig. 13. Converter input voltage (blue) and input current (red).

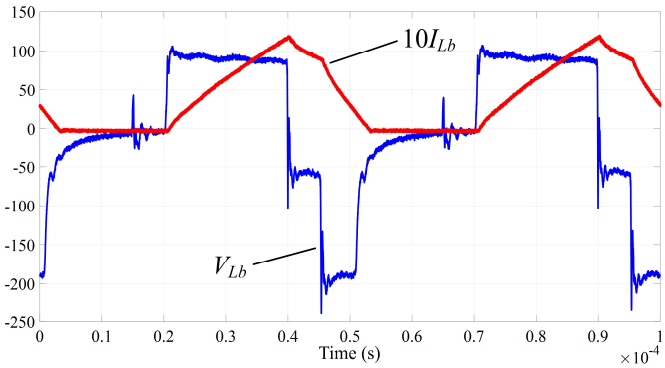

Fig. 14. Boost inductor voltage (blue) and current (red).

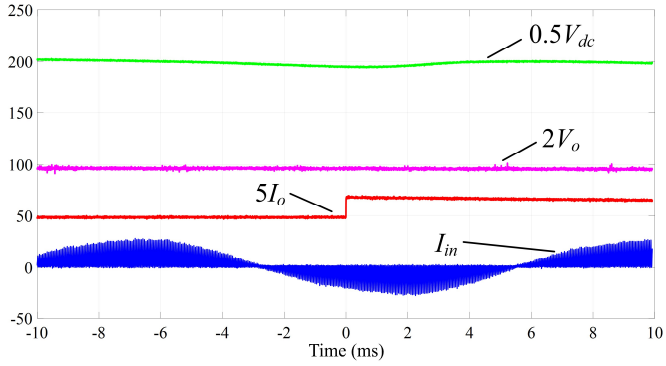

Fig. 15. DC bus voltage (green), output voltage (pink), output current (red) and input current (blue).

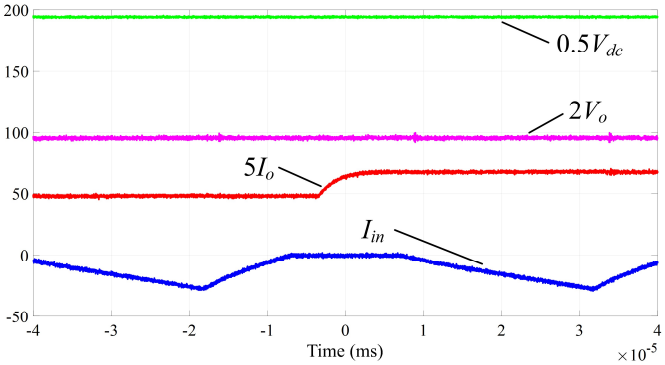

Fig. 16. Zoomed versions of the dc bus voltage (green), output voltage (pink), output current (red) and input current (blue).

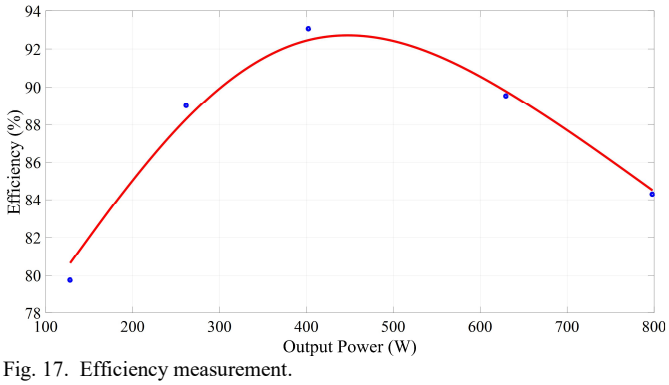

Fig. 17. Efficiency measurement.

waveforms shapes are the result of commutation scheme presented in Fig. 2. The input and output voltages were maintained at 400 Vdc and 48 Vdc, respectively. However, there was a voltage imbalance between the two capacitors in the primary dc bus (see the blue waveforms). Blocking capacitor C_d was connected in series with the HF-XFMR to

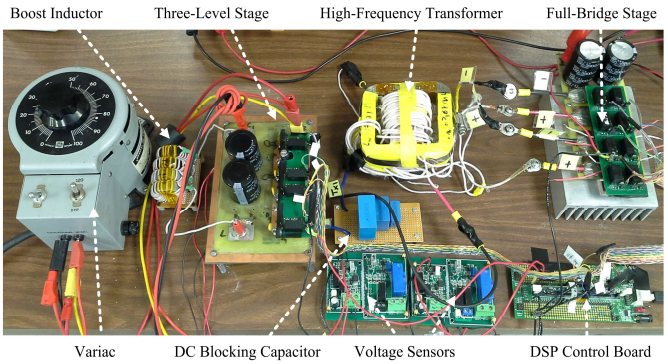

Fig. 18. Photo of the experimental setup.

avoid any dc offset caused by delays and dead times. Based on the analysis done in Section III and using Table II, all requirements for soft-switching are accomplished for the power conditions shown in Figs. 10 and 11. Therefore, all the transitions are done in a lossless manner. This does not happen for all transitions of the primary side switches at low load conditions (see Fig. 12). The reason is due to the fact that the imposed soft-switching conditions interfere with voltage control requirements. At low power conditions, the controller needs to make D_{T1} and D_{T3} smaller, which forces D_{T2} to grow larger as required by the constraint in (31), resulting in a further increase of the output voltage. Therefore, a relaxation of the constraints for soft-switching is needed to control the output voltage while losing the soft-switching operation for some devices.

The boost inductor current and ac input voltage are presented in Fig. 13. The input current operates in DCM and has two negative slopes when decreasing in value. A zoomed version of the boost inductor current and voltage are shown in Fig. 14.

The dynamic response of the proposed topology under a sudden 42% increase of load condition is shown in Figs. 15 and 16. It can be seen that the output voltage remains almost constant while the voltage sag at the dc link voltage is about 5% of the rated dc link voltage. Fig. 17 presents the efficiency measurements of the proposed prototype and Fig. 18 illustrates the experimental setup used to test the prototype.

VI. Conclusions

A new unidirectional-power-flow SST topology with reduced number of switches in the HV-side was presented. The proposed converter has four diodes and four IGBTs (operating under ZVS) in the transformer HV side, whereas the traditional bidirectional-power-flow SST based-DAB topology has eight IGBTs operating under hard switching.

The HV-side capacitor voltage is controlled using the primary side duty cycle D_{T1} and transferred power can be controlled by adjusting the fundamental phase-shift between the primary and secondary voltage waveforms, D_{T3}. Constraints were placed upon the secondary duty cycle D_{T2} to ensure the mode of operation and thus ZVS for all of the switches. In addition to this, the HF-XFMR two-winding configuration and the four-leg full-bridge converter, helps reduce current stresses on the LV power semiconductor devices.

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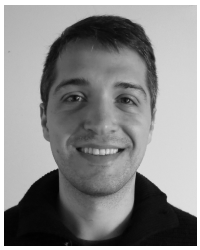

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