Control System to Balance Internal Currents of a Multilevel Current-Source Inverter

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***Abstract*—Multilevel Current Source Inverters (MCSI) have proved to be a high performance option for industrial applications due to reliability, fault tolerant capabilities, quasi soft switching and the use of lower filter capacitor values. One of its major challenges is to balance the internal currents that feed each module. Imbalances could be caused by manufacturing deviations of the reactive components, temperature drift or aging, nonlinear loads and modulation errors, among others. Using the well-known Phase Shift Carrier Sinusoidal Pulse Width Modulation (PSC-SPWM), a slight change in the amplitude of the carrier signals produces a variation in the average value of the internal currents. In this paper, we introduce a control strategy to balance the current of the inductors and its implementation in a prototype. Simulation and experimental results at different operating conditions show a robust behavior of the control system along with a low distortion in the output voltages and currents of the converter.**

***Index Terms*—Multilevel Current Source Inverter; FPGA Control; Inductor Current Balance.**

I. Introduction

OVER the past years, multilevel power converters have been used in several applications such as battery chargers [1], power factor correctors [2] and active filters [3], motor control [4]–[6] and interface with alternative energy sources [7]–[9], among many others [10]. They can be implemented both as a Multilevel Voltage Source Inverter (MVSI) or Multilevel Current Source Inverter (MCSI).

MCSIs particularly offer a great number of advantages such as a fast dynamic response, fault tolerant capabilities and the reduction of high frequency electrical disturbances in the load. Furthermore, they have less current stress in the switches and an increased Medium Time Between Failures (MTBF) because of the higher reliability of inductors compared to MVSI capacitors [11]–[13]. Their main disadvantages are the required reverse voltage blocking capabilities of the switches, and the size and weight of the internal inductors. These disadvantages could be partially solved by using wide band gap devices such as SiC and GaN that allows to increase the frequency without affecting efficiency [14]–[16].

The topology called "Single Rating Inductor MCSI" in [17] consists of n identical Current Source Inverter (CSI) modules. Each module is composed of two balance inductors and six switches that have reverse voltage blocking characteristics. One of the modulation techniques commonly used in these kind of converters is the well-known Phase Shift Carrier Sinusoidal Pulse Width Modulation (PSC-SPWM) [18], [19], which is based on the comparison of three sinusoidal references with a triangular carrier. Each module applies the SPWM technique taking into account that the phase of the carrier must be equally shifted by $\frac{360}{n}$ degrees.

The MCSI presents $2n+1$ current levels since each module has the capability of injecting $\pm\frac{1}{n}$ of the main DC current. The whole operation of the MCSI assumes that each module have the same current value. However, unmatched components, unequal ON-state characteristics of the semiconductor devices, modulation errors and nonlinear loads could cause an imbalance in these currents, so a balancing method must be implemented.

Even though the issue related to the voltage imbalance in the capacitors of different MVSI topologies has been widely studied in the literature [20]–[24], only a few techniques applied to the MCSI topology could be found [25]–[28].

The methods proposed in [25] and [26] deal with a 5-level MCSI and they are not easily extended to more levels. In [25] the balance of the internal currents is achieved by choosing the proper redundant vector in the Space Vector Modulation (SVM). In [26] a complex logic is used to modify the PSC-SPWM in order to balance the current of the two modules. Extra hardware is introduced in [27] to balance the currents in a 5-level single phase MCSI. Two methods based on the PSC-SPWM were proposed in [28]. A slight change either in the amplitude or the phase of the triangular carriers causes a change in the internal currents that could be used to generate a balanced operating point. The controller action slightly affects the output current THD without affecting the switching losses.

In this paper, the mathematical model of the MCSI and a current balance control algorithm is developed. A new version of the algorithm proposed in [28] is presented, analyzed and verified with an MCSI prototype under different experimental conditions. The proposed controller is based on controlling the average value between the upper and lower currents of

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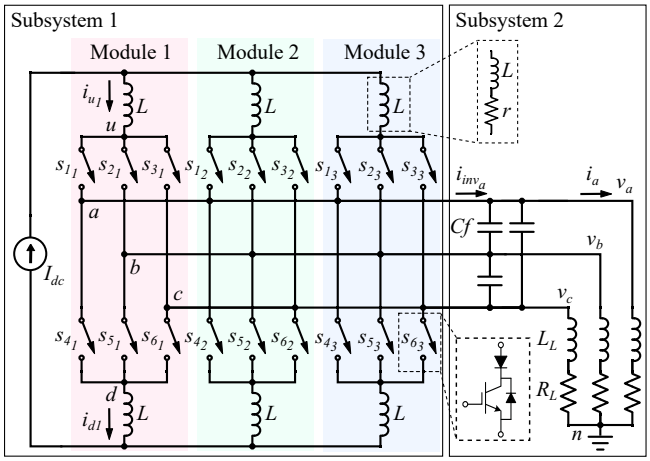

Fig. 1. MCSI Topology

each CSI module. The controller, along with the SPWM, are implemented in a Field Programmable Gate Array (FPGA) as in [29], allowing high speed data processing, variable bit accuracy, fault tolerant architectures and easily scalable design [30], [31]. In addition to these qualities, one of the most powerful advantages of an FPGA is the ability to compute all the converter control blocks in parallel, saving time and increasing reliability. In order to be scalable and comparable to the experimental results, simulation models in this paper consider the internal logic timing, the switches behavior, the parameters of the experimental setup, and the saturation limits of the actual control system.

In detail, this paper is organized as follows: in Section II, the system is described and its mathematical model is obtained. Then, the modulator and proposed controller are shown. Section III presents and analyzes the simulation results. Experimental results are shown in Section IV. Finally, in Section V some conclusions are drawn.

II. System Description

The system is composed of an MCSI, a DC current source, custom acquisition boards used to measure the internal currents of the MCSI, an FPGA, filtering capacitors and the load.

A. MCSI Topology

Fig. 1 shows the schematics of the MCSI. It consists of three Current Source Inverters (CSI) modules in parallel with a maximum of 7 different output current levels. Two inductors are required in each module to balance its current value. All the balance inductors should be identical and should carry the same average current, simplifying the design of the inverter. Each module is composed of six reverse blocking switches that could be implemented with integrated gate commutated thyristors (IGCT), reverse blocking insulated gate bipolar transistors (RB-IGBT) or insulated gate bipolar transistors (IGBT) with a series diode to block the reverse current and voltage, among others. In order to filter and improve the current and voltage waveforms at the load, a three phase capacitor of low capacitance value is placed at the output of the MCSI.

B. Mathematical Model

At any given time, each module of the multilevel inverter must grant a current path so one upper switch and one lower switch must be conducting. Furthermore, only one of the upper and lower devices must be conducting to ensure that the injected current of the inverter is defined only by the DC current source and the state of the switches. These restrictions can be stated as follows

$$s_{1_y} + s_{2_y} + s_{3_y} = s_{4_y} + s_{5_y} + s_{6_y} = 1 \quad y \in \{1, 2, 3\} \quad (1)$$

Where the last sub index y is the module number, with $s_{1,6_y} = 1$ when the switch is conducting and 0 otherwise. The proposed topology can be modeled as two interconnected subsystems: one involving the MCSI with its current source and other composed of filtering capacitors and a load, which are shown in Fig. 1 as Subsystem 1 and Subsystem 2. Both models have 6 state variables with the output of the first model connected to the input of the second one and vice versa. Applying the Kirchhoff's laws on the topology and rearranging the equations, the space state model of the MCSI is obtained

$$\begin{aligned}
\begin{bmatrix} \dot{i}_{u_1} \\ \dot{i}_{u_2} \\ \dot{i}_{u_3} \end{bmatrix} &= \frac{1}{3\,L}\Gamma \begin{bmatrix} v_{un_1} \\ v_{un_2} \\ v_{un_3} \end{bmatrix} - \frac{r}{L} \begin{bmatrix} i_{u_1} \\ i_{u_2} \\ i_{u_3} \end{bmatrix} + \frac{r}{3\,L} \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} I_{dc} \\
\begin{bmatrix} \dot{i}_{d_1} \\ \dot{i}_{d_2} \\ \dot{i}_{d_3} \end{bmatrix} &= \frac{1}{3\,L}\Gamma \begin{bmatrix} v_{nd_1} \\ v_{nd_2} \\ v_{nd_3} \end{bmatrix} - \frac{r}{L} \begin{bmatrix} i_{d_1} \\ i_{d_2} \\ i_{d_3} \end{bmatrix} + \frac{r}{3\,L} \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} I_{dc}
\end{aligned} \quad (2)$$

where L is the self inductance of each module with an internal resistance r, the matrix Γ is

$$\Gamma = \begin{bmatrix} -2 & 1 & 1 \\ 1 & -2 & 1 \\ 1 & 1 & -2 \end{bmatrix} \quad (3)$$

and

$$\begin{aligned}
\begin{bmatrix} v_{un_1} \\ v_{un_2} \\ v_{un_3} \end{bmatrix} &= \begin{bmatrix} s_{1_1} & s_{2_1} & s_{3_1} \\ s_{1_2} & s_{2_2} & s_{3_2} \\ s_{1_3} & s_{2_3} & s_{3_3} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \\
\begin{bmatrix} v_{nd_1} \\ v_{nd_2} \\ v_{nd_3} \end{bmatrix} &= - \begin{bmatrix} s_{4_1} & s_{5_1} & s_{6_1} \\ s_{4_2} & s_{5_2} & s_{6_2} \\ s_{4_3} & s_{5_3} & s_{6_3} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}
\end{aligned} \quad (4)$$

in which s_{x_y} are the state of the switches, x is the switch number and y is the module number. The output current of the inverter is stated as follows

$$\begin{aligned}
\begin{bmatrix} i_{inv_a} \\ i_{inv_b} \\ i_{inv_c} \end{bmatrix} = &\begin{bmatrix} s_{1_1} & s_{1_2} & s_{1_3} \\ s_{2_1} & s_{2_2} & s_{2_3} \\ s_{3_1} & s_{3_2} & s_{3_3} \end{bmatrix} \begin{bmatrix} i_{u_1} \\ i_{u_2} \\ i_{u_3} \end{bmatrix} - \\
&\begin{bmatrix} s_{4_1} & s_{4_2} & s_{4_3} \\ s_{5_1} & s_{5_2} & s_{5_3} \\ s_{6_1} & s_{6_2} & s_{6_3} \end{bmatrix} \begin{bmatrix} i_{d_1} \\ i_{d_2} \\ i_{d_3} \end{bmatrix}
\end{aligned} \quad (5)$$

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The second subsystem that includes the load and the filter capacitors is modeled by

$$\begin{bmatrix} \dot{v_a} \\ \dot{v_b} \\ \dot{v_c} \\ \dot{i_a} \\ \dot{i_b} \\ \dot{i_c} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & a & 0 & 0 \\ 0 & 0 & 0 & 0 & a & 0 \\ 0 & 0 & 0 & 0 & 0 & a \\ b & 0 & 0 & c & 0 & 0 \\ 0 & b & 0 & 0 & c & 0 \\ 0 & 0 & b & 0 & 0 & c \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \\ i_a \\ i_b \\ i_c \end{bmatrix} - a \begin{bmatrix} i_{inv_a} \\ i_{inv_b} \\ i_{inv_c} \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (6)$$

$$a = -\frac{1}{3\,C_f} \qquad b = \frac{1}{L_L} \qquad c = -\frac{R_L}{L_L}$$

Where C_F represents the filter capacitance, R_L the load resistance and L_L load inductance. The interconnection between the two subsystems can be seen in (4) and (5). As shown in (2), the dynamics of the upper and lower currents, i_{u_y} and i_{d_y}, are different because they depend on the state of the switches and load voltages. Thus, a classic controller would have taken into account the values of the six internal currents in order to balance them. However, balancing the average value between the upper and lower currents for each module is a simpler approach that produces similar results. The average currents are defined by

$$\bar{i_y} = \frac{i_{u_y} + i_{d_y}}{2} \qquad y \in \{1, 2, 3\} \quad (7)$$

As this paper is focused on balancing the average currents, the resulting dynamics to control can be expressed as

$$\begin{bmatrix} \dot{\bar{i}}_1 \\ \dot{\bar{i}}_2 \\ \dot{\bar{i}}_3 \end{bmatrix} = \frac{1}{6\,L} \begin{bmatrix} -2 & 1 & 1 \\ 1 & -2 & 1 \\ 1 & 1 & -2 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} - \frac{r}{L} \begin{bmatrix} \bar{i}_1 \\ \bar{i}_2 \\ \bar{i}_3 \end{bmatrix} + \frac{r}{3\,L} \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} I_{dc} \quad (8)$$

Where the equivalent voltages of each module, v_1, v_2 and v_3 are defined by

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} v_{un_1} \\ v_{un_2} \\ v_{un_3} \end{bmatrix} + \begin{bmatrix} v_{nd_1} \\ v_{nd_2} \\ v_{nd_3} \end{bmatrix} \quad (9)$$

Since $v_{1,2,3}$, in (8), depend on the state of the switches, a variation in the modulation algorithm could be used to produce a change in the average current of all the modules.

C. Modulation

The modulation of the MCSI is performed applying the Phase Shift Carrier Sinusoidal Pulse Width Modulation (PSC-SPWM). It is based on comparing the reference sinusoidal signals with three equally phase-shifted triangular carriers [18]. A block diagram of the modulation stage is presented in Fig. 2, where $f_{ma2,3}$ are the outputs of the controller which is described in the next section. They are equal to 1 when the control is disabled. The implementation of this modulation in a CSI is not as simple as in a VSI since it requires more logic manipulation to generate the desired current levels at the output while ensuring a current path in all the inductors. Since the modulation algorithm is similar for each module, the modulation scheme of the first one is used as an example. The different signals of the modulation process are shown in Fig. 3. First, the current references of the MCSI, I_{A-ref} I_{B-ref} and I_{C-ref} are compared with the triangular carrier as depicted in Fig. 3a. The standard VSI SPWM signals G_{A_1} , G_{B_1} and G_{C_1}, shown in Fig. 3b are generated by the comparators. They are used as inputs of the Look Up Table States (LUT States), as shown in the top part of Fig. 2. The LUT States, shown in Table I, are used to transform the active vectors of a VSI, generated by the SPWM, into equivalent active vectors of a CSI. Zero vectors are considered separately. Since each module can produce a zero current state by turning

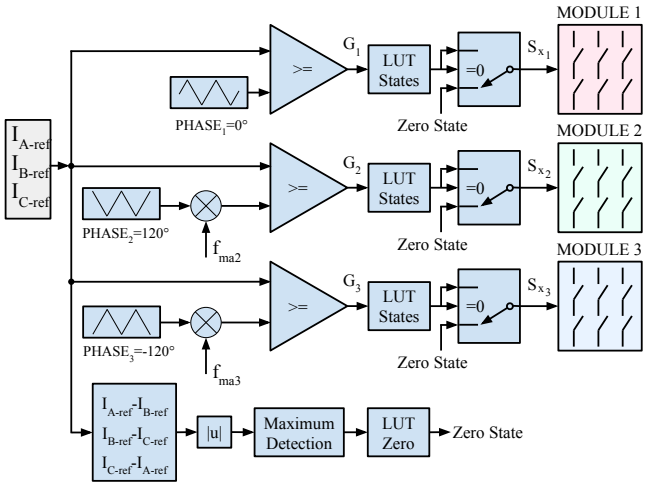

Fig. 2. Modulation Scheme

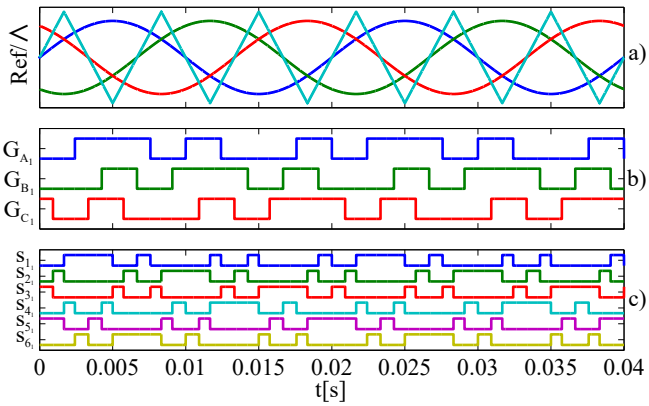

Fig. 3. SPWM Detail of one module

TABLE I
LUT STATES OF MODULE x

Input			Output					
G_{A_x}	G_{B_x}	G_{C_x}	$s1_x$	$s2_x$	$s3_x$	$s4_x$	$s5_x$	$s6_x$
0	0	0	0	0	0	0	0	0
0	0	1	0	0	1	0	1	0
0	1	0	0	1	0	1	0	0
0	1	1	0	0	1	1	0	0
1	0	0	1	0	0	0	0	1
1	0	1	1	0	0	0	1	0
1	1	0	0	1	0	0	0	1
1	1	1	0	0	0	0	0	0

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TABLE II
LUT ZERO, $x = 1, 2, 3$

Maximum value	Output					
	$s1_x$	$s2_x$	$s3_x$	$s4_x$	$s5_x$	$s6_x$
$\lvert I_{A-ref} - I_{B-ref} \rvert$	1	0	0	1	0	0
$\lvert I_{B-ref} - I_{C-ref} \rvert$	0	1	0	0	1	0
$\lvert I_{C-ref} - I_{A-ref} \rvert$	0	0	1	0	0	1

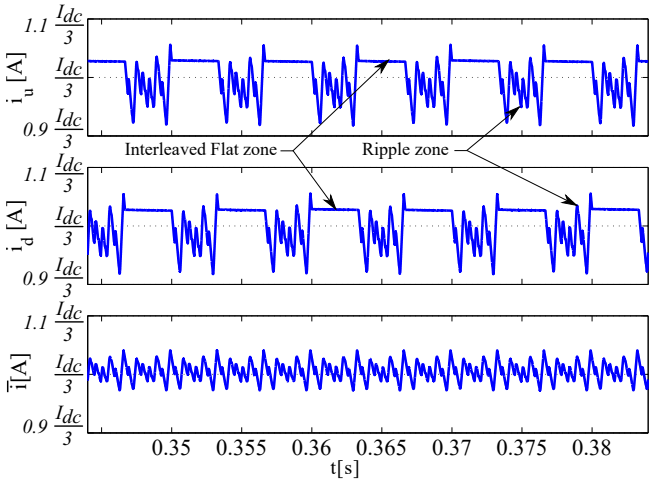

Fig. 4. From top to bottom. First trace: i_u, second trace i_d, and third trace: $\bar{i}$, average current of one module

on both switches in any of its three legs, the CSI has one extra zero state than the VSI. This extra redundancy could be used to reduce the commutation frequency, reduce the power dissipation and increase the efficiency. To select the zero state that meets these goals, first three current differences are calculated and the one that gets the maximum absolute value is related with the optimum zero state. Another look up table (LUT Zero), which is shown in Table II, holds the zero states. Both the output of the LUT States and the LUT Zero are fed into a multiplexer. The outputs of the multiplexer, $s1_1$, $s2_1$, $s3_1$, $s4_1$, $s5_1$ and $s6_1$ are shown in Fig. 3c.

D. Controller

One of the major drawbacks of the multilevel topologies is that the average currents of each module, $\bar{i}_{1,2,3}$, may have different mean values. This could be caused by nonlinear loads, imperfections of the modulation algorithm, unequal ON-state characteristics of the semiconductor devices and component variations. In this section a control algorithm to balance these currents is presented. The control algorithm is based on one proposed in [28], which uses slight changes of the PSC-SPWM carriers. In [28], the amplitudes of the triangular carriers in the modules 2 and 3 are modified, in order to balance the internal currents. The objective of this controller is just to balance only the average between the upper, i_{u_y}, and lower, i_{d_y}, currents of each module. The upper and lower currents of one module, along with their average value are depicted in Fig. 4. It can be noticed that the current waveforms have

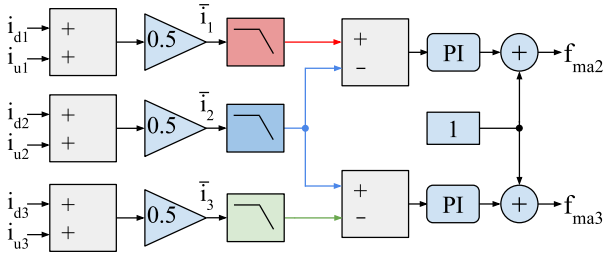

Fig. 5. Proposed current balance controller

two different parts: a flat zone and a ripple zone. The different mean values can be clearly recognized since the constant flat zone of each current is at a different level and depends on the relative phase and the amplitude relation between the carriers and the reference signals, m_a. The average current, defined in (7), has a lower ripple and its mean value could be obtained with a low pass filter. From (4), it can be deduced that a change in the SPWM carriers causes a change in the switch signals and hence, a change in the upper and lower voltages seen by each of the modules v_{un1}, v_{un2}, v_{un3}, v_{nd1}, v_{nd2} and v_{nd3}. Taking into account (9), these voltages are the inputs of the dynamic expressed in (8), which is the state space representation of the average currents, that must be controlled. The overall control algorithm is depicted in Fig. 5. The controller is implemented with two simple Proportional and Integral (PI) controllers. A change in the amplitude of the carrier that is used in the second module produces a variation of $\bar{i}_1$ and $\bar{i}_2$ while changing the amplitude of the third carrier produces a variation of $\bar{i}_2$ and $\bar{i}_3$. Considering this behavior, the error signal for the first PI is implemented by the difference between $\bar{i}_1$ and $\bar{i}_2$ while the error signal for the second one is done by the difference between $\bar{i}_2$ and $\bar{i}_3$. The low pass filter is needed because the main objective is to control the average current on the inductors of the converter and the commutation frequency must be rejected for this purpose. Since the aim of the controller is to introduce a slight change in the carrier amplitudes, a saturation of $\pm 6\%$ of the maximum m_a, is applied to the output of the PI controllers in order to limit their action and its effect over the SPWM signals. Then, the PI outputs are added to 1 to create a scale factor for the amplitude of both carriers. Both f_{ma2} and f_{ma3} signals are fed into the modulation scheme shown in Fig. 2. The frequency of the triangular carriers is not affected as the controller changes only their amplitudes. Therefore, there is no change on the average commutation frequency and hence switching losses are not affected.

III. SIMULATION RESULTS

Extensive simulations were performed using the SimPowerSystem toolbox from MATLAB™/Simulink™ down to switch level. The parameters used in the simulations and experiments are shown in Table III. The chosen bandwidth for the low pass digital filter, which is used to smooth the average of the upper and lower currents of each module, is 155Hz and the modulation index ma is 0.9. The controller is designed in discrete time with a sampling time $T_s = 1\mu s$.

TABLE III
SYSTEM PARAMETERS

Parameter	Value
I_{dc}	$10A$
Line frequency	$50Hz$
Balance inductors (L, r)	$80mH, 0.75\Omega$
Capacitor Filter (C_f)	$4.7\mu F$
Frequency Modulation Index (m_f)	21
Carrier frequency	$1050Hz$
Load (R_L, L_L)	16Ω, $9mH$

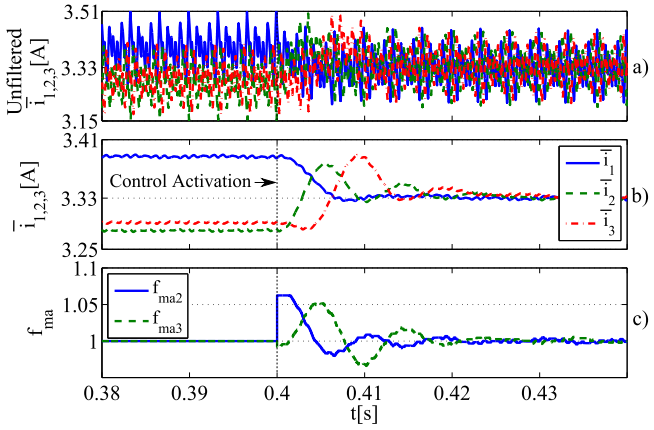

Fig. 6. Simulation of the proposed controller - Internal average currents $\bar{i}_{1,2,3}$, filtered and unfiltered and control output signals f_{ma2} and f_{ma3}

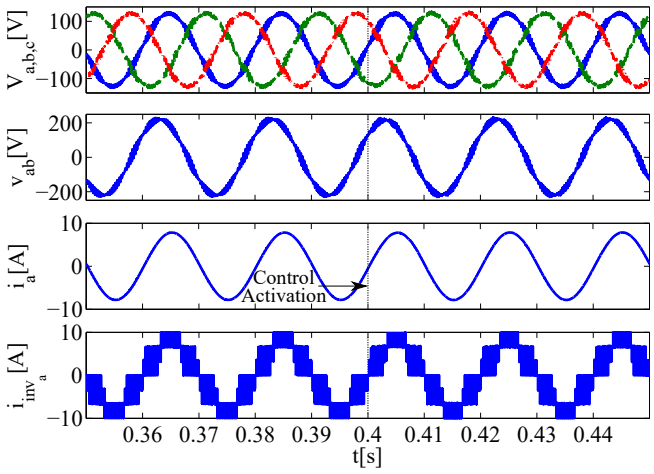

Fig. 7. Simulation of the proposed controller. Phase voltages $v_{a,b,c}$, line voltage v_{ab}, current i_a and the unfiltered output of the inverter i_{inv_a}

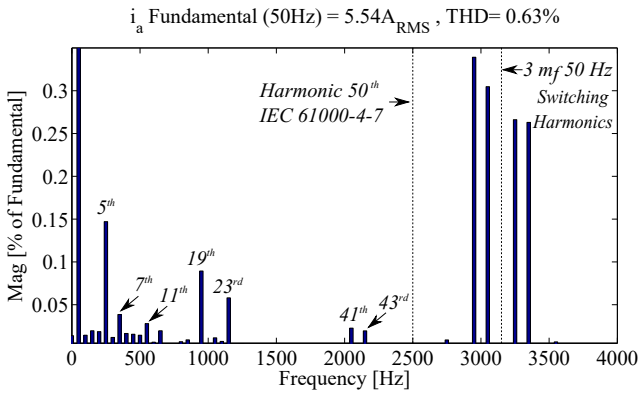

Fig. 8. THD of the simulated output current i_a with the controller enabled

Fig. 6 shows the response of the system before and after the controller is enabled. With the controller disabled, the scale factors remains at 1 and the internal currents have a difference of 100mA. At time $t = 0.4s$ the controller is enabled and the average currents converge to approximately 3.33A in less than 30ms. The filtered average currents $\bar{i}_{1,2,3}$ shown in Fig. 6b are used to feed the digital controllers. The output control signals that modifies the amplitude of the triangular carriers in the modulation block are depicted in Fig. 6c.

Fig. 7 shows the output variables of the system under examination. The output current i_a, shown in the third trace, is the inverter output of the phase a, i_{inv_a}, filtered by the output capacitors. The output variables of the system remain practically unchanged when the control is enabled. The output line voltage v_{ab}, shown in the second trace, is affected mainly by the fifth and higher order harmonics.

As shown in Fig. 8 the output current i_a presents low harmonic distortion and a THD of 0.63% even when the controller is enabled. The main difference with the theoretical spectrum of a discrete time SPWM modulator is the presence of low order harmonics, less than 0.025% of the fundamental current. These low order harmonics are caused by the effects of the quantization in the modulation and control algorithm. The main components of the i_a spectrum are also caused by the fifth harmonic and the switching harmonics. Since the MCSI consists of three identical modules to produce seven levels in the output current, the switching components are three times the commutation frequency of the switches or $3\,m_f\,50$ Hz, where m_f is the frequency modulation index . Hence, the harmonics corresponding to the switching frequency are centered at 3150Hz.

Fig. 9 shows the response of the system under a step down in m_a. At time $t = 0.46s$ it is changed from 0.9 to 0.5 and the controller is able to balance the internal currents with a settling time of less than $40ms$. The change of m_a causes a reduction in the number of levels that the MCSI outputs. It also produces an instant change on the current and voltage at the load. The ripple introduced in the internal average currents during the transient is less than 2.5%.

IV. EXPERIMENTAL RESULTS

A custom acquisition system was designed and developed in order to measure the internal currents of the MCSI. The current is sensed using the ACS714 hall effect sensor, a four channel 12 bit ADC with a Serial Peripheral Interface (SPI) capable of sampling up to 1MSps, digital isolators and LVDS converters to improve the CMRR of the communication with the FPGA [32]. Control algorithms along with the SPWM and support logic are implemented on a Xilinx FPGA, Xilinx Zynq-7000 AP SoC XC7Z020. It uses 1763 LUT (look up tables), 4 digital signal processing (DSP) blocks used as multipliers in PIs, and

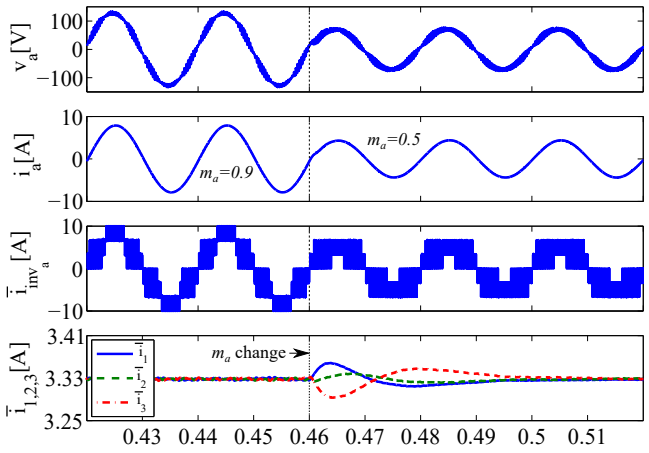

Fig. 9. Simulation of the proposed controller with $m_a = 0.5$, Phase voltage v_a, phase current i_a, unfiltered output of the inverter i_{inv_a} and internal average currents $\bar{i}_{1,2,3}$

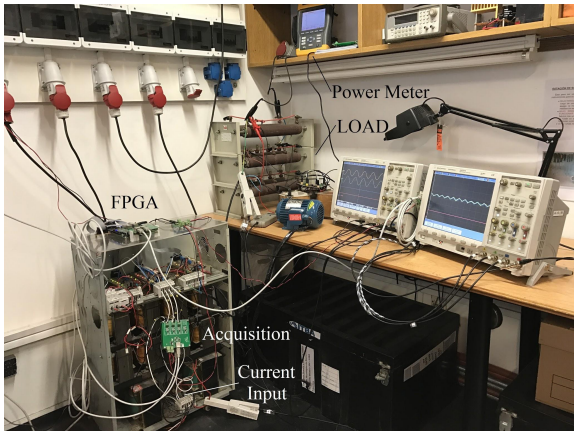

Fig. 10. Experimental Setup

5 Block Random Access Memory (BRAM) which represents less than 4% of the overall capacity. The experimental setup, which is composed of an MCSI, a DC current source, different type of loads, a power meter, acquisition and FPGA boards, is shown in Fig. 10. The parameters of the system are the same used in the previous section.

The internal filtered currents of each module $\bar{i}_{1,2,3}$ are shown in Fig. 11 prior and post controller activation. The ripple is mainly caused by the current source that supplies the MCSI which has a ripple of approximately 2% and the zero state selection of the modulator. When the controller is disabled, the internal currents have a difference of 80mA. After the controller is enabled, the internal currents of each module show the desired response converging to 3.33A in less than 50ms.

In Fig. 12, the controller is enabled and disabled again after 230ms. After being enabled, the currents of each module converge to the same value and when the control is disabled the currents return to their original value with a longer settling time. The longer settling time is caused by the open loop response of the system which depends only on the topology and the system parameters.

Fig. 13 shows the voltage v_a, current i_a and input current

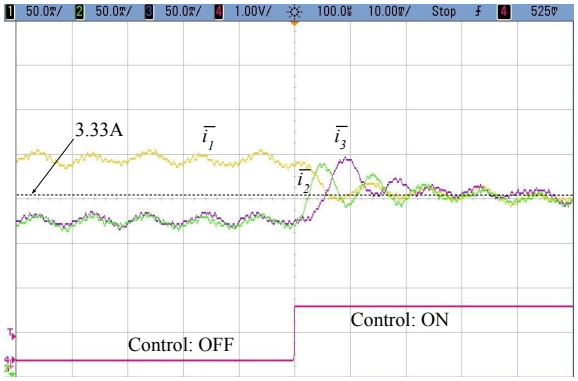

Fig. 11. Internal average currents with and without control. Upper traces: internal average currents $\bar{i}_{1,2,3}$ at a scale of $50mA/div$. Bottom trace: control enable signal

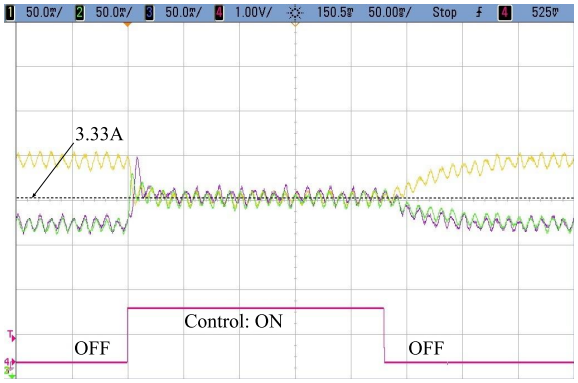

Fig. 12. Step on control activation. Internal average currents with and without control. Upper traces: internal average currents $\bar{i}_{1,2,3}$ at a scale of $50mA/div$. Bottom trace: control enable signal

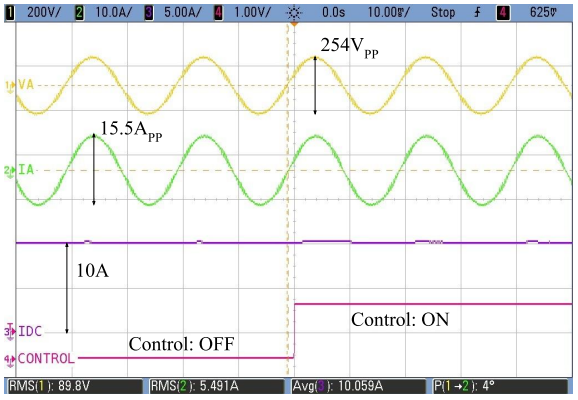

Fig. 13. Traces from top to bottom. First: output voltage v_a [V] at a scale of $200V/div$. Second: output current i_a [A] at a scale of $10A/div$. Third: input current I_{dc} [A] at a scale of $5A/div$. Fourth: control enable signal

i_{dc} along with the control enable signal. Both, v_a and i_a present a low distortion due to the multilevel capabilities of the inverter along with its high equivalent commutation frequency. There are no noticeable differences on the waveforms after the control is enabled.

The variation of the scale factors, $f_{ma2,3}$, after the controller is enabled are shown in Fig. 14. They introduce a slight change in the triangular carriers to perform the balancing of

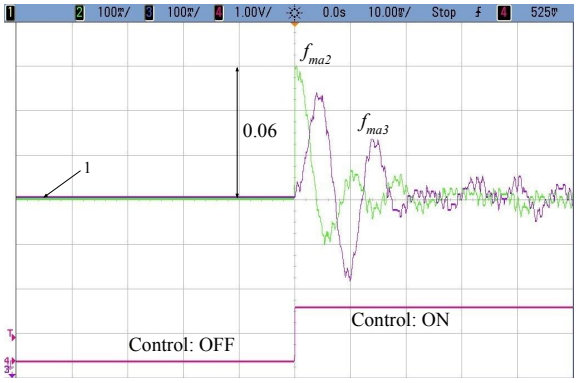

Fig. 14. Controller output signals with and without control. Upper traces: f_{ma2} and f_{ma3} at a scale of $0.02/div$. Bottom trace: control enable signal

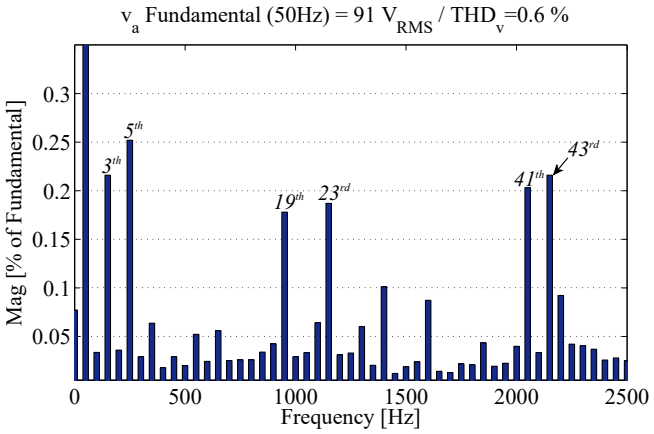

Fig. 15. THD measurement of output voltage v_a with control enabled

the internal currents. A good correlation between simulation and experimental results is observed.

The spectrum of the output waveforms, v_a and i_a are depicted in Fig. 15 and Fig. 16 respectively. The first 50 harmonics were measured using a Fluke 435 Series II Power Quality and Energy Analyzer, according to the IEC 61000-4-7 standard. The main differences with the simulation are the presence of the third harmonic and an increment of 0.1 % in most of the harmonics. The third harmonic is introduced mainly by the ripple of the DC current source. The power differences are due to delays introduced by the semiconductor switches, accuracy and resolution of the power meter, and small errors introduced by the FPGA implementation. The THD of the current is 0.3% when the controller is disabled and increases to 0.4% when enabled. The same behavior is observed for the voltage THD that gets increased to 0.6% when the controller is enabled. Results are very promising since, even when the controller is activated, THD values are below the 3% established by the IEC 61000-4-7 and the IEEE Standard 519.

V. Conclusions

A control technique to ensure the balance of the internal currents on an MCSI is presented. Although the implementation needs the measurement of the internal currents, it requires

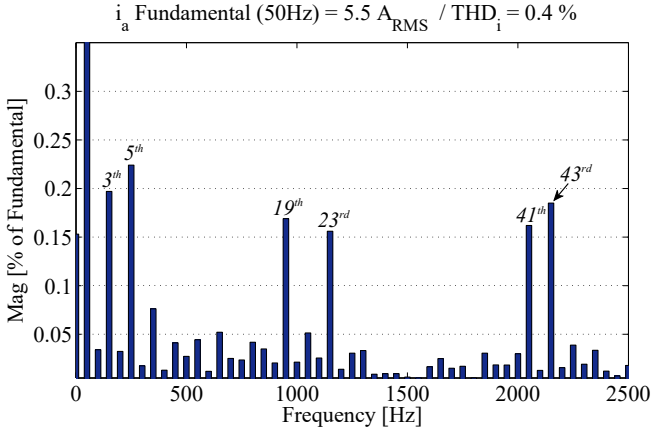

Fig. 16. THD measurement of output current i_a with control enabled

little computational effort, and hence a small area on an FPGA. It also introduces a minimal distortion to the SPWM signals without affecting the switching losses and increasing less than 0.1% the THD at the output of the inverter. The controller has been designed, evaluated through simulations and implemented on a prototype of a 7 level MCSI. Simulation and experimental results show an excellent behavior. This solution can be easily expanded adding only a PI controller for each additional module.

The proposed controller is suitable for industrial converters as it can withstand disturbances and imbalances of the components without affecting the internal currents of the MCSI.

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