Nonvolatile Multilevel Resistive Switching Memory Cell: A Transition Metal Oxide-Based Circuit

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***Abstract*—We study the resistive switching (RS) mechanism as a way to obtain multilevel cell (MLC) memory devices. In an MLC, more than 1 b of information can be stored in each cell. Here, we identify one of the main conceptual difficulties that prevented the implementation of RS-based MLCs. We present a method to overcome these difficulties and to implement a 6-b MLC device with a manganite-based RS device. This is done by precisely setting the remnant resistance of the RS device to an arbitrary value. Our MLC system demonstrates that transition metal oxide nonvolatile memory devices may compete with currently available MLCs.**

***Index Terms*—Multilevel cell (MLC), nonvolatile memory, resistive random access memory (ReRAM), resistive switching (RS).**

I. Introduction

DURING the last decade, the development of nonvolatile electronic memory devices based on the resistive switching (RS) effect in transition metal oxides made a great deal of progress, becoming one of the promising candidates to substitute for the standard technologies in the near future. RS refers to the reversible change of the resistance of nanometer-sized media by the application of electrical pulses [1]–[6].

Manuscript received January 2, 2013; revised July 11, 2013; accepted October 21, 2013. Date of publication December 19, 2013; date of current version January 13, 2014. This work was supported in part by the National Scientific and Technical Research Council (CONICET), by Agencia Nacional de Promoción Científica y Tecnológica (ANPCyT), by Universidad Nacional de San Martín, by E. I. du Pont de Nemours and Company (DuPont), and by Fundación José A. Balseiro Inc. This brief was recommended by Associate Editor H.-J. Yoo.

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Digital Object Identifier 10.1109/TCSII.2013.2290921

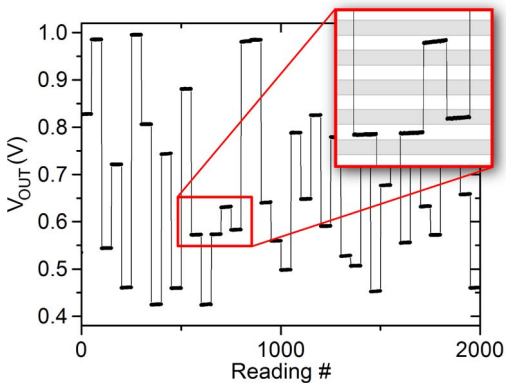

Fig. 1. Experimental results. A random memory level sequence that is stored in the 6-b MLC is shown. The plot presents the memory states during 50 readings (at 10 Hz) for each stored value. For a 6-b MLC, the working memory range is divided into 64 levels (as indicated in the inset).

Although the application for multilevel cell (MLC) memory devices was immediately envisioned after the discovery of the reversible RS effect in transition metal oxides [7]–[11], reports so far chiefly focused on single-level cell (SLC) devices [1], [3]. Unlike SLC memory devices, which can only store 1 b per cell, MLC memory devices may store multiple bits in a single cell [12]. MLCs of up to 4 b (16 levels) are currently available based in both the standard Flash [13] and phase-change [14] technologies.

In an n-bit RS-based MLC memory, one has to encode 2^n memory levels as distinct resistance states. Thus, the 2^n memory states can be identified with each of the consecutive and adjacent resistance "bins" of width $\triangle\mathcal{R} = \mathcal{R}_{i+1} - \mathcal{R}_i$, with $i = 1, 2, \ldots, 2^n$. To store the ith memory state, the device has to be SET to the corresponding bin, i.e., $\mathcal{R}_i < \mathcal{R} < \mathcal{R}_{i+1}$. The requirement of nonvolatility implies that the value should remain within that bin even after the input is disconnected or the memory state is read out. In Fig. 1, we plot the data of a random sequence of stored memory states in our implementation of a 64-level (6-b) MLC. For convenience, resistance levels are translated into voltage levels by a fixed bias current.

The central component of the MLC is an RS device of a resistance $\mathcal{R}$, whose magnitude can be changed by the application of a current pulse $I_{\rm pulse}$. The resistance change depends on $I_{\rm pulse}$ through a highly nontrivial function f; $\triangle\mathcal{R} = f\,(I_{\rm pulse})$. Function f is usually unknown; however, an important general requirement for the nonvolatile memory applications using RS is that $f = 0$ for currents below a given threshold. This allows for sensing (i.e., reading out) a stored memory state, i.e., the so-called remnant resistance $\mathcal{R}_{\rm rem}$, injecting a bias current $|I_0| < |I_{th}|$ without modifying the stored information. Thus, $\mathcal{R}_{\rm rem} \equiv \mathcal{R}(I_0)$, $|I_0| < |I_{th}|$. A two-level memory can

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be simply implemented by strongly pulsing an RS device with opposite polarities and by sensing the corresponding high and low $\mathcal{R}$ states with a weak bias current. However, the previous observation of a current threshold has an important consequence for the implementation of MLC memory devices. In fact, in order to implement an MLC, one should be able to tune the value of $\mathcal{R}_{\rm rem}$ to any desired value. The better the control on this tuning, the better the ability to define the bins, and a larger number of bits could be coded in the MLC. In principle, a perfect knowledge of function f should allow for this, but in practice the function is not known. However, any reasonable form of f would allow tuning of any arbitrary memory state by applying a sequence of pulses of decreasing intensity, following a simple "zero-finding" algorithm, as in a standard control circuit. Nevertheless, the requirement of a threshold current makes it difficult to perform fine tuning, as small corrections beneath $|I_{th}|$ have no effect. In practice, the dead zone that is introduced by relatively large values of $|I_{th}|$ prevents a straightforward implementation of an RS device as MLC memory devices with a large number of levels. In the following, we will demonstrate how this conceptual problem can be overcome and we exhibit the implementation of a 64-level MLC.

II. Implementation

We adopt a manganite-based RS device, which is made by depositing silver contacts on a sintered pellet of $La_{0.325}Pr_{0.3}Ca_{0.375}MnO_3$ (LPCMO) [15]. An RS-device is defined between the pulsed Ag/LPCMO and a second nonpulsed contact. A third electrode (earth) is required in a minimal three-contact configuration setup.

A requirement for our MLC is that the RS device should operate in the bipolar RS mode [1]–[3], i.e., depending on the pulse polarity, the remnant resistance either increases or decreases.

It is now well established that the mechanism behind the bipolar RS is the redistribution of oxygen vacancies within the nanometer-scaled region of the sample that is in contact with the electrodes [2]. In the case of the LPCMO, the oxygen vacancies significantly increase their resistivity because the electrical transport relies on the double-exchange mechanism that is mediated by the oxygen atoms [16].

Pulsing an electrical current through the contact will produce a large electric field at the interface due to the high resistivity of the Ag/LPCMO Schottky barrier. If the pulse is strong enough, it will enable the migration oxygen ions across the barrier, modifying the concentration of vacancies and, hence, changing the interface resistance. The ionic migration always remains near the interface and does not penetrate deep into the bulk, since the much larger conductivity there prevents the development of high electric fields. Thus, the RS effect remains confined to a nanometer-sized region near the interface, as schematically depicted in Fig. 2.

We now introduce the practical implementation of the RS-based MLC that produced the results shown in Fig. 1. We used an Ag/LPCMO interface and off-the-shelf electronic components. The block diagram of the concept is presented in Fig. 3 and the schematics and technical details are included in the Appendix. We envision an implementation of an

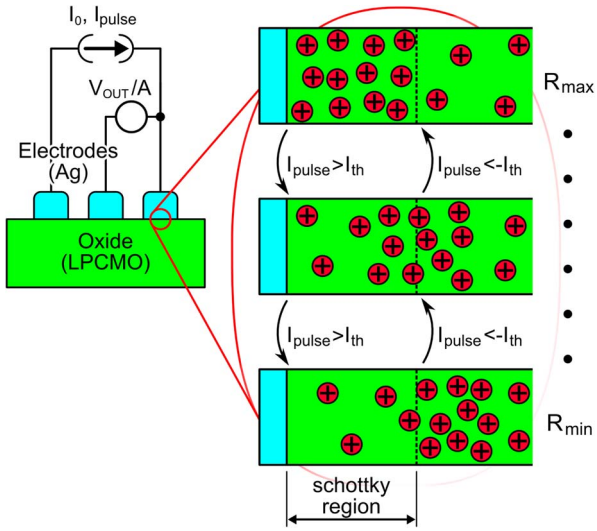

Fig. 2. (Left) Three-contact setup of the RS device. (Right) Schematic representation of the physical mechanism of resistive switching in Ag/LPCMO. The current pulses progressively change the profile of the oxygen vacancies within a nanometer-sized region that is in proximity to the Ag contacts. We define the positive pulses as those flowing from the electrode toward the LPCMO.

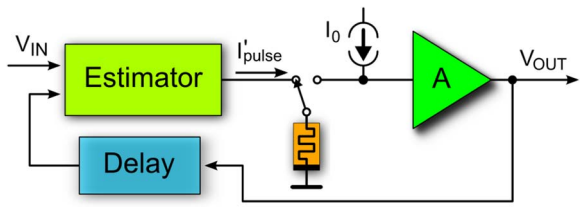

Fig. 3. Block diagram of the implementation. The switch commutes the system between a READ state, in which the resistance of the RS device is sensed with I_0, and a WRITE state, in which current pulses are applied in order to cancel the difference between $V_{\rm IN}$ and $V_{\rm OUT}$. When WR is deactivated, $I_{\rm pulse}$ is forced to zero.

RS-based MLC memory chip where the storage core is a set of several RS units with a single common control circuit. The common control would set each of the individual RS units one at a time, resembling the concept of the refresh logic circuit in the dynamic random access memory devices. In this brief, we demonstrate the implementation of the control circuit with a single RS memory unit.

A key to our MLC implementation is the adoption of a discrete-time algorithm that overcomes the problems discussed earlier [17], and we describe this next. The required memory state $\mathcal{R}_i$ is coded in terms of a $V_{\rm IN}$, whereas $V_{\rm OUT}$ indicates the actual stored value (see Fig. 3). The system iteratively applies the pulses $I_{\rm pulse}$ of a strength that is an estimate of the required value to set the target state $V_{\rm IN}$, eventually converging to it. This discrete-time feedback loop continuously cycles between two stages, i.e., the "probe" and "correct" stages. In the probe stage, the switch connects the RS device to the current source I_0, in order to sense the remnant resistance. In the correct stage, the switch connects the RS device to a pulse generator that applies the corrective pulse $I_{\rm pulse}$ of a strength that is obtained from the difference between the delayed $V_{\rm OUT}$ and target value $V_{\rm IN}$ as

$$I_{\rm pulse}[k] = K_P\, e[k] + K_I \sum_{i=0}^{k} e[i] \qquad (1)$$

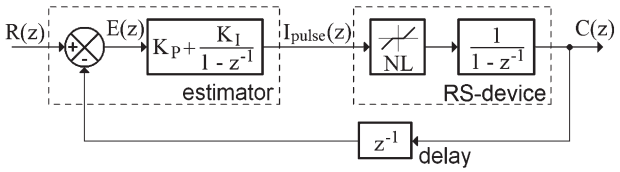

Fig. 4. Discrete-time model. In each cycle, the input signal $R(z)$ is compared with the output signal $C(z)$ after being delayed, generating error signal $E(z)$. Based on this signal, the estimator generates the corrective pulses $I_{\rm pulse}(z)$.

where error signal $e[k]=V_{\rm OUT}[k-1]-V_{\rm IN}[k]$ is the change that is required in the output voltage and $I_{\rm pulse}[k]=I_{\rm pulse}(kf_{\rm CLK}^{-1})$, with $f_{\rm CLK}$ as the frequency of the system clock and k is an integer. K_P and K_I are the generic proportional and integral constants, respectively, with an (A/V) unit, where A and V are the electric current and voltage units, respectively. The first term of the equation represents a proportional estimator. The second term prevents the system from getting stuck in a condition in which $|I_{\rm pulse}| < |I_{th}|$. In fact, for a low $e[k]$, a pulse of strength $K_P\, e[k-1]$ would lie below the threshold, thus not producing any further change in the state of the system. The magnitude of the second term linearly increases in time, thus making $I_{\rm pulse}$ eventually overcome the threshold and correct the output voltage in the desired direction.

Notice that although this approach resembles a standard proportional–integral (PI) control loop with a dead zone, there are substantial differences. First, the remnant resistance reading and the correcting pulse application occur at different times. This requires the addition of the continuously commuting switch. Second, we also needed the introduction of a delay, which is implemented as a sample and hold (S&H) circuit, as required for the feedback path. These differences and the strong nonlinearity in f makes the stability analysis of this approach (which also depends on specific values of K_P and K_I) a significant issue, which we describe in the following.

III. Stability Analysis

A. Discrete-Time Model

The study of the stability of the system is based on the discrete-time model that is presented in Fig. 4. In the z-domain, (1) becomes

$$I_{\rm pulse}(z) = E(z)\left(K_P + \frac{K_I}{1-z^{-1}}\right). \tag{2}$$

The resulting $\mathcal{R}_{\rm rem}$ after these corrective pulses is probed by connecting the RS device to the bias current source I_0, obtaining output signal $c[k]$ ($C(z)$ in the z-domain). In the next cycle, it will be compared with reference input $r[k+1]$, generating error signal $e[k+1]$. This fact implies the one-cycle delay z^{-1}.

Central to the present proposal is the following, which is a discrete-time model for the RS-device:

$$\mathcal{R}_{\rm rem}[k] = R_0 + R_1 \sum_{j=-\infty}^{k} {\rm NL}\left(I_{\rm pulse}[j]\right) \tag{3}$$

where R_0 and R_1, having resistance units, are an offset and a proportionality factor, respectively. NL is a nonlinear function that has to be defined on the basis of the general behavior of an RS device operating in bipolar mode. In this model, $\mathcal{R}_{\rm rem}$ is calculated by integrating the writing pulses after being weighted by the NL function. In this way, we model the possible change of the device resistance after the kth pulse as $\triangle\mathcal{R}_{\rm rem}[k] = \mathcal{R}_{\rm rem}[k] - \mathcal{R}_{\rm rem}[k-1] = R_1{\rm NL}(I_{\rm pulse}[k])$.

A concrete implementation of NL is presented in

$${\rm NL}[k] = \begin{cases} (I_{\rm pulse}[k]+I_{th})\ \frac{1}{A}, & I_{\rm pulse}[k] < -I_{th} \\ 0, & -I_{th} < I_{\rm pulse}[k] < I_{th} \\ (I_{\rm pulse}[k]-I_{th})\ u_1, & I_{\rm pulse}[k] > I_{th}. \end{cases} \tag{4}$$

The unit of u_1 is $(1/A)$. When a negative signal exceeds threshold $I_{\rm pulse}[k] < -I_{th}$, $\mathcal{R}_{\rm rem}$ decreases as a linear function of $I_{\rm pulse}[k]$, with a slope of $1(\Omega/A)$. For a positive signal that is greater than I_{th}, $\mathcal{R}_{\rm rem}$ increases with a slope of $u_1\Omega$. For the sake of the stability analysis, (3) is simplified as

$$c[k] = V \sum_{j=-\infty}^{k} {\rm NL}\left(I_{\rm pulse}[j]\right). \tag{5}$$

In this way, the analysis is not considering any instability when sensing $\mathcal{R}_{\rm rem}$ with I_0. Indeed, our actual implementation did not present any critical issue at this level (see the Appendix). From now on, a unit-step sequence is considered as an input signal [18]. The steady-state error for the system with $K_I = 0$ (just proportional control) and $u_1 = 1A^{-1}$ is $e_s = \lim_{k\to\infty} e[k] = I_{th}/K_P$. Then, the steady-state response is $c_s = 1 - (I_{th}/K_P)$. In fact, Fig. 5(a) shows that the system converges to the required set point only for $I_{th} = 0$. The system arrives to this condition because, when $|e[k]| \le (I_{th}/K_P)$, the excitation of the RS device is $|I[k]| \le I_{th}$, i.e., lower than the minimum current that is required to produce a change in $R_{\rm rem}$. A proportional control that enters into this condition remains there indefinitely. The integral term in (2) that turns the system into a PI control avoids the problem; when continuously integrated, $e[k]$ makes $I_{\rm pulse}[k]$ eventually overcome threshold $|I_{th}|$. [See Fig. 5(b) and (c).]

B. Analysis Without NL

We begin by considering the simplified situation in which the stability is analyzed by removing the nonlinearities that are introduced by NL$[k]$ ($u_1 = 1A^{-1}$, and $I_{th} = 0$). The transfer function of the system is $(C(z))/(R(z)) = (K_P + K_I - K_P\, z^{-1})/(1 + (K_P + K_I - 2)\, z^{-1} + (1 - K_P)\, z^{-2})$. For $K_I = 0.25\ (A/V)$ (the typical value), the system is critically damped when $K_P = 0.75\ (A/V)$ and it remains stable for $K_P < 1.875\ (A/V)$. Increasing K_I moves the location of the poles following $|z| = 1$, arriving to $z = -1$ when $K_I = 4\ (A/V)$, in which the system becomes unstable for any K_P [see Fig. 5(m)].

C. Analysis With NL

Although the introduction of nonlinearities in (4) does not allow for the analytical study of the system, as in the previous section, its response might be numerically simulated. In fact, simulations were performed in the k-space by solving (5) after substituting $I_{\rm pulse}[k]$ [see (1)] and NL$[k]$ [see (4)]. For the computation of $e[k]$, we assigned $V_{\rm OUT}[k] = c[k]$ and the unitary step function at the input (i.e., $V_{\rm IN}[k \ge 0] = 1$ V).

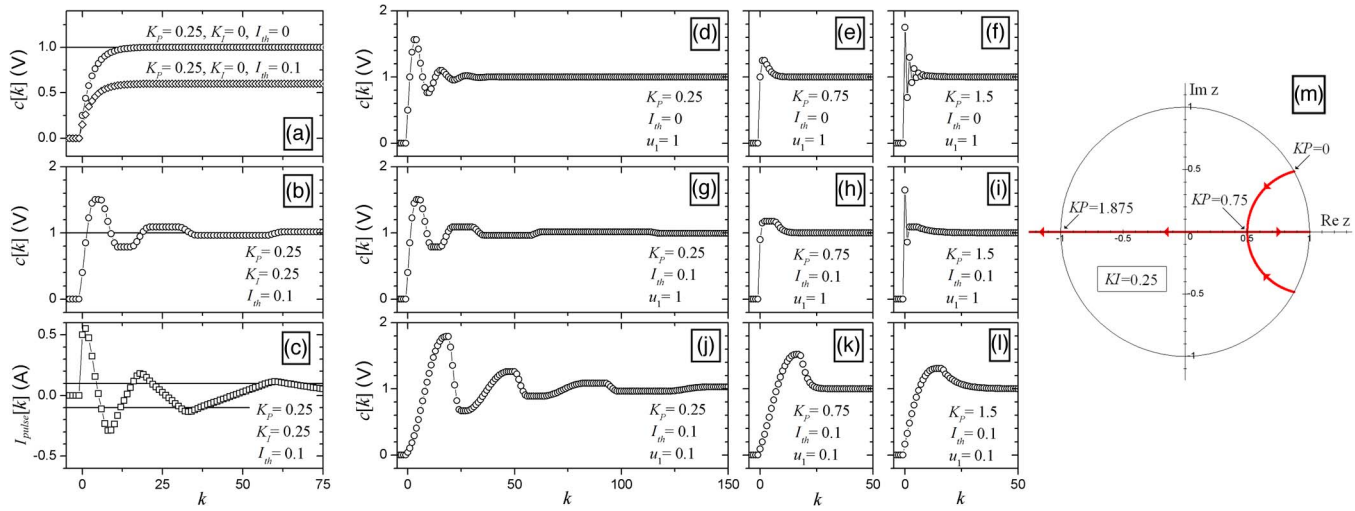

Fig. 5. Simulated output $c[k]$ of the system upon a unitary-step input for (a) proportional control and (b) PI control loop. (c) Excitation $I_{\text{pulse}}[k]$ applied to the RS device model that corresponds to (b). $c[k]$ does not change when $|I_{\text{pulse}}[k]| \leq 0.1$ A. $u_1 = 1A^{-1}$ in all these plots. (d)–(l) present the different conditions for nonzero K_P (indicated in the panels) and $K_I = 0.25$. (m) Root locus for the system without NL. K_I and K_P are indicated in (A/V) units, and I_{th} is indicated in amperes.

Fig. 5(d)–(f) shows this simulated response of the system for three sets $\{K_P,\ K_I\}$, corresponding to the representative position of the poles of the equivalent system without nonlinearities.

Fig. 5(g)–(i) shows the effect of introducing threshold $I_{th} \neq 0$ for the same set $\{K_P,\ K_I\}$. The system response is qualitatively the same with the addition of periods, in which $c[k]$ is "frozen" because $|I_{pulse}[k]| \leq I_{th}$, whereas the integral term is growing. Fig. 5(j)–(l) shows the effect of further introducing asymmetry into the nonlinear function $u_1 \neq 1A^{-1}$. The effect that this nonlinearity introduces when $u_1 < 1A^{-1}$ is equivalent to reducing the gain of the system for $I_{\text{pulse}}[k] > 0$ [see (4)]. In fact, Fig. 5(j) shows a clear difference between the system speed when $c[k]$ is increasing compared with the speed when $c[k]$ is decreasing. The case for $u_1 > 1A^{-1}$ is equivalent to a case in which $u_1 \to u_1^{-1}$ and $K_P \to K_P\, u_1^{-1}$.

Simulations also show a change in the stability limit, as reported in

I_{th} (A)	u_1 $(\frac{1}{A})$	stability limit $(K_I = 0.25)$
0	1	$K_P = 1.875$
0.1	1	$K_P = 1.969$
0.1	0.1	$K_P = 11.1181$

In summary, the simulations show that the system stability is not compromised after the introduction of nonlinearities, although in some conditions the system might require a considerably higher number of cycles to stabilize.

IV. Results

Two tests were conducted to evaluate the performance of the MLC memory. Experimental results for the memory retention test are presented in Fig. 6. We emphasize that the relatively slow operation speed of our MLC memory would be dramatically improved with device miniaturization and integration. For simplicity, we sampled a random subset of 16 out of 64 different voltages that are uniformly distributed along the operative range [see Fig. 6(a)]. Each WRITE (WR) and READ (RD) cycle had a duration of 13 s. In the first 5 s, the WR signal was active and a memory value was SET. After a memory value was SET, we observed a small relaxation of V_{OUT}, with a time constant

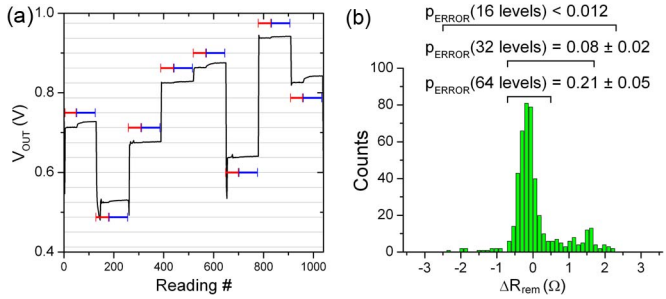

Fig. 6. Retentivity of the LPCMO-based MLC. (a) V_{OUT} is continuously sampled at ten readings per second. During the readings indicated by the red bars, the signal WR was active; the output value accurately follows the sequence of input values that is randomly chosen on the grid. During the readings indicated by the blue bars, no pulses were applied to the RS device, resulting in a drift. (b) Histogram of the last read value of the memory in each cycle (i.e., the last value of the blue sections). The horizontal bars denote the ΔR intervals corresponding to the 16-level, 32-level, and 64-level devices. The location of the bars are chosen to minimize the error probability (i.e., the area of the histogram outside the interval).

of $\tau \sim 1.6$ s. The value of V_{OUT} essentially remained stable afterward. Thus, for the sake of performing a large number of measurements, we only monitored the memory retentivity during the five time constants (i.e., 8 s) that immediately followed the SET. Within that period, the WR signal was inactive, and the memory state that is stored in V_{OUT} was probed every 0.1 s (i.e., the memory was read out 80 times).

In Fig. 6(b), we present the histogram of the distribution of observed errors in the reading of a given stored memory value. The observed values correspond to the remnant resistance of the memory cell after reading it 80 times at a rate of 10 Hz, following the SET. The histogram is constructed from a sequence of 460 memory state recordings.

The finite dispersion of the histogram is the main limitation for implementing a high number of memory levels. To easily visualize the retentivity performance of the memory for increasing the number of levels, we indicate the resistance interval $\Delta R\ (= \Delta V/I_0)$ that corresponds to having a 16, 32, and 64 MLC memory (i.e., 4, 5, and 6 b, respectively) with horizontal bars. The probability of error in storing a memory state corresponds to the area of the histogram that lies outside

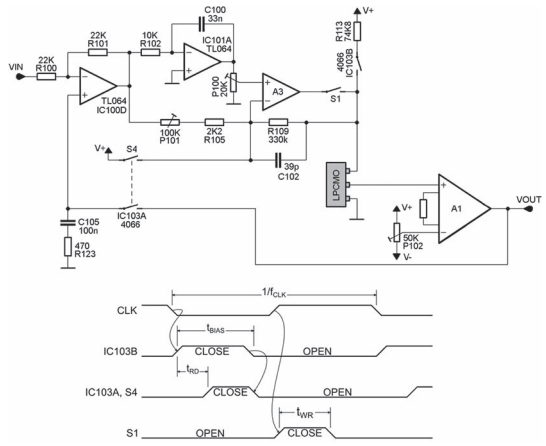

Fig. 7. Simplified circuit of the proposed implementation with its corresponding timing diagram. In this proof-of-concept implementation, $f_{\rm CLK} = 33$ Hz, $t_{\rm BIAS} = 1.7$ ms, $t_{\rm RD} = 0.25$ ms, and $t_{\rm WR} = 120$ μs.

the resistance interval that is normalized to the total area. With a confidence level of 95%, the probability that the MLC fails to retain a stored state is 0.21 ± 0.05, for a 64-level system (6-b MLC). This error probability rapidly improves as the number of levels is decreased, being < 0.012 for a 16-level MLC.

The previous data on the performance of the memory can also be expressed in terms of bit error rates (BERs). In our MLC, we find that a BER ≤ 0.006 for the 16-level system, a BER ≤ 0.07 for the 32-level system, and a BER ≤ 0.1 for the 64-level system. The lower error probabilities for bits than for levels reflect the fact that, typically, the error corresponds to the memory level drifting to an immediate neighbor level (which often shares a large number of bits).

V. Conclusion

In conclusion, we have introduced a feedback algorithm to precisely set the remnant resistance of an RS device to an arbitrary desired value within the device working range. This overcomes the conceptual problem of fine tuning a resistance value in nonvolatile RS devices for MLC applications due to the presence of a threshold current behavior. The feedback configuration is intrinsically time discrete, since it is based on READ/WRITE sequences. The overhead in the writing time that is introduced in this feedback system may be a limitation for its utilization as a primary memory in a computer system, but it can easily compete with the actual speed of current mass storage devices (Flash memory devices). The applicability of the concept in implementing an n-bit MLC memory was successfully demonstrated for $n = 4$, 5, and 6, with an LPCMO-based circuit, which clearly illustrates the critical tradeoff between the BER, the number of memory levels, and the (power and area) overhead of the control circuitry.

Appendix
Schematic and Technical Details of the Circuit

Fig. 7 shows a simplified circuit of our implementation. The "estimator" circuit (see Figs. 3 and 4) is implemented by IC100D, IC101A, and the high-current buffer A3 (and associated components). It compares the output of the S&H against the input signal divided by 2 and then computes the PI function. K_P and K_I are set using of P101 and P100, respectively.

During the correct state, corrective pulses are applied to the RS devices (the LPCMO) by closing S1 during $t_{\rm WR} = 120$ μs. C102 and R109 introduce a time constant of $\sim$13 μs, reducing the rise time of the pulses in order to avoid overshoots. In the probe state, IC103B closes first, and $t_{\rm RD} = 0.25$ ms after, IC103A closes. Moreover, S4 clamps the inverting input of A3 to $\sim$V+. The timing of the circuit is generated by a timing circuit based on the master clock CLK (see Fig. 7). Current $I_0 \approx ((\mathrm{V}+)/(\mathrm{R113}\|\mathrm{R109})) \approx 120$ μA flows through the LPCMO ($\mathrm{V}+ = 7.5$ V, $\mathrm{V}- = -7.5$ V). The voltage drop at the switching interface of the RS device (ranging from 20 to 50 mV) is amplified by the instrumentation amplifier A1 (gain = 21), eventually setting the voltage at the output of the S&H. Both the interfaces of the RS device behave complementary to each other (i.e., when one interface reduces its resistance, the other increases [2]) and then the total drop across the device is $\sim$70 mV and is quite insensitive to the state and, therefore, I_0.

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