Digital Control for a Multiple-Stage Pulsed Current Source

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***Abstract*—Multiple-stage converters are composed of a set of structures with different voltage, current and switching frequency capabilities. In particular, in applications like particle accelerator beam deflection and focusing, the requirement is high-current high-precision current pulses generation. In order to satisfy the specifications of this application, a novel multiple-stage converter topology was proposed and presented in a previous work. However, said proposal should be complemented with a control system to perform the control of each structure, manage its global interconnection and execute the regulation loops. This work describes the implementation of the digital control developed for the proposed converter. Experimental results are presented by applying the proposed control to a prototype.**

***Index Terms*—Digital control, power electronics, pulsed power converter.**

I. Introduction

PARTICLE accelerators applied to high-energy physics and clinical treatment use high-current pulsed converters to supply an inductive load made up of different types of magnets to produce a high-magnetic field that has to be constant throughout the beam length [1]–[3]. For these applications, the key aspects of these converters are current stability and precision during flat top. Current rise and fall times are not critical; yet they should be reduced so as to decrease the output Root Mean Square (RMS) current value and minimize the loss in the magnet load and its associated cooling.

Even though, for many years, the solution offered for these pulsed converters has been the use of a capacitor discharge topology [4]–[7], certain drawbacks in this system (low flexibility and high RMS load current value) created the need of a new development based on switching converters. Moreover, a trapezoidal waveform is the best solution when it comes to reducing the RMS current in the load. This current waveform involves the application of a high voltage (with reverse polarity) during rise and fall times, which allows to reduce the duration of these stages (Fig. 1). Besides, during flat top a high-precision high-dynamic current control is required which implies switching the power semiconductors at high-frequency. These requirements (high-voltage, high-current, and high-frequency) cannot be fulfilled by conventional converters and current semiconductor devices [8]–[11].

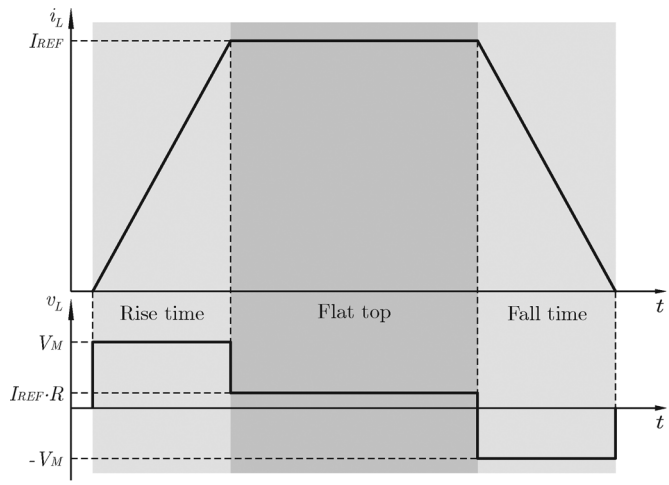

Fig. 1. Trapezoidal load current waveform and corresponding applied voltage.

In order to overcome this technological limitation, a novel converter topology for high-current and high-precision current sources was proposed by [12] and later improved by [13]. The power converter, denoted as a multiple-stage converter, is based on the use of different structures, each one specific for a particular operation range in terms of voltage, current, and switching frequency. These structures are connected during one or more stages of the generated waveform to accomplish the specific requirements corresponding to each stage. The control system associated to this converter must meet hard requirements. It must perform the individual control of each structure, manage the global interconnection of the several structures, and execute the regulation loops assuring minimum duration and amplitude transient response in the load current and high-precision in the flat top. Additionally, it must calculate the initialization parameters before each pulse, manage the peripheral communication and carry out communication with a more hierarchical supervision and command system, among other tasks.

Although there are many powerful digital platforms able to perform the control of multiple-stage converters, the concurrent stages management, peripheral attention and high-speed

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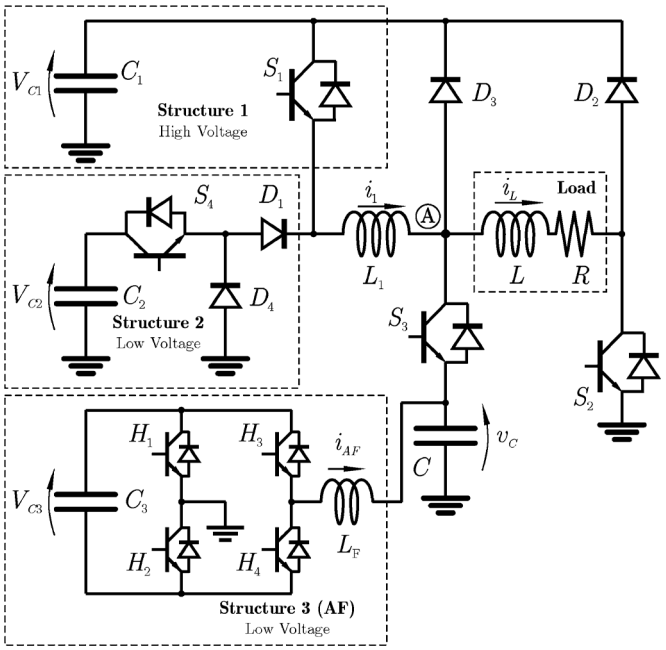


Fig. 2. Simplified scheme of the proposed topology.

calculations require the utilization of a Field Programmable Gate Array (FPGA). The use of this technology to develop and improve digital control systems is known [14]–[16] and has been well exemplified in papers like [17]–[20]. In this paper, an FPGA-based digital control for the multiple-stage converter proposed in [13] is presented. The next sections introduce the multiple-stage converter basics and highlight the most relevant aspects of the proposed control that enable to achieve the stringent requirements of the above mentioned applications. The experimental results obtained with a prototype that emulates the full scale features validate the control system implementation.

II. Power Source Description

This section describes the operating principle of the topology presented in [13] to better understand the different tasks to be performed by the control system. Fig. 2 provides the general scheme of the converter which is based on three structures. The aim is to use structure 1 (High-Voltage and High-Current) during rise and fall times, structure 2 (Low-Voltage and High-Current) to control the flat top mean current with moderate precision, and structure 3 (Low-Voltage and Current) to control the load current with the required precision.

The operational principle of this topology is summarized as follows.

— **Rise time**: During this stage, only structure 1 is activated, which initiates the charge of L_1 and L through the high-voltage source V_{C1}. This condition is obtained by means of S_1 and S_2 turned on and S_3 and S_4 turned off. Besides, the use of D_1 is needed to provide structure 2 high-voltage isolation. If the load resistance is considered negligible, the required voltage V_{C1} to reach the flat top current I_{REF} in a rise time T_R is given by (1).

$$V_{C1} = I_{\mathrm{REF}} \frac{L + L_1}{T_R}. \tag{1}$$

— **Flat top**: When currents $i_L = i_1$ reach the reference value I_{REF}, structure 1 is disconnected and structures 2 and 3 are connected by means of S_1 turning off and S_3 turning on.

Structure 2 is a one quadrant inverter composed by C_2, S_4, D_4, and D_1 which is used to control the i_1 so as to provide the mean load current. This system is modeled as a current generator called $GI1$ which operates in PWM mode with a commutation frequency f_{I1}. It is common knowledge that an increase of this frequency causes a decrease of the ripple current. However, due to the technological limitations of semiconductor devices, f_{I1} switching frequency is limited by the current and the voltage maximum ratings. Therefore, since structure 2 must handle the high load current, a medium S_4 switching frequency must be adopted. As a consequence, a peak to peak ripple current ΔI_1, much higher than the required one, is obtained.

Structure 3 is a full bridge inverter (composed by C_3, H_1, H_2, H_3, and H_4) connected in series with the inductance L_F. This structure, named Active Filter (AF), must operate at a switching frequency f_{IF} higher than f_{I1} in order to cancel ΔI_1. A current ripple ΔI_F is generated.

In order to ensure the operation of the current controls, the voltages V_{C2} and V_{C3} must be higher than $I_{\mathrm{REF}} \cdot R$.

The turning on of S_3 allows the connection of the active filter and the capacitor C to the node Ⓐ. C is connected in parallel to structure 3 to avoid overvoltage in this node.

— **Fall time**: To decrease the load current, all switches are turned off. The energy stored in the load and inductor L_1 returns to the capacitor bank C_1 through D_1, D_2, and D_4. The current difference between i_{L1} and i_L when S_3 is turned off flows through D_3 or the antiparallel diode of S_3 depending on the current flow direction.

Fig. 3 illustrates the current waveforms of the proposed system and the state of the different semiconductor switches.

III. Control System Implementation

This section deals with the digital implementation of the several tasks that the control system must perform. The proposed control system is organized in hierarchical layers. The top layer performs the communication with the external supervision and command system (SCS). The following layer is in charge of pulse shaping according to the parameters provided by the SCS; and the bottom layer is composed of the current controls and the regulation loops. This latter contains the most complex and most computational intensive tasks. Additionally, the communication with the analog to digital and digital to analog converters is realized concurrently with the tasks performed in all these layers. Fig. 4 depicts a block diagram of the implemented control system. A more detailed description of these blocks, listed hierarchically, is provided next.

1) Supervision and Command System Interface: This block performs the communication with the hierarchical supervision and command system. This system receives the pulse width, the reference current, and the synchronization command (the pulse must be synchronous with other converters). This block provides the converter status as well.

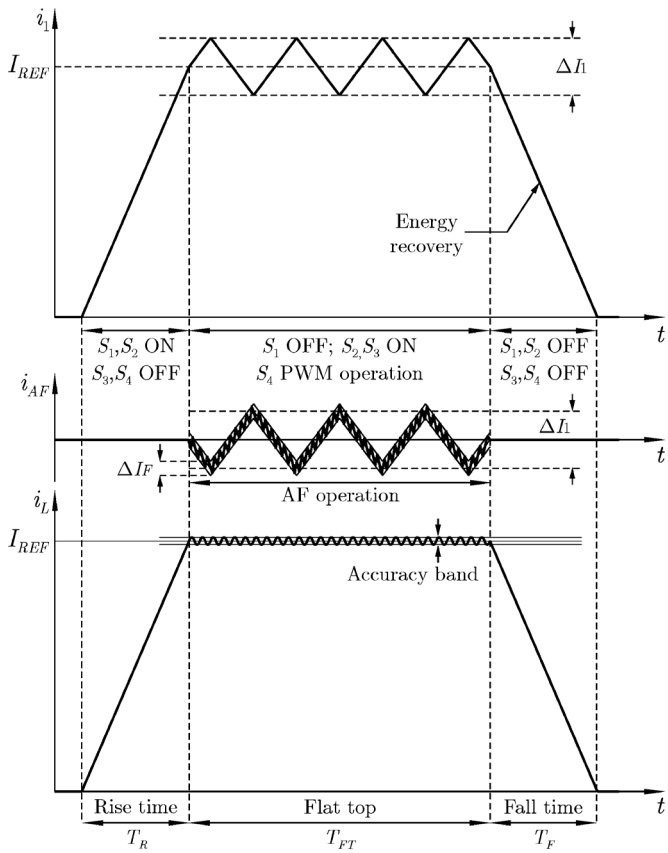


Fig. 3. Current waveforms and operation principle.

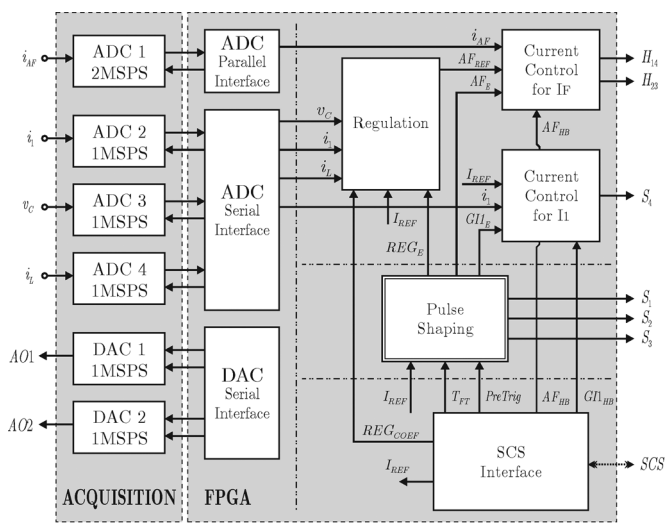


Fig. 4. Block diagram of the digital control board.

2) Pulse Shaping: This block manages the interconnection of different structures through the control of S_1, S_2, and S_3 states, and the enabling of the Current Control and Regulation Blocks. The performed tasks in the different stages are implemented by means of a state machine depicted by the flow chart in Fig. 5.

In this flow chart, it can be noticed that the system remains in idle state and goes to the triggering stage when the pretrigger command is received from the SCS block.

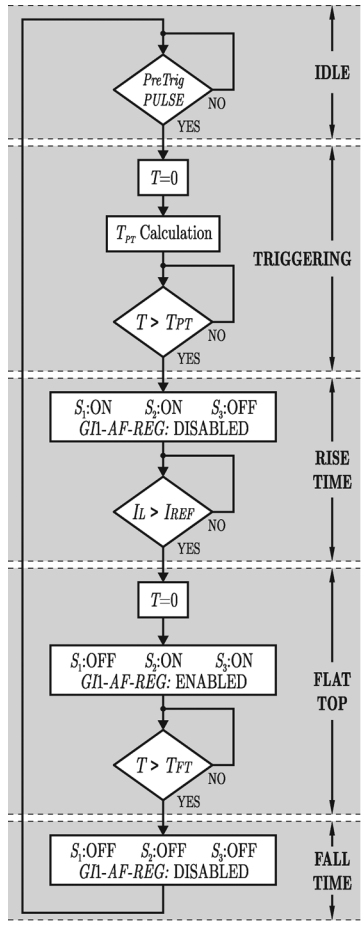


Fig. 5. Flow chart of the pulse control block.

The triggering stage determines the rise time beginning. This event must be adjusted to obtain a constant delay, $\Delta T_{\rm PT}$, between the pretrigger signal and the flat top beginning. $\Delta T_{\rm PT}$ is composed of two times, the delay $T_{\rm PT}$ between the pretrigger signal and the start pulse, and the rise time T_R. Since, T_R depends on the reference current, $T_{\rm PT}$ must be adjusted for each pulse. Fig. 6 illustrates the synchronism to different flat top currents. The pretrigger time $T_{\rm PT}$ is calculated by means of (2)

$$T_{\rm PT} \approx \Delta T_{\rm PT} - \frac{(L+L1)I_{\rm REF}}{V_{C1}}. \tag{2}$$

During rise time, switches S_1, S_2, and S_3 are commanded as it was previously indicated in Section II, while current controls and regulation loops remain disable. The transition from the rise time stage to the flat top stage is performed when the condition $i_L > i_{\rm REF}$ is satisfied. Once in the flat top, the state of the switches S_1, S_2, and S_3 change and, the current controls and the regulation loops are enabled. The transition from the flat top stage to the fall time stage is done when a timer, that starts at flat top beginning, reaches a time $T_{\rm FT}$. In fall time stage, all switches are turned off and, the current controls and the regulation loops are disabled.

3) Current Control Blocks: The current controls of $GI1$ and AF are performed by digital hysteresis controls. These controls involve the acquisition of the currents and its comparison

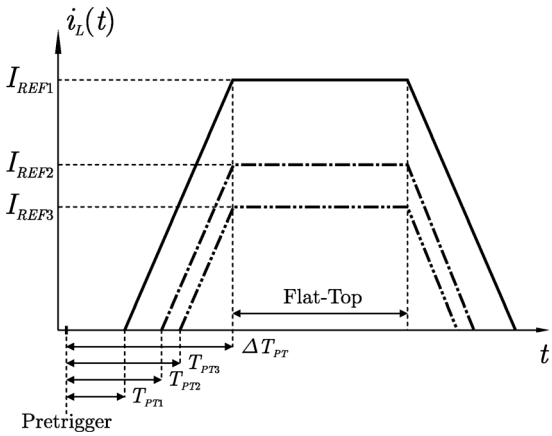


Fig. 6. Scheme of the discharge pulse triggering system operation.

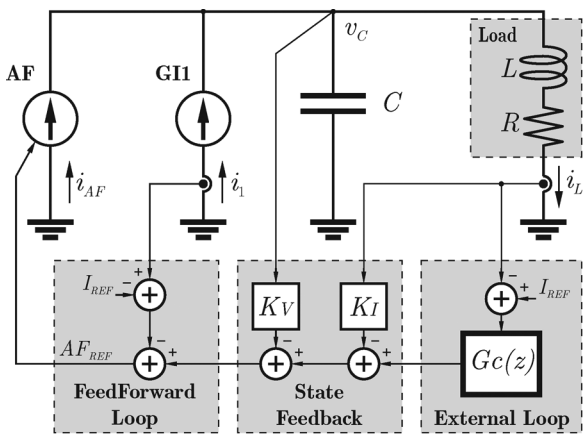


Fig. 7. Flat top equivalent circuit.

with hysteresis bands. The presence of delays in the acquisitions leads to errors in the detection of the crosses with the bands. The magnitude of these errors depends on the current slopes. Therefore, due to the high slopes of i_1 and $i_{\rm AF}$, high acquisition frequencies are needed.

The current controls are implemented with state machines, comparators, and counters. The switching output signal to generate the $i_{\rm AF}$ i_1 current is limited in frequency to avoid switch damage.

4) Regulation: As the system is made up of different interconnected structures, a transient is generated each time a structure is connected/disconnected. This aspect is critical at the beginning of the flat top, as the generated transient can exceed the system specifications of duration and amplitude. Fig. 7 illustrates an equivalent circuit of the system in the flat top. The capacitor and the load form a second order circuit with a low damping factor. If the initial conditions of the circuit are not appropriate ($i_1 = i_L \neq I_{\rm REF}$ or $v_C \neq I_{\rm REF} \cdot R$), a damped oscillatory response is generated.

In practice, the appropriate conditions are very difficult to obtain due to possible delays in the devices operation. To improve the transient response of the system, a state feedback control is proposed to place the closed loop poles of the second order circuit. This control is implemented by means of the gains of K_V

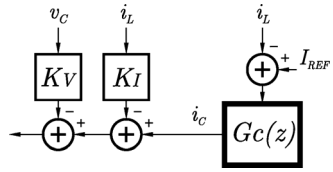


Fig. 8. Feedback loops.

and K_I, which are estimated by means of the Ackerman method [21]. As the resulting transfer is a type-0 system, there will be a steady-state error in the mean value of i_L, which is compensated by an external loop with an integral type controller. With a view to improving i_1 current ripple rejection in the flat top and to reduce the external loop requirements, a feedforward loop is incorporated by adding the difference between the $I_{\rm REF}$ and i_1. The feedforward, state feedback, and external loops are implemented by means of the AF.

The duration and the amplitude of the load current transient error can be adjusted by setting the state feedbacks and the external loop gains. In order to obtain a transient response mainly dependent on the external loop bandwidth, K_I and K_V are adjusted to place the poles above the bandwidth. To improve the transient response, the loop gains must be adjusted, with the consequent higher control effort. This implies that the feasibility of improving the transient response is limited by the capabilities of the AF.

The control system is implemented in a Spartan-3 FPGA that provides embedded multipliers. These ones accept two 18-bit words as inputs and produce a 36-bit product. Consequently, the regulation loops are implemented using an 18-bit fixed point arithmetic format for the multipliers input variables and a 36-bit word length for the addition calculations.

In order to select the normalization constant, the signals of greatest magnitude, in this case those corresponding to blocks G_C and K_I, are determined (Fig. 8).

The block G_C output (i_C) can be divided into two components

$$i_C = \overline{I_C} + \widetilde{I_C} \tag{3}$$

where $\overline{I_C}$ is the constant term that equals the addition of the feedbacks from K_V and K_I, and $\widetilde{I_C}$ is the variable term that corrects i_L variations.

The constant term can be expressed as

$$\overline{I_C} = K_V \overline{V_C} + K_I \overline{I_L} = (K_V R + K_I) \cdot I_{\rm REF} \tag{4}$$

Since this term is constant and known and its magnitude is highly elevated, it is eliminated from the controller and later added as a summing stage in its output. As a result, the controller output operates at low levels of magnitude. Besides, if $K_V R \ll K_I$, the term $K_V R$ can be simplified, giving rise to the schematic shown in Fig. 9.

Still there are problems associated to a resolution loss for normalization due to the fact that the $K_I i_L$ and $K_I I_{\rm REF}$ terms are much higher than the controller output or $K_V v_C$. This can be overcome by modifying the order of operations, as shown in Fig. 10. It can be observed that as i_L is close to $I_{\rm REF}$, $K_V v_C$,

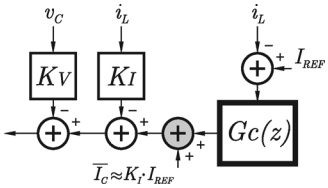


Fig. 9. Feedback loop modification.

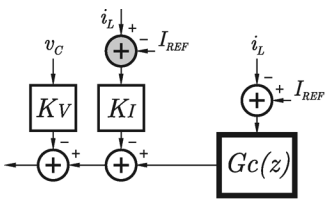


Fig. 10. Resultant feedback loop.

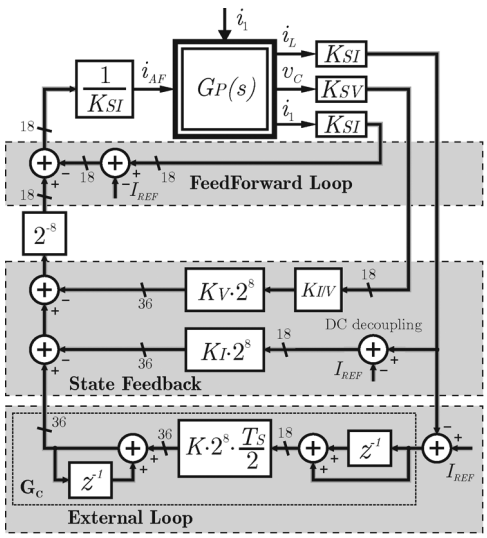


Fig. 11. Detailed implementation.

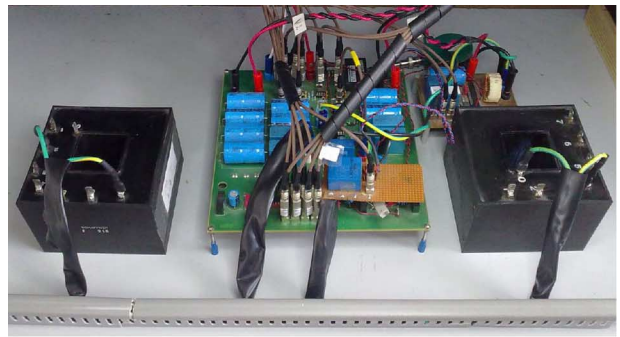
$K_I i_L$ and $G_C(z) \cdot (i_L - I_{\mathrm{REF}})$ terms are of the same order of magnitude.

Finally feedback loops gains were normalized with a 2^8 factor, that is considered before the feedforward loop. Fig. 11 depicts a detailed scheme of the loops implemented in this block.

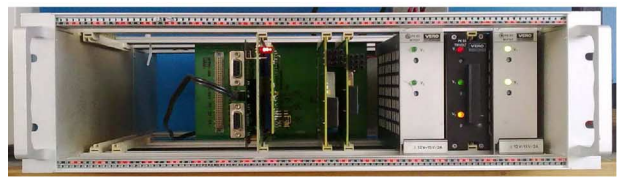
The gain blocks K_{SI} and K_{SV} include the magnitudes from the sense and the ADC conversion stages. These gains are $K_{SI} = 2^{17}/I_{\mathrm{MAX}}$ and $K_{SV} = 2^{17}/V_{\mathrm{MAX}}$, where I_{MAX} and V_{MAX} represent the input dynamic ranges of the sensing system. The sensing stage gains are scaled in order to maintain the dynamic range of the digital control platform fixed regardless of the generated current value. The ADC outputs are converted from 16 to 18 bits to match the numeric format.

The factor $K_{I/V}$ before the K_V block adjusts a gain difference between K_{SV} and K_{SI}. The i_{AF} generator is represented with the gain $1/K_{SI}$.

5) ADC and DAC Interface Blocks: The acquisition module consists of four ADC converters with their corresponding differential input filters. The 16-bit ADC converters are used to acquire i_1, i_L and v_C at 1 MSPS with serial communication and i_{AF} at 2 MSPS with a parallel one. This board is also equipped with two DAC converters able to generate test signals to debug the system. The blocks used to command the ADC and DAC converters are implemented with state machines that work at 40 and 20 MHz, respectively.



(a)



(b)

(c)

(d)

Fig. 12. Photos of the control system implementation. (a) Converter prototype (Current Scale 1:100). (b) Control system rack (control system board and power supplies). (c) Control system board–front side (Xilinx FPGA development kit). (d) Control system board–back side (acquisition and debugging board).

IV. Experimental Results

In order to validate the proposed topology and the associated control system, a low scale prototype was developed [Fig. 12(a)]. This prototype was designed based on the full scale converter specifications (Table I) proposed in [13]. The current and voltage values of the prototype were scaled down to laboratory levels (∼100 times). Even though this downscaling would allow to operate the prototype with frequencies higher

TABLE I
FULL SCALE PROTOTYPE PARAMETERS

L	1 mH	I_{REF}	2000 A
R	0.15 Ω	T_R, T_F	$<$ 1 ms
L_1	500 μH	Settling time T_{ST}	$<$ 200 μs
L_F	50 μH	Flat top duration	3 ms
C	4 μF	Current precision	500 ppm
V_{C1}	3000 V	f_{I1}	10 KHz
$V_{C2} = V_{C3}$	600 V	f_{IF}	100 KHz

TABLE II
LOW SCALE PROTOTYPE PARAMETERS

L	1 mH	I_{REF}	15 A
R	0.15 Ω	T_R, T_F	$<$ 1 ms
L_1	500 μH	Settling time T_{ST}	$<$ 200 μs
L_F	50 μH	Flat top duration	3 ms
C	4 μF	Current precision	500 ppm
V_{C1}	20 V	f_{I1}	10 KHz
$V_{C2} = V_{C3}$	10 V	f_{IF}	100 KHz

than those indicated in Table I, the switching frequencies and the relevant times (T_R, T_F and T_{ST}) were kept as in this table. The main parameters of the low scale prototype are listed in Table II.

Note that the differences between these prototypes are given by the power and the sensing stages while the developed control platform is valid for both systems. Therefore, the prototype could be used like a simulator for this platform.

The control system was developed to be mounted on a 2U rack [Fig. 12(b)]. To test it, a FPGA development Kit of Xilinx [Fig. 12(c)] together with a custom acquisition and debugging board that includes ADC and DAC converters [Fig. 12(d)] were used. An additional board was used to link and connect them to the rack. The latter also provides the circuitry necessary to adapt the levels of the switch command signals. Currently, a single board containing the complete control system is under development.

The control was described in VHDL and implemented in a Xilinx FPGA Spartan 3 (3S200FTG256-5) with ISE software [22]. This FPGA contains a total of 1920 slices and 12 18-bit dedicated multipliers. Resources utilization was around 39%, and it included 3 out of the 12 available multipliers. The design was defined with timing constrains to assure the time specifications of the acquisitions and the regulation loops. The main clock used was of 160 MHz which was generated from the external 50 MHz clock using a Digital Clock Manager.

Fig. 13 displays the more relevant signals of the topology when a 15 A pulse with a 3.5 ms flat top time is generated. Load current i_L, $GI1$ generator current i_1, capacitor voltage v_C and active filter current $i_{\rm AF}$ are arranged from the top downwards. As it can be observed, pulse generation presents no oscillations or significant variations during the coupling of structures (beginning and end of the flat top), as expected. In addition, times $T_R = 1$ ms and $T_F = 0.6$ ms were within specifications. It can be seen that T_R was greater than T_F because, during the rise time, the forward voltage of the devices and V_{C1} have an

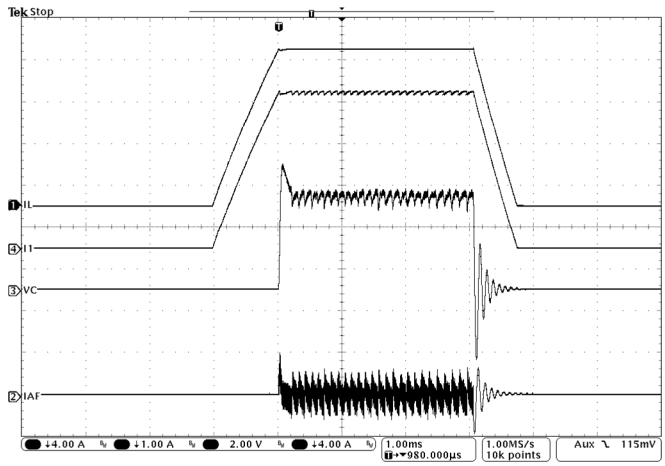


Fig. 13. Waveforms of the more relevant voltage and current signals.

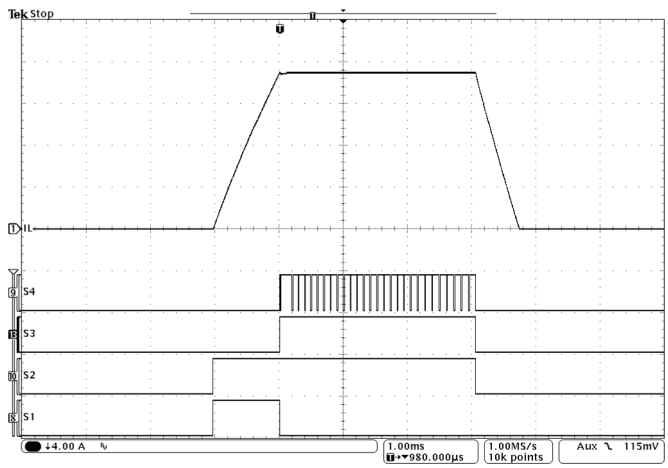


Fig. 14. Waveforms of the i_L current and S_1, S_2, S_3, and S_4 control signals.

opposite polarity, while during the fall time they have the same polarity.

Fig. 14 depicts the load current together with the signals to drive the S_1, S_2, S_3, and S_4 switches. The states of the switches associated to each pulse generation stage can be seen; and the difference between the commutation frequencies of the switches noticed.

A detail view of the signals at the beginning of the flat top is illustrated in Fig. 15. i_L and i_1 currents, command signals for S_1, S_3 and S_4, voltage v_C, current $i_{\rm AF}$ and signals to control the active filter are arranged from the top downwards. This figure shows that a transient response in the load current is produced as previously described in Section III-A4. In this test, the worst case was evaluated, which corresponds to the connection of the capacitor initially discharged. This condition generates a transient response with a drop in the load current. By means of the compensation strategy applied, the transient response has been adjusted so as to obtain a damped response with a settling time below 200 μs, thereby meeting the specifications. During the transient response it can also be noticed, that variations in v_C change the slopes of i_1, which temporarily modifies its switching period.

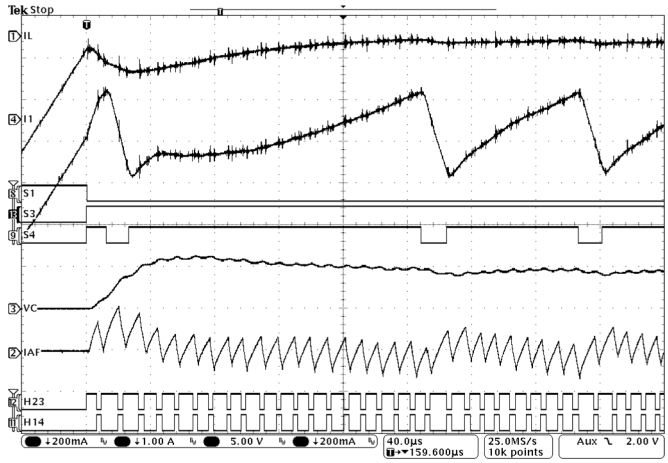


Fig. 15. Waveforms of the more relevant voltage, current and switch control signals at the flat top beginning.

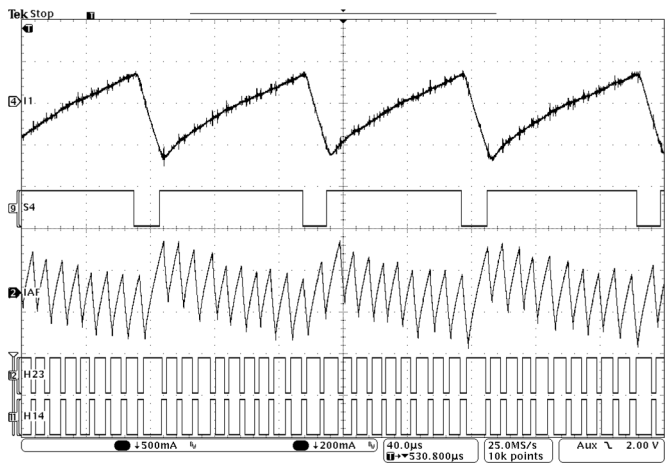


Fig. 16. Current waveforms generated by $GI1$ and AF and its corresponding control signals once the transitory was finished.

Fig. 16 exhibits the currents of the $GI1$ (top) and AF (bottom) generators during the flat top once the transient response is extinguished. In addition, together with each of these, the switch command signals are displayed. Note that the commutation frequency of the $GI1$ and AF are closed to 10 and 100 KHz, respectively. It can be noted that, as the active filter must cancel the $GI1$ ripple, the average value of i_{AF} results approximately equal to the inverse of the i_1 ripple.

V. Conclusion

This paper describes the most relevant aspects of the digital control system implementation developed for a multiple-stage converter. The proposed control, based on FPGA technology, enables the management of the several converter structures assuring the requirements of minimum duration and amplitude transient response in the load current and high-precision in the flat top. This control, associated to a previously proposed converter topology, makes the power source suitable for the generation of high-current pulses with high precision in the flat top and low rise and fall times. Tests performed with a prototype validate the proposal.

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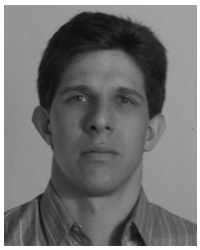

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