Performance of a Zero Average Dynamics-controlled buck converter using different pulse-width modulation schemes

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SUMMARY

The response of a digital Zero Average Dynamics (ZAD)-controlled buck converter under the variation of its intrinsic parameters as well as the pulse-width modulation signal is studied in detail. The multiparameter analysis presented here leads to a complete knowledge of the different dynamical scenarios exhibited by the system. Numerical results indicate that the success of the ZAD-strategy is highly dependent on the parameter and pulse-width modulation (PWM) combinations. Experiments are included to validate the performance inside the so-called optimum region. Copyright © 2013 John Wiley & Sons, Ltd.

1. INTRODUCTION

Basically, a dc-dc buck converter is an electronic circuit that transforms its input voltage into a lower one by means of a transistor, acting as a switch, and an RLC low-pass filter. The switching actions are administrated by a pulse-width modulation (PWM) block. Because the output also needs to be regulated, this kind of circuits always includes a feedback loop [1,2].

The output voltage of a buck converter is proportional to the so-called duty cycle, which is defined by the relation between the turn-on and turn-off intervals assigned to the switch. Ideally, the output is independent of the sequence in which they arrived during a period. Some of the modulation schemes traditionally used in the practice [3] are the following: the trailing-edge PWM (TE PWM), where the turn-on interval always occurs at the beginning of the period; the leading-edge PWM (LE PWM), where the turn-off interval always occurs at the beginning of the period; and the symmetric double-edge PWM (DE PWM), where the turn-off (or turn-on) interval is distributed into two equal parts at the beginning and the end of the switching cycle.

Because of the development of more accessible and versatile microcontrollers and processor units, the digital implementation of the modulation and control of dc-dc converters has became a common alternative. Among other advantages, this approach adds flexibility to the following: the PWM block, making possible to implement different modulation signals; the data acquisition, permitting to select the sampling instants and rates. Nowadays, it is common to find, for example, that the

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commutations of the switch are displaced with respect to the measurement instants [4,5], avoiding basically that the noise originated by the operation of the transistor propagates to the feedback loop. Furthermore, new double-edge modulations have been proposed trying to improve steady-state and transient performances of buck converters [6].

Traditional discrete-time models have demonstrated to be very useful for describing the appearance of different dynamical scenarios (e.g. period-doubling bifurcations, Neimark–Sacker bifurcations, discontinuity-induced bifurcations and even chaos) related to analog, and even digital, implementations [7–14]. However, they are not prepared to consider all the current sampling and modulations variations. Several contributions have shown that the dynamical response of different converters can change because of delays in the digital feedback loop [15,16]. A particular case takes place when a buck converter is controlled by a nonlinear law known as Zero Average Dynamics (ZAD) strategy. Results show that the closed-loop system changes radically its characteristics implementing a DE PWM instead of a TE PWM. Although contributions always associate the former with this kind of control, neither of them try to explain why the DE PWM seems to be the most appropriate modulation [17–22].

Recently, new small-signal discrete-time models for dealing with different kinds of delays in the digital loop and/or sampling instants at any time during a switching period have been proposed in [23,24]. A small-signal z-domain model is also derived in [25] but with the purpose of quantifying the dynamic of a converter for different modulation signals. All these contributions have in common that the proposed models are inappropriate for carrying out a complete study of the influence of digital PWMs over the appearance of nonlinear phenomena.

A discrete-time model that can reproduce the nonlinear dynamics of a buck converter under different PWM schemes is considered in this paper. By means of the variation of a new parameter, it is possible to represent any arbitrary location of the switching instants. State-variable equations are derived by fixing the sampling instants at the beginning of the period. The aim is to describe how the performance of the converter controlled by a digital version of the ZAD-strategy is improved/degraded depending on the parameters and the implemented modulation signal. The closed-loop system is analyzed in detail via numerical simulations.

Results presented here extend and enhance the preliminary contribution [26] where the study is made for a specific output voltage reference. The analysis not only contemplates the variation of that parameter for all its possible range but also considers deviations in the switching period and the time constant of the circuit. An optimum operation region, which clearly includes the DE PWM modulation, is defined. Experimental measurements corroborate the findings.

This paper is organized as follows. The generalized discrete-time model of the buck converter and the respective ZAD control expressions are presented in Sections 2 and 3, respectively. Changes presented in the behavior of the system according to parameter and PWM combinations are described in Section 4. Robustness of the system is analyzed in Section 5, and experimental results are included in Section 6. Finally, conclusions are given in Section 7.

2. GENERALIZED DISCRETE-TIME MODEL OF THE DC-DC BUCK CONVERTER

The circuit diagram of a well-known dc-dc buck converter is shown in Figure 1(a), where E is the input voltage to be reduced, S and D are the switch and the diode used for generating a square signal of frequency f, and inductance L, capacitor C and load resistance R are the components of the low-pass filter necessary to obtain the new dc level (which actually is the average value of the square signal).

Ideally, the controller maintains the output voltage at the desired v_{ref} value calculating the duty cycle d_k ($0 \le d_k \le 1$) that has to be assigned to the switch at each fixed period kT. Because it is considered a digital implementation, d_k will be obtained according to state values at the sampling instants (at the beginning of the period).

The PWM block generates the modulation signal u that governs switch S. A form of representing u, which is valid for most PWM schemes used in the practice, is proposed in Figure 1(b). According to the figure, variable u can be expressed as
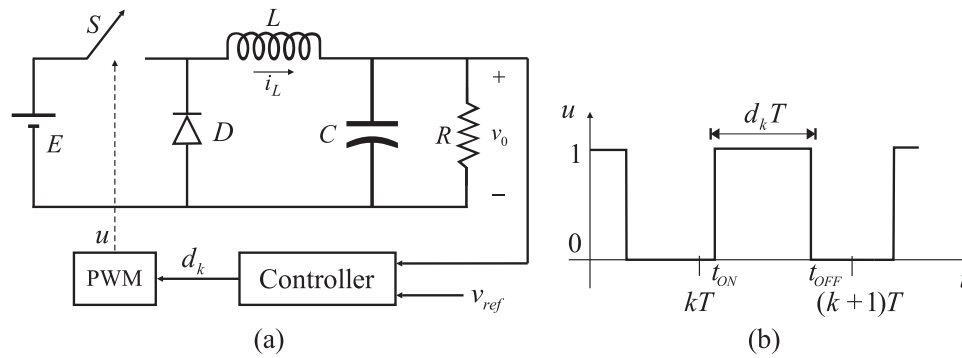
Figure 1. (a) Voltage controlled buck converter; (b) Generalized pulse-width modulation signal.

$$u = \begin{cases} 0 & \text{if} \quad kT \leq t < t_{ON}, \\ 1 & \text{if} \quad t_{ON} \leq t < t_{OFF}, \\ 0 & \text{if} \quad t_{OFF} \leq t < (k+1)T, \end{cases}$$

where $u = 1$ ($u = 0$) implies that S is closed (open) and t_{ON} (t_{OFF}) is the instant where S is turned on (off). As it can be inferred, $t_{OFF} - t_{ON} = d_k T$. For compactness, instants t_{ON} and t_{OFF} are specified as

$$t_{ON} = kT + (1 - \alpha)(1 - d_k)T/2,$$
$$t_{OFF} = kT + (1 - \alpha)(1 - d_k)T/2 + d_k T.$$

with α ($-1 \leq \alpha \leq 1$) as a parameter that results more representative of the PWM scheme. Table I illustrates the correspondence between some α values and the classical PWM.

As it has been widely demonstrated in the literature, discrete-time models results are appropriate to carry out a detailed analysis of the dynamic of dc-dc converters [7–9]. Defining the normalized variables $x_1 = i_L E^{-1} \sqrt{L/C}$, $x_2 = v_0/E$, $\tau = t/\sqrt{LC}$ and parameters $\gamma = R^{-1} \sqrt{L/C}$, $x_{2ref} = v_{ref}/E$ and $T_n = T/\sqrt{LC}$, the state-space representation of the buck converter is given by

$$\dot{x} = Ax + Bu \tag{1}$$

where x is the state vector $x = [x_1, x_2]^T$,

$$A = \begin{pmatrix} 0 & -1 \\ 1 & -\gamma \end{pmatrix} \text{and } B = \begin{pmatrix} 1 \\ 0 \end{pmatrix}.$$

Then, taking into account the ODEs general solution [27], that is,

$$x(\tau) = e^{A(\tau - \tau_0)} x(\tau_0) + \int_{\tau_0}^{\tau} e^{A(\tau - \xi)} Bu d\xi, \tag{2}$$

Table I. Relation between the α values and the classical PWM schemes.

α	t_{ON}	t_{OFF}	PWM scheme
1	kT	$kT + d_k T$	TE PWM
−1	$kT + (1 - d_k)T$	$(k+1)T$	LE PWM
0	$kT + (1 - d_k)T/2$	$kT + (1 - d_k)T/2 + d_k T$	DE PWM

it is possible to calculate the state variables at instant $(k+1)T_n$ as a function of the states at the previous period kT_n. In fact, considering the initial condition $x_k = x(kT_n)$ and solving (2) during one period [Figure 1(b)], it results[1]

$$x_{k+1} = e^{AT}x_k + \psi(d_k),$$
(3)

where

$$\psi(d_k) = e^{-A(1-\alpha)(1-d_k)\frac{T}{2}}e^{AT}(I - e^{-Ad_kT})A^{-1}B.$$

In contrast to the classical mappings, the definition of α permits to formulate a more complete nonlinear discrete-time model that reproduces the dynamics of the buck converter according to the variations of its intrinsic parameters as well as the adopted modulation signal.

3. DIGITAL ZAD CONTROL LAW

The duty cycle d_k is calculated here taking into account the ZAD control law [17,18]. This nonlinear feedback can be considered as a modified version of sliding mode control. Given a dynamical system $\dot{x} = f(x)$ and a switching surface $s(x) = 0$, sliding-mode control consists on making the trajectories evolve on $s(x) = 0$. This approach implies the operation of the converter at variable switching frequencies, leading to undesirable chattering phenomena. In the ZAD-strategy, $s(x) = 0$ is fulfilled only in average over each period, that is $E_T(s(x)) = 0$ with

$$E_T(s(x)) = \frac{1}{T}\int_{kT}^{(k+1)T} s(x(t))dt,$$
(4)

making it possible to operate at a fixed switching frequency.

Considering the surface $s(x) = (x_2 - x_{2ref}) + k_s\dot{x}_2$ with k_s as the time constant associated to its first order dynamics, the calculation of (4) leads to the treatment of a transcendental equation in each switching period. Because it is usually time-consuming to solve such expression in a digital implementation, a piecewise-linear approximation of the error surface is adopted [18,19]. For the generalized modulation signal of Figure 1(b), the alternative function is given by

$$\hat{s}(x) = \begin{cases} s_0 + (t - kT)\dot{s}_1 & \text{if } kT \le t < t_{ON} \\ s_0 + (t_{ON} - kT)\dot{s}_1 + (t - t_{ON})\dot{s}_2 & \text{if } t_{ON} \le t < t_{OFF} \\ s_0 + (t_{ON} - kT)\dot{s}_1 + (t_{OFF} - t_{ON})\dot{s}_2 + (t - t_{OFF})\dot{s}_1 & \text{if } t_{OFF} \le t < (k+1)T \end{cases}$$

where $s_0 = s(x_k)$, $\dot{s}_1 = \dot{s}_1(x_k)$ is the derivative of $s(x)$ calculated at $t = kT$ with $u = 0$,

$$\dot{s}_1 = (1 - k_s\gamma)(x_{1,k} - \gamma x_{2,k}) - k_s x_{2,k},$$

and $\dot{s}_2 = \dot{s}_2(x_k)$ is the same derivative evaluated at $t = kT$ but considering $u = 1$,

$$\dot{s}_2 = (1 - k_s\gamma)(x_{1,k} - \gamma x_{2,k}) - k_s(x_{2,k} - 1) = \dot{s}_1 + k_s.$$

Thus, solving (4), it results the algebraic equation

$$s_0T + \frac{1}{2}\dot{s}_1T^2 + \frac{1}{2}(1 + \alpha)k_s d_kT^2 - \frac{1}{2}k_s\alpha(d_kT)^2 = 0,$$
(5)

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[1]For simplicity, T_n is rewritten as T.

which makes it possible to obtain explicit expressions of duty cycle d_k as a function of the state values at the beginning of each period. Table II summarizes them according to the different PWM schemes. The respective deductions can be found in the APPENDIX.

4. NUMERICAL ANALYSIS OF THE CLOSED-LOOP SYSTEM

Different aspects to take into account in the implementation of the ZAD-strategy for controlling a buck converter are described here. They derive from the numerical analysis of stability, regulation, and nonlinear dynamics exhibited by the system when the control gain, the voltage reference, and the PWM scheme are varied. Most results are obtained by using the continuation toolbox MATCONT (Belgium) [28]. Table III resumes the nominal values of the experimental prototype used as a reference, the corresponding normalized quantities and the desired specifications.

4.1. Stability and regulation

To make the system operate according to specifications, it is essential to choose an appropriate value for the ZAD control gain. In general, the steady-state error (e_{ss}) has a tendency to decrease as k_s is diminished [19]. However, the gain cannot be reduced as much as desired because of stability and transients issues. As it will be shown here, the admissible k_s values are conditioned not only by the rest of the parameters but also by the adopted PWM scheme.

A family of curves illustrating the stability limits of the converter according to the (α, k_s) combination and considering different x_{2ref} values are shown in Figure 2. In all cases, the system is stable for k_s values above the curve. Crossing the curve, the controlled system becomes unstable as one eigenvalue of its Jacobian leaves the unit circle through -1.

Contrary to expectations, the k_s limits (named in the following as k_{smin}) could be considered practically independent from parameter α only for reference levels belonging to a very small neighborhood around $x_{2ref} = 6/12 = 0.5$. Figure 3(a) shows the obtained steady-state output voltage for some fixed k_s values. Although e_{ss} becomes greater as the gain moves from k_{smin}, it never exceeds the specified value. As k_{smin} is relatively small, the regulation of the converter is naturally satisfactory. Unfortunately, the transient response of the system presents the opposite behavior because it becomes worse as k_s is closer to k_{smin} [Figure 3(b)–(c)].

Table II. Control law expressions according to the different modulations.

State condition	$\alpha = 0$	$\alpha \neq 0$
$0 \leq -\frac{2s_0 + \dot{s}_1 T}{k_s T} \leq 1$	$d_k = -\frac{2s_0 + \dot{s}_1 T}{k_s T}$	$d_k = \frac{1+\alpha}{2\alpha} - \frac{\sqrt{k_s T(1+\alpha)^2 + 4\alpha(2s_0 + \dot{s}_1 T)}}{2\alpha\sqrt{k_s T}}$
$-\frac{2s_0 + \dot{s}_1 T}{k_s T} < 0$	$d_k = 0$	$d_k = 0$
$-\frac{2s_0 + \dot{s}_1 T}{k_s T} > 1$	$d_k = 1$	$d_k = 1$

Table III. Characteristics of the system under study.

Parameter	Value	Normalized parameter	Value
Inductance	238 μHy	γ	0.7116
Capacitance	18.8 μF	T	0.2990
Nominal resistance	5 Ohm	x_{2ref}	0.1 to 0.9
Input voltage	12 V		
Output voltage[a]	1.2 to 10.8 V	Specifications	
Switching frequency	50 KHz	Voltage steady-state error	< 2%
Clock frequency[b]	75 MHz	Transient response	<< 1 ms

[a]The range defined as possible output dc levels derives from practical duty cycle limits.
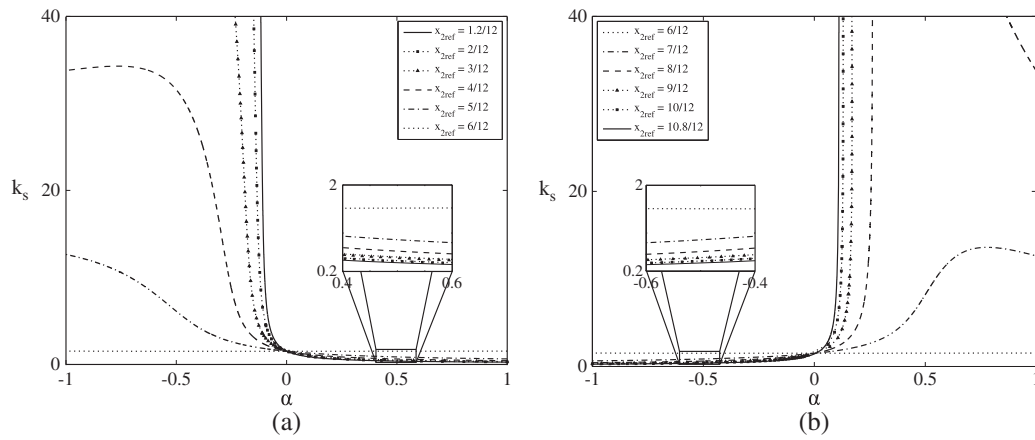[b]As a reference, it is considered the clock frequency of the processor Texas Instruments DSP TMS320F2812.

Figure 2. Stability curves of the ZAD-controlled buck converter: (a) $0.1 \leq x_{2ref} \leq 0.5$; (b) $0.5 \leq x_{2ref} \leq 0.9$.

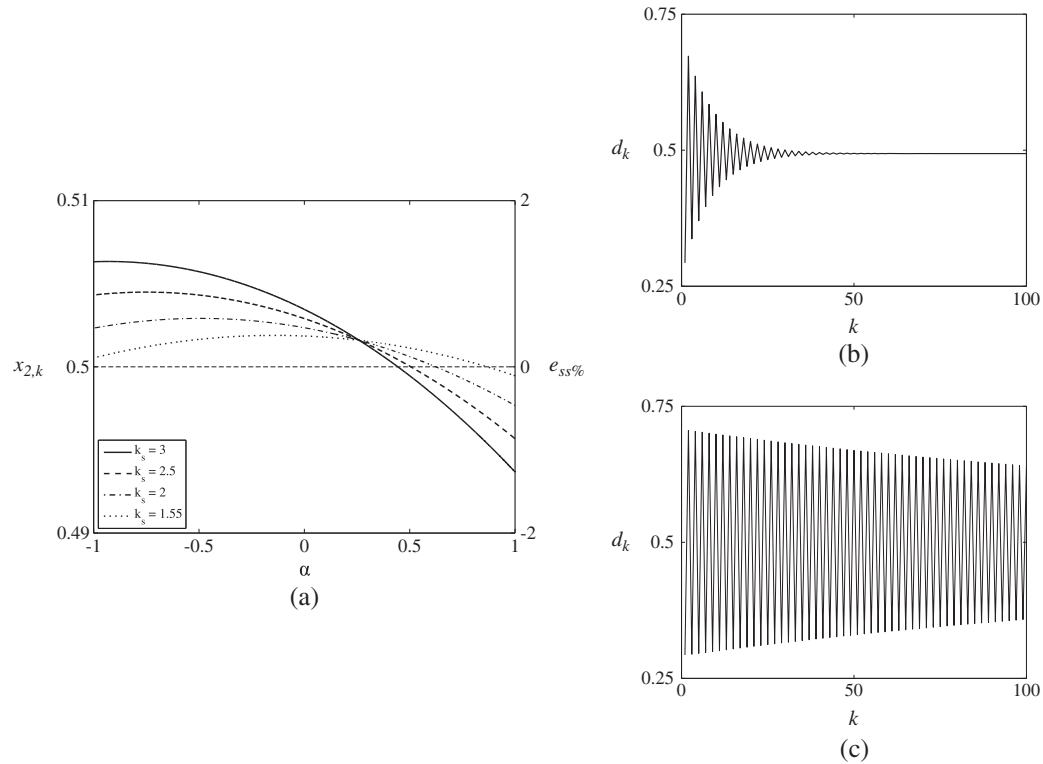

Figure 3. Response of the converter as a function of α for $x_{2ref} = 0.5$ and different k_s values. (a) Output voltage and steady-state error; (b) and (c) Evolution of d_k implementing the ZAD control with a TE PWM ($\alpha = 1$) and $k_s = 3$ and 1.55, respectively.

Now, as x_{2ref} moves away from 0.5, the performance of the ZAD-controlled buck converter becomes sensitive to modulation signal. For clarity, it will be differentiated into five cases:

(A) $x_{2ref} < 0.5$ and $\alpha \in [-1, 0)$
(B) $x_{2ref} < 0.5$ and $\alpha \in (0, +1]$
(C) $x_{2ref} > 0.5$ and $\alpha \in [-1, 0)$
(D) $x_{2ref} > 0.5$ and $\alpha \in (0, +1]$
(E) $0.1 \leq x_{2ref} \leq 0.9$ and α around zero.

The respective behaviors are discussed in the following cases.

4.1.1. Cases A and D. These two cases have in common that k_{smin} depends strongly on the pair (α, x_{2ref}), growing even excessively as x_{2ref} approaches to 0.1 or 0.9 [Figure 2(a) with $\alpha \in [-1, 0)$ and Figure 2(b) with $\alpha \in (0, +1]$, respectively]. This situation affects the regulation of the system because the admissible k_s gains can result significatively greater than zero. Thus, for example, the output voltage of the converter obtained by chosen TE PWM and LE PWM schemes and considering a k_s gain, which assures stability for all references, is shown in Figure 4(a). In all cases, the e_{ss} is superior to the maximum expected, achieving illogical levels such as 50%, 100%, and even more [Figure 4(b)].

The response could be improved only if each x_{2ref} is analyzed separately. Figure 5 illustrates how e_{ss} can be reduced for $x_{2ref} = 5/12$ and $7/12$, fixing gains near their own stability limits. However, because the admissible k_s values are still greater, the regulation is not so good as desired.

4.1.2. Cases B and C. For both cases, k_{smin} values present significatively minor variations with respect to α and x_{2ref}; moreover, their magnitudes are relatively small. As it can be observed in the blow-up of Figure 2(a) and (b), k_{smin} curves are always below the stability limit corresponding to $x_{2ref} = 0.5$.

Figure 6 shows the response of the converter obtained by considering TE PWM and LE PWM schemes and a k_s gain, which assures stability for all references. In contrast to the scenario of Figure 4, the e_{ss} keeps below the maximum expected for most reference levels [Figure 6(b)].
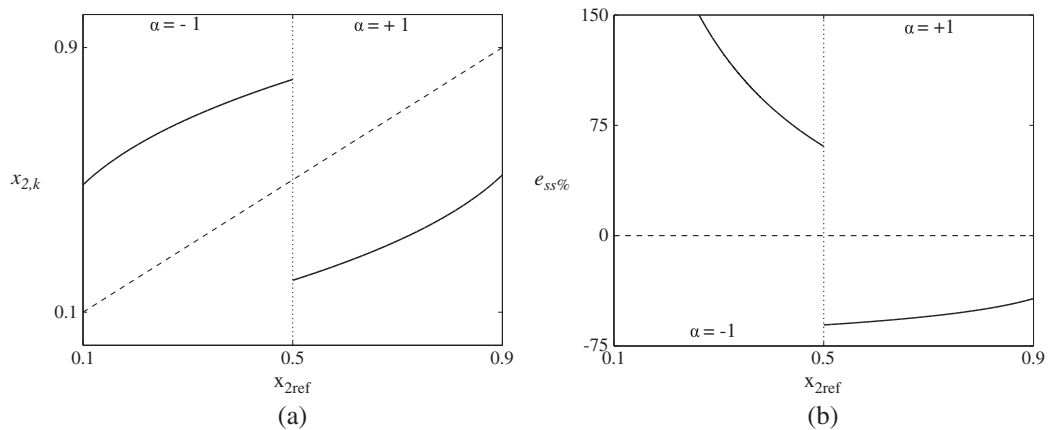

Figure 4. Response of the system as a function of x_{2ref} for $k_s = 100$. Modulation signals correspond to a LE PWM for $x_{2ref} < 0.5$ and a TE PWM for $x_{2ref} > 0.5$. (a) Output voltage; (b) the respective steady-state error.
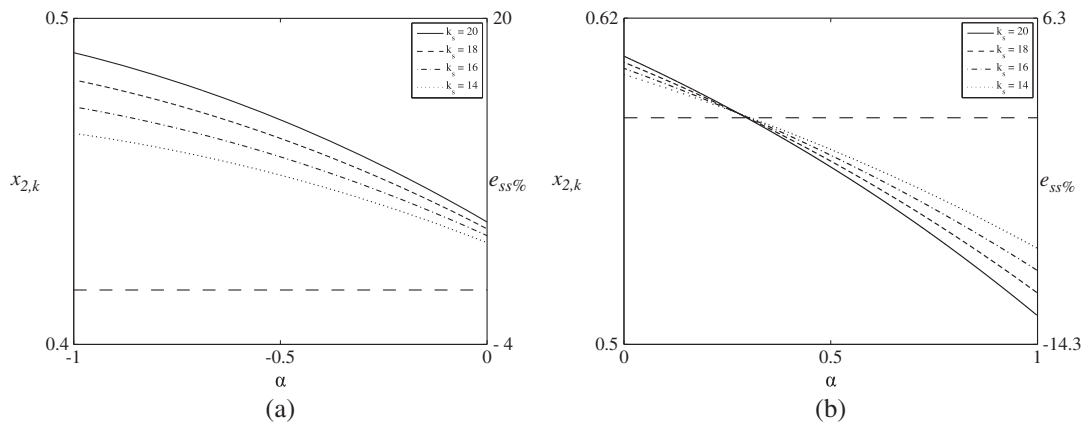

Figure 5. Output voltage regulation as a function of α for different k_s values. (a) $x_{2ref} = 5/12$; (b) $x_{2ref} = 7/12$.
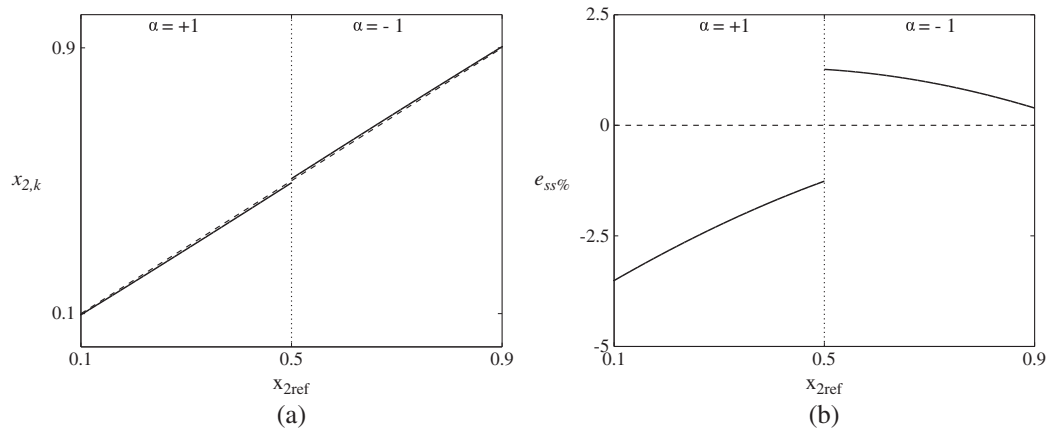
Figure 6. Response of the system as a function of x_{2ref} for $k_s = 3$. Modulation signals correspond to a TE PWM for $x_{2ref} < 0.5$ and a LE PWM for $x_{2ref} > 0.5$. (a) Output voltage; (b) the respective steady-state error.

Similarly to the previous cases, differences between the actual output voltage and the desired level can be ameliorated even more if the converter will operate at a fixed x_{2ref}. As it is illustrated in Figure 7 for $x_{2ref} = 5/12$ and $7/12$, regulation can be improved by using different α values and diminishing the control gain.

Conditions established in cases B and C make it possible to find combinations of k_s gains plus PWM schemes leading to a closed-loop response according to specifications for a determined set of reference levels: $x_{2ref} < 0.5$ for case B and $x_{2ref} > 0.5$ for case C. Unfortunately, there not exist a pair (α, k_s), which results appropriate for all x_{2ref} range. This is a limitation for those applications where variable output voltages are required.

4.1.3. Case E (Optimum region). Combining Figure 2(a) and (b), it can be noticed that there exist a zone around $\alpha = 0$ in which (α, k_s) pairs could result in a satisfactory implementation of the ZAD-strategy for all possible reference values. As depicted in Figure 8, the so-called optimum region can be defined as that delimited by the stability curves corresponding to the maximum and minimum x_{2ref} levels ($x_{2ref} = 0.1$ and 0.9). Except for a very small part of them (see blow-up), the rest of the curves is located below the defined region. Indeed, that zone of intersections will be hardly used in practical implementations because it is not convenient to choose control gains so close to the limits.

Figure 9(a) shows the steady-state response of the converter obtained by considering modulation schemes around the DE PWM ($\alpha = 0$) and a k_s gain, which assures regulation according to specifications for all reference levels. As it can be observed in Figure 9(b) and (c) for $x_{2ref} = 5/12$ and $7/12$, respectively, transients are also in the order of the desired value. To obtain faster
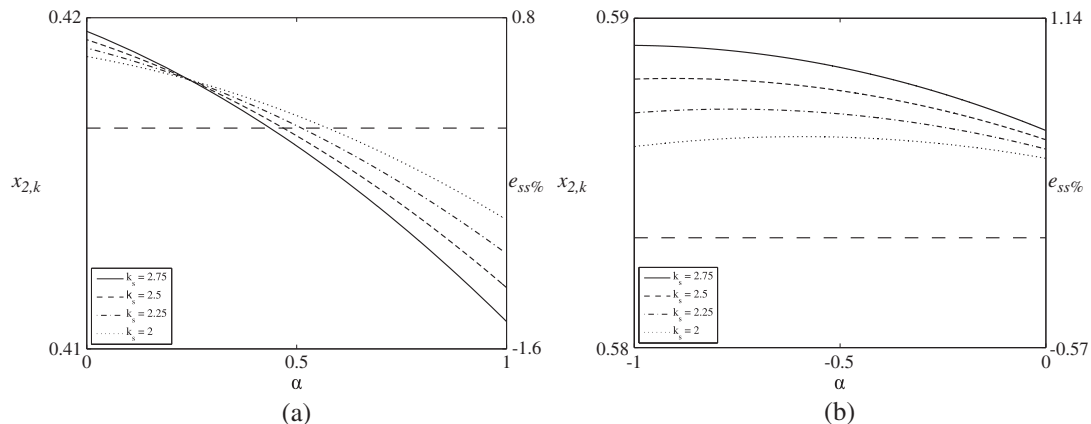

Figure 7. Output voltage regulation as a function of α and different k_s values. (a) $x_{2ref} = 5/12$; (b) $x_{2ref} = 7/12$.
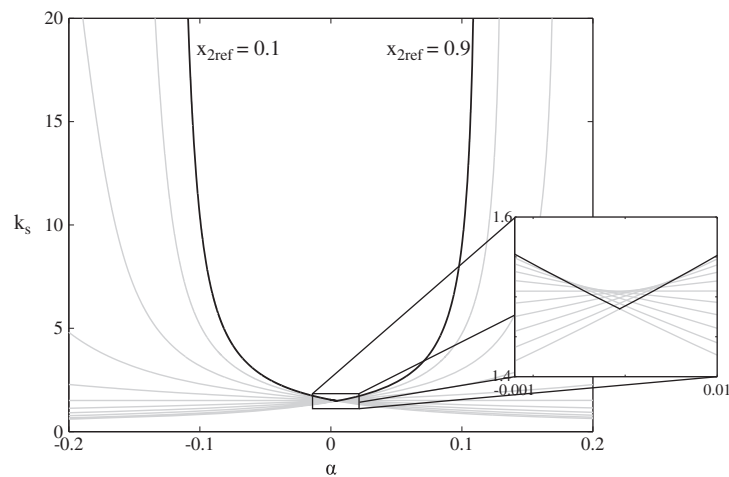
Figure 8. Optimum operation region defined by the stability limits of $x_{2ref} = 0.1$ and $x_{2ref} = 0.9$.
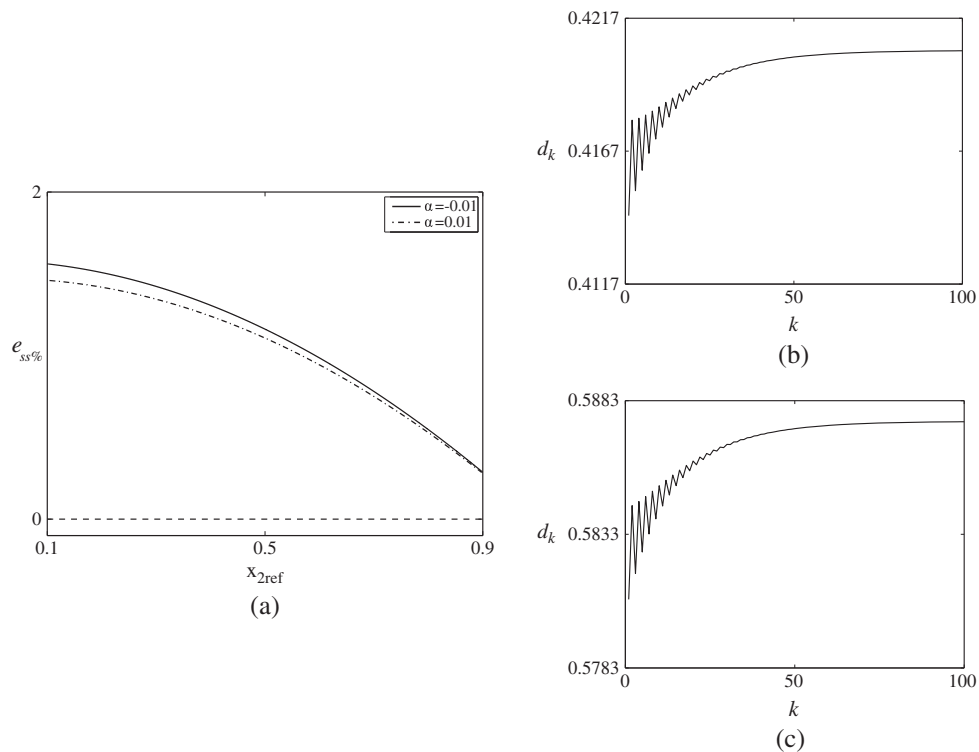

Figure 9. Response of the system for $k_s = 5$ and different α values around zero. (a) Steady-state error as a function of x_{2ref}; (b) and (c) Evolution of d_k implementing the ZAD control with $\alpha = 0$ and $x_{2ref} = 5/12$ and $7/12$, respectively.

responses, it is necessary to increase k_s, deteriorating the e_{ss}. It will be always a trade-off between regulation and transient response.

In some sense, Case E explains why the DE PWM is naturally associated to the ZAD-strategy in almost all the related contributions previously presented in the literature [18–21]. Moreover, results are in consonance with those given in [22], where it was formalized that, for arbitrary T and γ values, the stability limit of a ZAD-controlled buck converter with a DE PWM practically keeps unchanged as the reference level is varied.

4.2. Nonlinear dynamics

All the stability curves previously presented (Figure 2) actually correspond to the birth of period-doubling (PD) bifurcations. Analyzing the normal form coefficient σ also provided by the continuation toolbox MATCONT, it is found that the PD bifurcations can be subcritical ($\sigma < 0$) or supercritical ($\sigma > 0$) depending on parameter values. Moreover, it occurs that $\sigma = 0$ meaning that the PD bifurcation can also be degenerated [29]. In the first case, an unstable period-two orbit appears when the equilibrium point is stable. This new attractor acts reducing the domain of attraction of the desired operation point. In the second one, a stable period-two orbit appears when the equilibrium point is unstable. This orbit manifests as a over-modulation of the states of frequency $f_s/2$ but only if the parameter combination crosses the stability limit. Dynamic around the degeneracy is more complicated because there could exist multiple period-two orbits. In all cases, orbits are destroyed by a corner collision (CC) bifurcation, which occurs when the duty cycle of the switch reaches its bounds (ideally, $d_k = 0$ and $d_k = 1$).

Focusing on the optimum operation region (Figure 8), the ZAD-controlled buck converter could manifest these nonlinear behaviors if the reference level is equal to its maximum or minimum value, and the pair (α, k_s) is near the corresponding stability limit. As it is indicated in Figure 10, PD bifurcations are subcritical (PD−) for the segment of the curve above the degeneracy (located at $k_{smin} = 5.736739$ and $\alpha = -0.086138$). The rest of the curve corresponds to supercritical PD bifurcations (PD+). Figure 11 illustrates how these two kinds of nonlinear phenomena develop as the control gain is decreased for arbitrary α values. The adopted reference levels and PWM schemes are the following: $x_{2ref} = 0.1$, $\alpha = -0.095$ for Figure 11(a) and $x_{2ref} = 0.9$, $\alpha = 0.095$ for Figure 11(b). In both examples, bifurcation branches grow abruptly originating a fast saturation (corner collision) of the duty cycle. This is a common characteristic of ZAD-controlled converters, as it is pointed out in [19,20,22].

In the neighborhood of the degeneracy, PD− and CC bifurcations interact with a saddle-node (SN) bifurcation curve. The SN curve is originated by the two-codimension point $\sigma = 0$, and it indicates the birth of a pair of period-two orbits [29]. In this case, the inner one is unstable, while the outer one is stable. The point $\sigma = 0$ plus the intersections of the CC curve with the PD− and SN ones form a *triangular* zone. A very detailed description of the complete scenario developed in its locality is given in [21]. Basically, it occurs that, for parameter values inside the *triangle*, the stable equilibrium point coexists with a stable period-two oscillation. This phenomenon of existence of *feasible* orbits (as it is called in [21]) is illustrated in Figure 12(a) for $\alpha = -0.08614$.

From a practical viewpoint, this complex zone is extremely small. Qualitative changes take place when parameters are perturbed in their forth and even sixth decimal place. So, it results almost
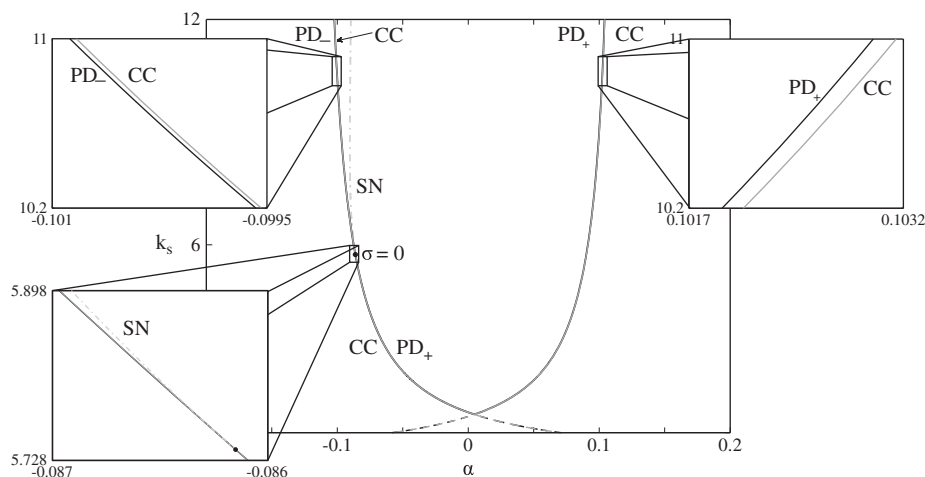

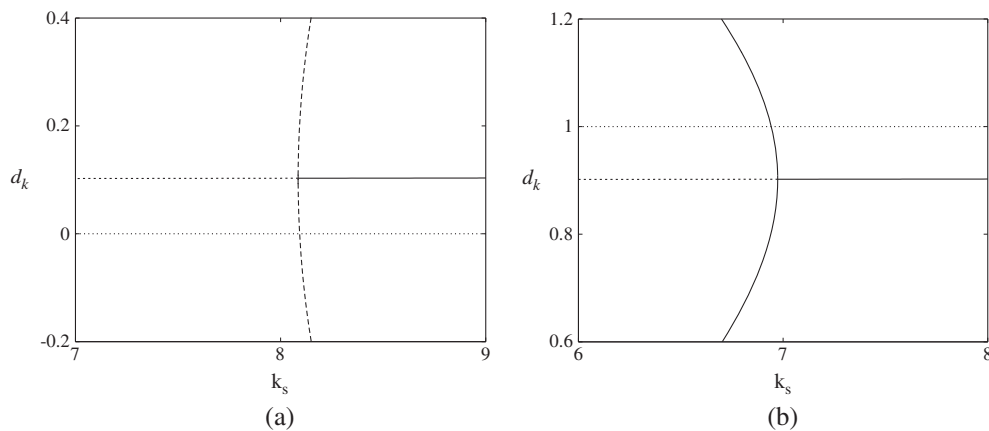Figure 10. Description of the nonlinear phenomena associated with the optimum region.

Figure 11. Examples of PD bifurcations for different parameter values: (a) Subcritical PD bifurcation for $x_{2ref}=0.1$ and $\alpha=-0.095$; and (b) Supercritical PD bifurcation for $x_{2ref}=0.9$ and $\alpha=0.095$.
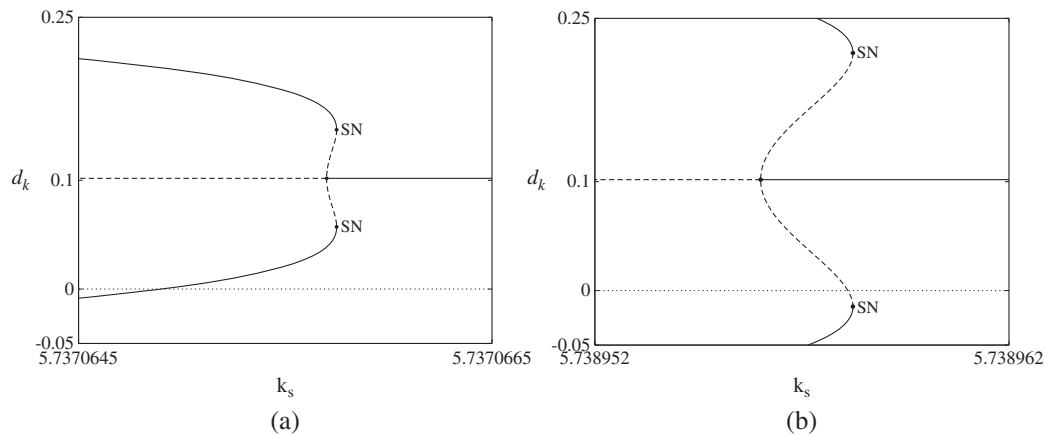

Figure 12. Multiple orbits near the degeneracy: (a) Existence of a *feasible* period-two oscillation for $\alpha=-0.08614$; (b) Existence of a *virtual* period-two oscillation for $\alpha=-0.08615$.

impossible to observe multiple attractors in a real implementation. Figure 12(b) shows how diminishing the previous α value in 1×10^{-5} ($\alpha=-0.08615$), the SN bifurcation occurs now after the saturation ($d_k=0$), indicating that the system is already outside the *triangle*. According to [21], the stable period-two oscillation becomes a *virtual* orbit.

Finally, it was analytically formalized in [22] that PD bifurcations are always supercritical when the ZAD-strategy is implemented by using a DE PWM. As it is clearly shown here, the scenario can become more complex with only changing the PWM scheme slightly. The expected dynamic is the same as that described in [21] for the transcendental version of the control law.

5. ROBUSTNESS

The optimum region defined previously for the appropriate operation of the ZAD-controlled buck converter can suffer modifications because of variations of its intrinsic parameters as well as unmodeled electrical characteristics of the switch and diode used in the practice. The possible effects of both aspects are discussed below.

5.1. Intrinsic parameters

The stability limits given by $x_{2ref}=0.1$ and $x_{2ref}=0.9$ change if parameters T or γ deviate from their nominal values. As it is shown in Figure 13, limit curves move to greater k_s magnitudes if γ is decreased [Figure 13(a)]. This can provoke that fixed k_s and α pair locates near the stability limit (deteriorating transient responses) or even crosses it for a new γ value. Thus, for example, considering that the buck converter operates with the same parameter values established in Figure 9 but the load resistance is increased to 10Ω ($\gamma=0.3558$), the steady-state error keeps under specifications; however, transients become worse (Figure 14).

The other phenomenon observable in Figure 13 is the contraction of the region: the smaller the parameters, the narrower the region. The effect of this variation is related to the practical implementation of the PWM signal. As it is known, a digital PWM has always associated a determined resolution, which depends on the relation between the switching frequency and the internal clock frequency of the processor unit. In this case (Table III), each period $T=20\mu s$ is formed by $f_{clock}/f_s=1500$ cycles of the internal clock so that the respective resolution is $PWM_R=T/1500=0.0133\mu s$. Now, if it is decided to operate the buck converter by using a DE PWM scheme, switch S should turn on exactly at $(1-d_k)T/2$ after the beginning of the period. However, instant t_{ON} will actually occur when the processor counts for a number of cycles defined by the integer part of $(1-d_k)/2 \times 1500$. The maximum error between the ideal t_{ON} and the implemented one is precisely given by PWM_R.
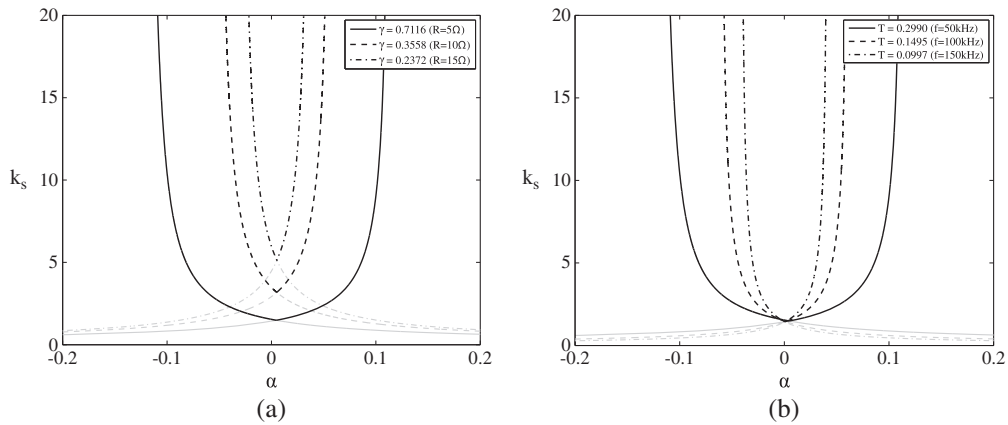

Figure 13. Changes of the optimum region as parameters deviate from their nominal quantities (a) Limit curves for different γ values; (b) Limit curves for different T values.
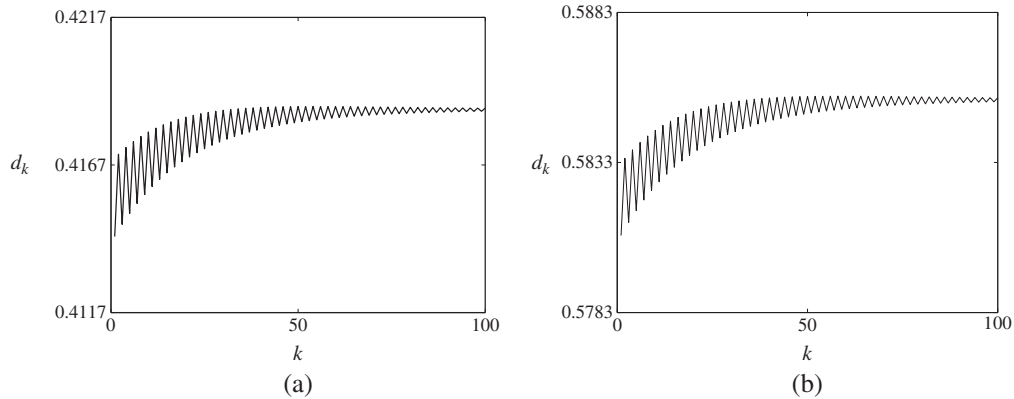

Figure 14. Evolution of d_k implementing the ZAD control with $k_s=5$, $R=10\Omega$, and $\alpha=0$. (a) $x_{2ref}=5/12$; (b) $x_{2ref}=7/12$.

In some sense, the real modulation signal sent to switch S can actually be interpreted as a new PWM defined by α values different from zero. The deviation with respect to the original DE PWM has a resolution of $\Delta\alpha = PWM_R/[(1 - d_{max})T/2] = 0.0133\mu s/1\mu s = 0.0133$. So, this means that the gain of the ZAD control should be chosen to guaranty stability not only for $\alpha = 0$ (DE PWM) but also for the α interval necessary to deal with the quantization variations given by the practical implementation of the DE PWM.

The optimum region corresponding to nominal T and γ values (Figure 9) results sufficiently wide to operate without inconvenience with quantization errors in the order of several times the minimal interval $\alpha \in [-0.0133, +0.0133]$. However, as T and γ are reduced, operation conditions can become critical for k_s gains commonly used. Thus, for example, it should be at least $k_s > 4.6$ for $R = 10\Omega$ ($\gamma = 0.3558$) and $k_s > 10.5$ for $R = 15\Omega$ ($\gamma = 0.2372$) to assure stability in the range $\alpha \in [-0.0133, +0.0133]$. As it has been mentioned, the k_s increase degrades necessarily the regulation. Furthermore, because PWM_R becomes worse as T is diminished, $\Delta\alpha$ could be even greater. In fact, for $T = 0.1495$ ($f_s = 100$ KHz), the minimal α interval increases twice.

It is worth mentioning that degeneracies mentioned in the previous section move to greater k_s values if parameters γ or T are decreased. This implies that the nonlinear scenario described earlier is developed for (α, k_s) combinations, which are rarely used. Thus, for example, considering the γ values of Figure 13(a), point $\sigma = 0$ occurs for $k_s > 20$ so that PD bifurcations are supercritical along all the curves depicted there.

5.2. Unmodeled dynamics of the switches

Nonlinear discrete-time models used to analyze the dynamics of dc-dc converters are derived by considering that switch S and diode D are ideal [7–9]. In practical implementations, these components introduce unmodeled dynamics into the system that could cause modifications in the expected performance. Most of the classical control laws are able to compensate differences. The digital version of the ZAD strategy, being essentially a static nonlinear law, can present some limitations to deal with perturbations.

To analyze the effects of physical switch and diode, the circuit was simulated by using the SimPower toolbox of Matlab. The electrical characteristics of the components were fixed according to the experimental prototype used as a reference. The specified values are the on resistance ($R_{onS} = 0.038\Omega$, $R_{onD} = 0.032\Omega$), the output capacitance ($C_{outS} = 430$pF, $C_{outD} = 310$pF), and the diode forward voltage ($V_{SD} = 0.5$ V).

In general, it is observed that the optimum region occurs for quite greater k_s magnitudes and regulation percentages become relatively worse. However, these variations do not produce substantial changes in the responses for control gains commonly chosen. Temporal evolutions of the system obtained by considering ideal and real components are compared in Figure 15. In the simulations, $\alpha = 0$ (DE PWM), $k_s = 5$, and the voltage reference takes the values $x_{2ref} = 5/12$
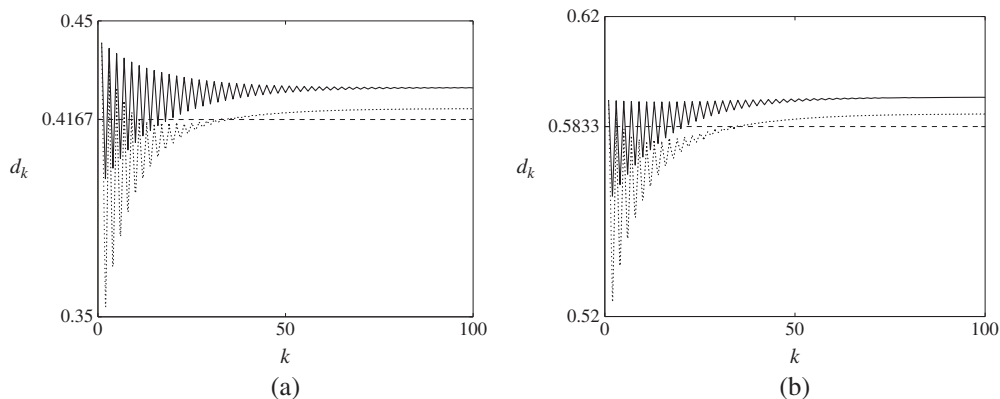

Figure 15. Evolution of d_k for $k_s = 5$, $\alpha = 0$ and considering real (solid line) and ideal (dotted line) components. (a) $x_{2ref} = 5/12$ ($v_o(0) = 4.70247$; $i_L(0) = 0.93091$); (b) $x_{2ref} = 7/12$ ($v_o(0) = 6.6273$; $i_L(0) = 1.3264$).

[Figure 15(a)] and $x_{2ref} = 7/12$ [Figure 15(b)]. In both cases, the unmodeled characteristics of the switch and the diode cause a tolerable degradation of the regulation and transients of the closed-loop system.

6. EXPERIMENTAL VALIDATION OF THE OPTIMUM REGION

The ZAD-strategy was tested in the standard laboratory prototype shown in Figure 16, which consists of a buck converter circuit, a kit ezdspTMF2812 of Spectrum Digital and an interface stage. The nominal values of input voltage, inductance, capacitor, and load resistance are those given in Table III; switch S and diode D are implemented by means of the integrated circuit IRF7901D1 containing a dual MOSFET plus a Schottky diode. Driver TPS2834 builds the necessary signals to command the transistors. Voltage and current signals are conditioned and sensed by using an operational amplifier LMC6484 and an instrumentation amplifier INA110.

To simplify the operations, the control law was programmed by using an IQMath library, which emulates floating point arithmetic on a fixed point processor unit. The format Q25 was chosen, which implies a precision of 30×10^{-9}. The time involved in the calculations was always less than $2\mu s$ (corresponding to the specified minimum duty cycle). The compare unit registers of the DSP Event Manager were set appropriately to reload the calculated d_k immediately, avoiding undesired delays in the feedback loop.

Figures 17 and 18 present the response of the experimental system when the voltage reference v_{ref} is varied from a specified value to 5 and 7 V, respectively. To validate the performance inside the optimum region, the DE PWM modulation and the control gain usually considered in the numerical simulations ($k_s = 5$) were chosen. The oscilloscope waveforms in Figure 17(a) and 18(a) correspond to the changes in the dc level of the output voltage (channel A) and to the input voltage (channel B). The first 100 samples of the output signal, stored in the DSP memory after the reference variation, are shown in Figure 17(b) and 18(b).

As it can be observed, there exists a reasonable agreement between measured and simulated curves. In all cases, simulations were obtained by considering the electrical characteristics of the switch and the diode (the values are detailed in Section 5.B). Steady-state error and transients exceed the specified values lightly. Nevertheless, from a qualitative point of view, responses pursue the predicted results given in Section 4.
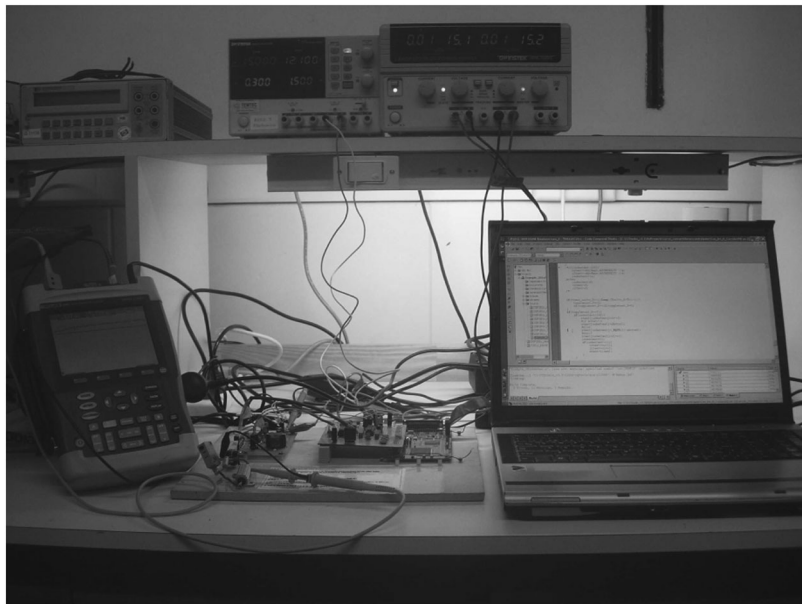

Figure 16. Standard laboratory prototype consisting of a buck converter, a kit ezdspTMF2812, and an interface stage.
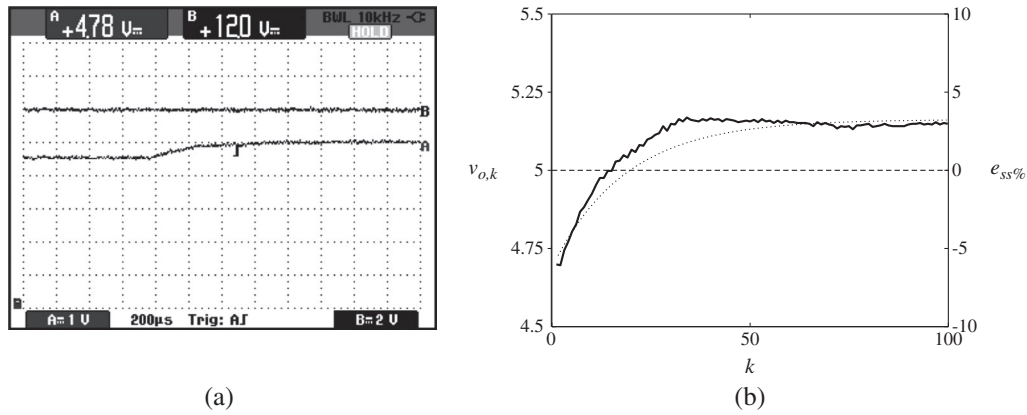
(a)

(b)

Figure 17. Experimental evolution of the ZAD control considering the DE PWM modulation, $k_s = 5$ and a desired output level of $v_{ref} = 5$ V. (a) Oscilloscope output voltage waveforms; (b) Comparison between experimental (solid line) and numerical (dotted line) results.

(a)

(b)

Figure 18. Experimental evolution of the ZAD control considering the DE PWM modulation, $k_s = 5$ and a desired output level of $v_{ref} = 7$ V. (a) Oscilloscope output voltage waveforms; (b) Comparison between the experimental (solid line) and numerical(dotted line) results.
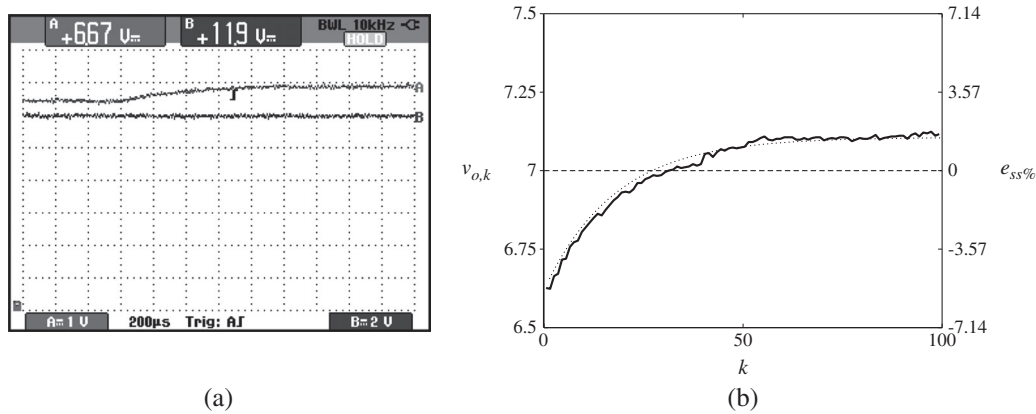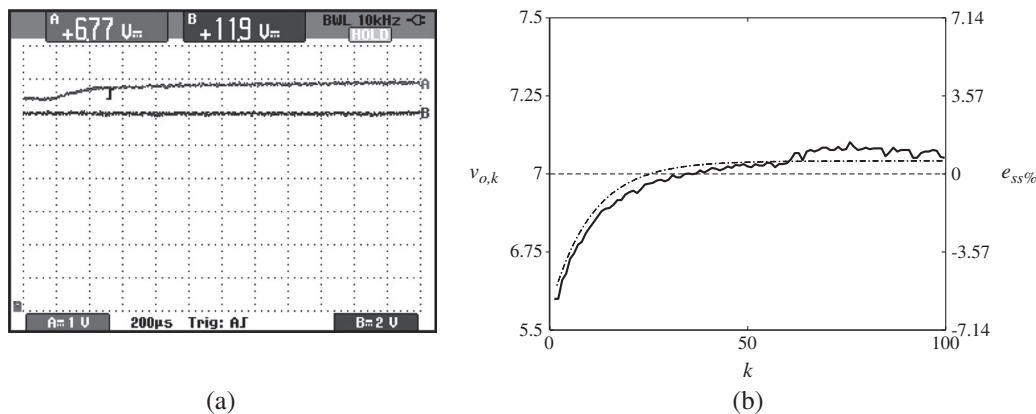

(a)

(b)

Figure 19. Experimental evolution of the ZAD control considering the DE PWM modulation, $k_s = 3$ and a desired output level of $v_{ref} = 7$ V. (a) Oscilloscope output voltage waveforms; (b) Comparison between the samples of the experimental (solid line) and numerical (dotted line) output voltages.

Finally, it was also verified that steady-state error can be improved by diminishing the control gain value. Thus, for example, Figure 19 depicts how the error corresponding to $v_{ref} = 7\,\text{V}$ is diminished considerably by fixing $k_s = 3$.

7. CONCLUSIONS

A generalized discrete-time model was used to analyze the performance of a ZAD-controlled buck converter under the variation of its intrinsic parameters as well as the pulse-width modulation signal. A detailed multiparameter study shows that the selected PWM can restrict the success of the nonlinear control law.

For implementations where the reference level is fixed, the best option is to choose traditional TE PWM or LE PWM. However, neither of both can be adopted deliberately. The first one is only appropriate for voltage references below middle range while the second one for references above middle range. For systems where variable reference levels are expected, the ZAD-strategy has to be necessarily associated to those PWM schemes determined by the optimum operation region. Among the possible signals, the DE PWM is a convenient alternative for these kinds of applications. Results also justify why the ZAD control is always used with this modulation.

Besides, the ZAD-strategy is a modified version of sliding mode control; it does not preserve all the presuppose characteristics. Numerical simulations show that the closed-loop system losses robustness under parameter perturbations or unmodeled dynamics of the switching components. In particular, the optimum region reduces as time constant γ or the switching period T is decreased. For a fixed control gain, the system can become unstable if the resulting α interval is comparable to the quantization noise of the digital PWM.

The nonlinear scenario inside the optimum region was also studied. It is displayed that dynamics can become complex due to the interaction of degenerate PD and CC bifurcations. However, the related phenomena are essentially impossible to detect in the applications because they imply parameter variations in the order of the forth or even sixth decimal place.

Experimental results were included to corroborate the expected performance of the system for different output voltages when the DE PWM is implemented. A reasonable agreement between measured curves and numerical findings was observed.

APPENDIX

A. The DE PWM case

As it can be inferred from (5), an operation of the buck converter with a DE PWM leads to a simplified ZAD control law. As $\alpha = 0$, (5) reduces to a first order polynomial on d_k, and the unique solution is given by the linear combination of the states

$$d_k = -\frac{2s_0 + \dot{s}_1 T}{k_s T}.$$

Finally, because d_k has to belong to the interval [0,1], it will be set

$$d_k = 0 \text{ if } -\frac{2s_0 + \dot{s}_1 T}{k_s T} < 0,$$

$$d_k = 1 \text{ if } -\frac{2s_0 + \dot{s}_1 T}{k_s T} > 1.$$

B. The general case

There are two possible solutions of (5) for $\alpha \neq 0$. One of them always leads to inadmissible duty cycle values. The other one is defined as

$$d_k = \frac{1+\alpha}{2\alpha} - \frac{\sqrt{k_sT(1+\alpha)^2 + 4\alpha(2s_0 + \dot{s}_1 T)}}{2\alpha\sqrt{k_sT}}. \tag{6}$$

The applicability of this control law is restricted to the verification of condition

$$k_sT(1+\alpha)^2 + 4\alpha(2s_0 + \dot{s}_1 T) > 0. \tag{7}$$

Two situations can be discriminated according to the α values.

(i) *Interval* $0 < \alpha \leq 1$. In this case, restriction (7) is equivalent to

$$-\frac{2s_0 + \dot{s}_1 T}{k_sT} \leq \frac{(1+\alpha)^2}{4\alpha}. \tag{8}$$

Now, as the d_k values has to belong to [0,1], it is also necessary to verify that

$$-\alpha \leq 1 - \sqrt{(1+\alpha)^2 + 4\alpha\frac{2s_0 + \dot{s}_1 T}{k_sT}} \leq \alpha.$$

Making some routine operations, this inequality reduces to

$$0 \leq -\frac{2s_0 + \dot{s}_1 T}{k_sT} \leq 1, \tag{9}$$

which is included into (8).

(ii) *Interval* $-1 \leq \alpha < 0$. Expression (7) can be rewritten as

$$\frac{(1+\alpha)^2}{4\alpha} \leq -\frac{2s_0 + \dot{s}_1 T}{k_sT}.$$

Then, to obtain d_k values inside the interval [0,1], it is also necessary to verify that

$$\alpha \leq 1 - \sqrt{(1+\alpha)^2 + 4\alpha\frac{2s_0 + \dot{s}_1 T}{k_sT}} \leq -\alpha,$$

which results again in (9).

To summarize, the ZAD control law (7) will be valid for any $\alpha \neq 0$ whenever condition (9) is verified. If not, the obtained d_k will result in a real number belonging to $(-\infty, 0) \cup (1, +\infty)$ or in a complex number. In the second case, the real part of d_k, given by $(1+\alpha)/2\alpha$, will be again greater than 1 for $0 < \alpha \leq 1$ or less than 0 for $-1 \leq \alpha < 0$. Therefore, it is possible to unify conditions and directly assume that

$$d_k = 0 \text{ if } -\frac{2s_0 + \dot{s}_1 T}{k_sT} < 0,$$

$$d_k = 1 \text{ if } -\frac{2s_0 + \dot{s}_1 T}{k_sT} > 1.$$

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