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Semi-conductors faults analysis in dual active bridge DC–DC converter

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Abstract: Failures in power semi-conductors of a dual active bridge converter are characterised considering open-circuit faults in diodes and transistors. A detailed electrical waveforms analysis to identify the main symptoms of the converter during normal and failure conditions is presented. Based on this analysis, a fault diagnosis strategy is proposed which is able to identify failures either in a diode or in a transistor as well as its location in the circuit. Finally, simulation and experimental results, using a prototype of 1 KW, are presented in this study to demonstrate the practical feasibility of the theoretical proposal.

1 Introduction

Hybrid electric systems, such as micro grids with high penetration of renewable energies, electric and hybrid electric vehicles (EV), aircraft, among others several applications, use more than one power sources (e.g. wind, photovoltaic panels, combustion engines), energy storage systems (e.g. batteries, super-capacitors, flywheels) and different loads, simultaneously [1–4]. Usually the rated voltages and currents of the components are different, which requires the use of power converters as interfaces with the aim to share a common dc or ac bus [1, 2].

Advances in power electronics and electrical drives have allowed replacing pneumatics and hydraulic actuators, as it is mentioned in [5, 6], in areas as diverse as agriculture and avionics applications. The main reasons for this replacements include more efficiency, lower costs, reduction in environment pollution, reduction in size and weight of the overall system and the possibility to include fault tolerance [7, 8].

For the applications mentioned above, and when a dc bus is used, DC–DC converters play an important role in adapting the different voltages and currents levels between the bus, the power sources and loads. In many cases, these converters need to operate in step-up or step-down voltage modes, and with the ability to perform bidirectional power flow control [9, 10].

Many bidirectional DC–DC topologies have been proposed to integrate different components in hybrid electric systems. For example, an extensive literature review is presented in [11], where the different electronic interfaces are grouped into standard, multilevel and multiport categories. Most of these relevant topologies and their main features are mentioned below.

A dual half bridge bidirectional DC–DC converter is proposed in [12] to be used as interface of the auxiliary power supply in EV applications. This topology presents significant advantages in these applications but requires a big capacitor bank, which could result in a heavy and bulky converter.

A non-isolated multiple input converter topology for the integration of various energy sources is proposed in [13]. As this topology can only perform unidirectional power flow control, it is not useful as an interface when bidirectional power flow control is required.

In [14] a super-capacitor energy storage system based on a bidirectional DC–DC converter for an electric vehicle is implemented. The transference of energy is optimised during regenerative braking and acceleration manoeuvres. As this topology does not require the use of a transformer, high power density can be achieved. Nevertheless, a large number of batteries and supercapacitors must be connected in series for high voltage applications.

The proposal presented in [15] uses a new generation of silicon carbide MOSFET devices for avionic power supply, which show feasibility to incorporate this new technology in order to develop interfaces with higher power density.

The dual active bridge (DAB) converter has been proposed for many applications for which bidirectional power flow control is required; for example in connecting a high voltage dc bus to a low voltage dc regenerative load [4, 16] or as an isolated DC–DC interface in high-power solid state transformers [17]. The DAB converter is a bidirectional topology composed of two active (full or half) bridges connected and isolated by a high-frequency transformer. It can step down or step up the output voltage, as a function of the converter parameters and the phase shift, as a DAB converter operates as a current source converter [10, 16]. In addition, the DAB converter allows achieving high efficiency because it is possible to operate its power semi-conductors under soft switching [18, 19]. These features make this converter an attractive topology for the applications previously mentioned.

Since power converters are designed to operate at certain power levels range, when a failure occurs in any component, it may not be able to operate at the power level required by loads at that moment. For this reason, reliability becomes a critical issue, especially for critical loads (i.e. space vehicles and power train in an electric vehicle, among others).

An overview of power electronic systems reliability is presented in [20]. In that work, three different situations are studied: (i) preventive reliability: the components prone to failure are replaced before their known mean time before failure, (ii) a logical reconfiguration of the system: fault tolerant schemes with no additional hardware, and (iii) reliability at the design stage: the design is reliable from its origin.

An industry-based survey concerning with reliability of power electronic converters was carried out among different users of aerospace, automation, automotive and electrical drives, among others [21]. The survey respondents agreed on that power semi-conductors are the most prone to failure components (31%),

followed by those of capacitors (17%) and gate driver circuits (15%). Failures associated with other components, such as sensors, inductors and coolers, are less likely to fail, and hence they can be neglected [20]. These results justify the necessity to incorporate a fault diagnosis scheme, which requires an in-depth study of the different failures that can occur in the power semi-conductors used in topologies for critical applications.

When a power semi-conductor presents a fault, overvoltage and/or over current anomalies may occur, which may cause damage to other components or even require the converter shutdown. For this reason, it becomes necessary to detect faults as early as possible to either perform a controlled shutdown, to avoid major damages, or reconfigure the topology when it is able to operate using a fault-tolerant scheme [22], even if this scheme does not ensures the converter full operating range.

Several strategies have been proposed aiming to detect and diagnose anomalies in power semi-conductors for different DC–DC topologies. For example, in [23, 24], open and short-circuit failures in full-bridge phase-shift (FBFS) and flyback DC–DC converters are studied and different strategies based on the analysis of voltage and current waveforms are proposed. These strategies are effective to detect a failure event, but they cannot identify which is the failed semi-conductor.

An open circuit fault diagnosis technique based on the voltage measured in a third winding of the transformer and a fault-tolerant scheme based on a logical reconfiguration of the switching sequence in an isolated FBFS DC–DC converter are proposed in [25]. In addition, an open-circuit fault diagnosis technique and fault-tolerant scheme for a three-level step-up converter in a photovoltaic power system is presented in [26]. This fault diagnosis method uses the voltages and currents measured to control the converter. The strategies presented in [25, 26] allow detecting faults in the transistors, but they cannot detect a fault in the freewheeling diodes.

In [27] a new fault diagnostic technique for a semi-conductor open-circuit fault in a neutral-point clamped three-level AC motor drive, based on the average current using Park's vector approach is presented. This approach allows detecting open-circuit faults in transistors grouped by pairs, but it is not possible the individual allocation of the faulty device.

In [28] a model-based on the open transistor fault diagnosis method is presented for a voltage-source inverter supplying a five-phase permanent magnet motor drive. This method uses an observer designed to estimate model parameters and it is able to detect multiple open switches or open phases faults. However, neither in [27] nor in [28] open circuit faults in free-wheeling diodes are considered nor detected.

The operation under fault conditions of a DAB converter is studied in [29], and a diagnosis method is proposed, based on the measurement of voltages at the transformer terminals. With these measurements, the authors propose a fault detector able to identify open-circuit failures in the transistors. However, individual failures in semi-conductors cannot be diagnosed due to the symmetry of the voltage waveforms of DAB converters.

In this paper, failures in power semi-conductors of a DAB converter are characterised considering open-circuit faults in diodes and transistors. A detailed waveforms analysis is presented to identify the main symptoms of the converter electrical variables for normal and failure conditions. To validate the theoretical analysis, simulation and experimental results are presented using a prototype of 1 kW. In addition, the basis for outlining a fault diagnosis strategy, able to identify failures either in a diode or in a transistor as well as its location in the circuit, is also proposed and validated through simulation results.

This paper is organised as follows: In Section 2, the DAB topology and its waveforms for normal operation are shown. In Section 3, voltage and current waveforms are analysed and the symptoms due to faults are deduced. Moreover, a fault detection and diagnosis scheme is proposed in this section. Section 4 presents some simulation results of failure detection and diagnosis scheme, whereas experimental results of the failures studied are presented and discussed in Section 5. Finally, conclusions are drawn in Section 6.

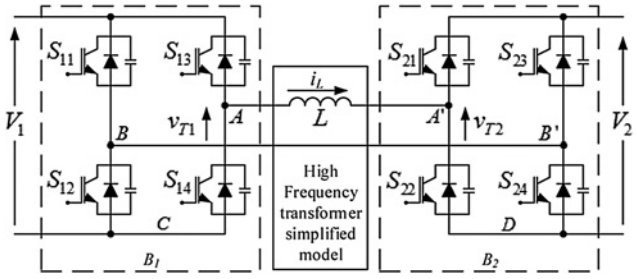

Fig. 1 *Simplified representation of the DAB topology*

2 DAB converter topology

A description of the DAB converter topology and its principle of operation is presented in this section.

The DAB topology is shown in Fig. 1. It consists of a full bridge working as a DC–AC converter feeding a high-frequency transformer, which supplies a second full bridge working as an AC–DC converter. As it can be observed in this figure, each switch, S_{xy}, is implemented by a power transistor, T_{xy}, (e.g. insulated gate bipolar transistor), a diode, D_{xy}, and a snubber capacitor, C_{xy}.

The analysis of the DAB converter can be simplified by referring the model to one side of the high-frequency transformer and considering its magnetising inductance much greater than its leakage inductance [30]. Therefore, the branch including the magnetising inductance can be considered as an open circuit and the converter is represented by a simplified scheme composed of two active full bridges linked by the transformer leakage inductance, L, as shown in Fig. 1. In this paper, to simplify the analysis, the transformer turns ratio will be considered hereinafter equal to 1.

The conventional modulation strategy consists on applying a phase-shift between the transformer voltages, v_{T1} and v_{T2}, with a constant frequency and 50% of duty cycle square waveform [30].

2.1 Principle of operation

Fig. 2 shows the voltage waveforms at the transformer terminals, v_{T1} and v_{T2}, and current, i_L, for steady-state operation of the converter, in step-down mode and soft switching conditions, when power flows from V_1 to V_2. In this figure, δ is the phase shift between v_{T1} and v_{T2}, and β is the zero-crossing angle of current i_L.

A detailed explanation of the operation principle can be found in [30]. A brief description of the working principle is presented below:

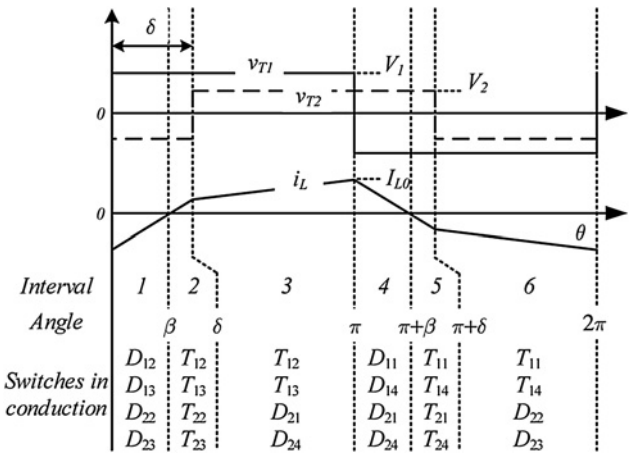

Fig. 2 *Waveforms of the DAB converter main variables for normal operation*

IET Power Electron., 2016, Vol. 9, Iss. 6, pp. 1103–1110

2.1.1 Interval 1: In the initial state, previous to $\theta = 0$, the current $i_L < 0$ has a negative slope established by $v_L = -V_1 + V_2$, flowing through T_{11}, T_{14}, $D_{22}y$ D_{23}, and the remaining switches are off. Fig. 2 shows that at $\theta = 0$, T_{11} and T_{14} are turned off under hard switching mode, and as consequence D_{12} and D_{13} start conducting naturally. Current $i_L < 0$ increases with a positive slope established by voltage $v_L = V_1 + V_2$. During this interval, the gate signals of T_{12}, T_{13}, T_{22} and T_{23} are on, however, due to current i_L is negative, it flows through D_{12}, D_{13}, D_{22} and D_{23}. This interval finishes when current i_L crosses zero at instant $\theta = \beta$.

2.1.2 Interval 2: At instant $\theta = \beta$, when the current i_L becomes positive, D_{12}, D_{13}, D_{22} and D_{23} go to blocking state, and T_{12}, T_{13}, T_{22} and T_{23} start conducting naturally, as their turn on signals where established in the previous interval. Current i_L increases with positive slope, and remains determined by $v_L = V_1 + V_2$. This interval finishes when the turn on signals of T_{21} and T_{24} are established at instant $\theta = \delta$.

2.1.3 Interval 3: At instant $\theta = \delta$, T_{22} and T_{23} are turned off under hard switching mode, and as consequence D_{21} and D_{24} start conducting naturally. Current $i_L > 0$ increases with a positive slope established by voltage $v_L = V_1 - V_2$, flowing through T_{12}, T_{13}, D_{21}, and D_{24}. This interval finishes when turn off signals are sent to T_{12} and T_{13} at instant $\theta = \pi$.

2.1.4 Interval 4: At instant $\theta = \pi$, T_{12} and T_{13} are turned off under hard switching mode, and as consequence D_{11} and D_{14} start conducting naturally. Current $i_L > 0$ decreases with a negative slope established by voltage $v_L = -V_1 - V_2$. During this interval, the turn on signals of T_{11}, T_{14}, T_{21} and T_{24} are established. However, due to current i_L is positive, it flows through D_{11}, D_{14}, D_{21} and D_{24}. This interval finishes when current i_L crosses zero at instant $\theta = \pi + \beta$.

2.1.5 Interval 5: At instant $\theta = \pi + \beta$, when the current i_L becomes negative, D_{11}, D_{14}, D_{21} and D_{24} go to blocking state, and T_{11}, T_{14}, T_{21} and T_{24} start conducting naturally, as their turn on signals where established in the previous interval. Current i_L increases with negative slope, still established by $v_L = -V_1 - V_2$. This interval finishes when the turn on signals of T_{21} and T_{24} are established at instant $\theta = \pi + \delta$.

2.1.6 Interval 6: At instant $\theta = \pi + \delta$, T_{21} and T_{24} are turned off under hard switching mode, and as consequence D_{22} and D_{23} start conducting naturally. Current $i_L < 0$ increases with a negative slope established by voltage $v_L = -V_1 + V_2$, flowing through T_{11}, T_{14}, D_{22}, and D_{23}. This interval finishes when turn off signals are sent to T_{11} and T_{14} at instant $\theta = 2\pi$.

2.2 Converter behaviour during switching process

Previous sections showed the converter behaviour during normal operation, assuming ideal and instantaneous switching process in the switches. However, this is not what happens in practice. In this section, the influence of blanking time during switching process is depicted.

To avoid short circuits in the DC bus, a blanking time is always necessary, which must be higher than the minimum time needed to completely turn the transistor off [16, 31]. In addition, to avoid over-voltage caused by parasitic inductances, a snubber capacitor may be present in parallel to every switch. The value of this capacitance is the resultant of two components: (i) snubber capacitance, and (ii) transistor output capacitance.

During the switching intervals, the parallel capacitors associated to each semi-conductor are charged/discharged whenever every time the switches are deactivated/activated, respectively [16]. These capacitors also provide a current path in case of some open-circuit faults.

Fig. 3 shows a simplified equivalent circuit valid to analyse the behaviour during blanking time. From Fig. 3, it is possible to determine the resonant frequency of the circuit, given by $f_0 = 1/2\pi\sqrt{LC}$, where $C = C_{11} + C_{12}$.

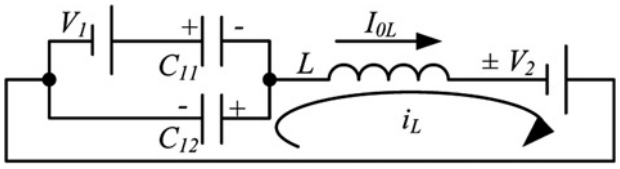

Fig. 3 *Simplified equivalent circuit for a bridge leg during blanking-time*

3 Fault analysis and detection

When a failure occurs, deformations in the transformer voltage and current waveforms may appear, since these waveforms are function of the switches in conduction state for each interval defined in Fig. 2.

An analysis of open-circuit faults in diodes and transistors of the DAB converter is presented next. This analysis determines the behaviour of the different faults, and allows outlining the principles of a fault detection scheme.

3.1 Analysis of open-circuit fault in diode D_{11}

Fig. 4 shows the waveforms for v_{T1}, v_{T2} and i_L, for a diode open-circuit fault. It is considered that before the interval $4F$, the DAB converter operates normally. Then, the symptoms related to fault in diode D_{11} appear. The shaded area in Fig. 4 shows these waveforms corresponding to an open-circuit fault in diode D_{11} at the instant the device should, but in fact, it does not start conducting.

Due to the diode D_{11} is open, and the current present in the circuit at the beginning of the interval $4F$ is different to zero, it flows by the snubber capacitors in parallel with each switch, as explained in Section 2.2. The voltage in capacitor C_{11} increases with negative slope until the zero crossing of the current i_L. Then, at the beginning of interval $5F$, the capacitors voltage reaches its maximum negative value, and starts decreasing with positive slope. These oscillations in capacitors voltage are reflected at transformer terminal v_{T1}.

In the worst case, the maximum over-voltage shown in Fig. 4 can be obtained by equalling the energies stored in the inductor and capacitors $\left(v_{C11_{\max}}\right)^2 C = \left(\frac{I_{0L-\max}}{2}\right)^2 L$, thus

$$v_{C11_{\max}} = \sqrt{\frac{L}{C}}\frac{I_{0L-\max}}{2} \tag{1}$$

where $I_{L0-\max}$ is function of the output power that the DAB converter transfers at the moment when the fault occurs, and the converter parameters. $I_{L0-\max}$ can be obtained using the following expression, obtained analysing the current and voltage waveforms at instant π [32],

$$I_{L0-\max} = \frac{V_1(2d\delta + \pi - d\pi)}{4\pi f_{sw} L} \tag{2}$$

where $d = V_2/V_1$ and f_{sw} is the switching frequency.

Using (1) and (2) it is possible to determine the minimum C_{xy} switching capacitance to limit the over-voltage across the transistor which is connected in parallel with the faulty diode.

Waveforms and switches in conduction state within intervals $5F$, $1F$, $2F$ and $3F$ under this fault condition are also shown in Fig. 4.

If the diode D_{11} fails when it is conducting, within the Interval 4, the current is transferred to capacitors. Therefore, over-voltage occurs on the inductor L at the instant when the fault occurs. Hereinafter, the evolution of the waveforms is similar as that shown in Fig. 4.

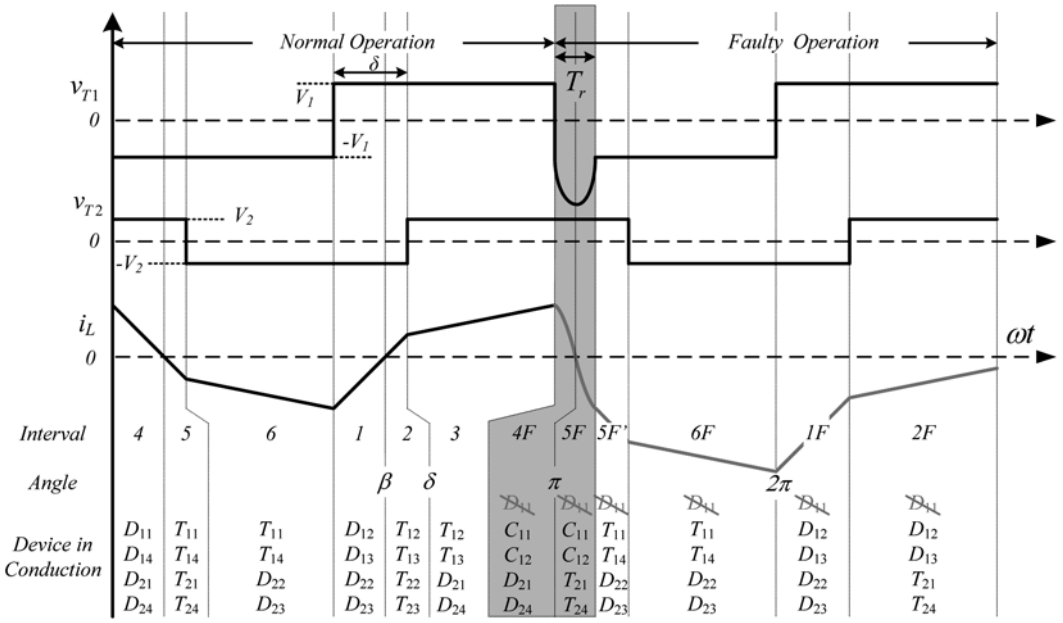

Fig. 4 *Waveforms of the DAB converter main variables for an open-circuit fault in diode D_{11} within Intervals 1, 2, 3, 5 or 6*

From the analysis and the waveforms shown in Fig. 4, it can be concluded that a diode open-circuit fault is characterised by an overvoltage, though limited by the snubber capacitor, at the transformer terminals on the side of the bridge containing the faulty device at the instant it should start conducting, plus a DC component in the inductor current. The period of this overvoltage can be estimated as $T_r = 1/2f_0$.

3.2 Analysis of open-circuit fault in transistor T_{11}

In this paper, it is assumed that a transistor fault can be caused by failures either in the transistor itself or in the gate driver circuit.

Fig. 5 shows waveforms for signals v_{T1}, v_{T2} and i_L, for open-circuit fault in T_{11}. Before the interval 5*F*, the DAB converter operates normally. Then, an open-circuit fault occurs in T_{11}. The shaded area in Fig. 5 shows the behaviour of voltage and current waveforms when the fault in T_{11} is present.

Under DAB normal operation conditions, current i_L becomes zero at the end of interval 4. Then, the converter starts operating in failure at the beginning of interval 5*F*, instant at which capacitor C_{11} is discharged while C_{12} is charged up to V_1.

Then, within interval 5*F*, it appears the resonant circuit shown in Fig. 3, charging C_{11} to the level of voltage V_1 and discharging C_{12} to zero volts.

As T_{14} is activated at the beginning of interval 4 and voltage at the capacitor C_{12} terminals is zero within interval 6*F*, then voltage v_{T1} becomes zero and current i_L starts decreasing linearly within this interval, since voltage at the inductance L terminals is equal to-V_2.

At the beginning of interval 7*F*, voltage on bridge B_2 is reversed, and then current i_L starts increasing linearly within the interval.

Interval 8*F* begins when the zero crossing of current i_L occurs, and a resonant circuit appears as shown in Fig. 3, discharging capacitor C_{11} and charging capacitor C_{12} to zero and V_1 voltage levels, respectively.

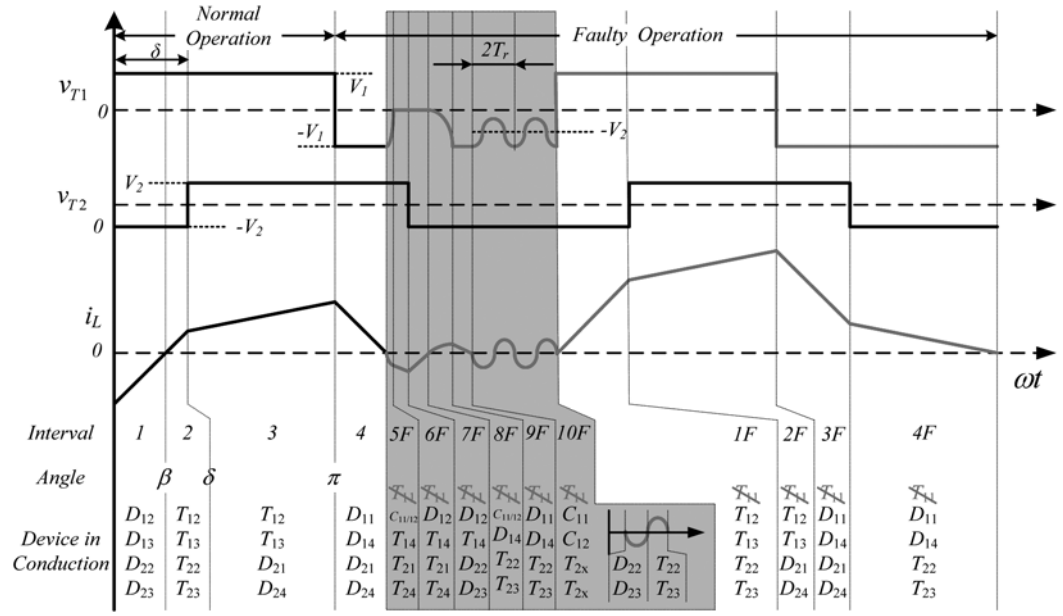

Fig. 5 *Waveforms of the DAB converter main variables for open-circuit fault in transistor T_{11} for Intervals 1, 2, 3, 5 or 6*

IET Power Electron., 2016, Vol. 9, Iss. 6, pp. 1103–1110

Table 1 Open-circuit faults in bridge B_1

Symptom/device	D_{11}	D_{12}	D_{13}	D_{14}	T_{11}	T_{12}	T_{13}	T_{14}
mean value of i_L	–	+	+	–	+	–	–	+
interval in which the failure appears in v_{T1}	4	1	1	4	5	2	2	5
interval in which the failure appears in v_{AC}	WD	WD	1	4	WD	WD	2	5
interval in which the failure appears in v_{BC}	4	1	WD	WD	5	2	WD	WD

WD: without deformation

At the beginning of interval $9F$, v_{C11} is zero and T_{14} is still activated, then the voltage v_{T1} is equal V_1. Therefore, voltage v_L in inductance L is equal $-(V_1 + V_2)$, and as a consequence, current i_L starts decreasing linearly.

At instant $10F$, current i_L becomes null and capacitor C_{12} is charged. Then, the resonant circuit results as the one shown in Fig. 3, in which the voltage v_{T1} and current i_L oscillate with sinusoidal waveforms. Voltage v_{T1} shown in Fig. 5, oscillates with a period and an amplitude given by $2T_r = 1/f_0$ and $(V_1 - V_2)$, respectively.

From this analysis, it can be concluded that the open circuit transistor faults are characterised by deformations and oscillations of the voltage waveform at the transformer terminals on the bridge containing the faulty device, plus a DC component in current i_L.

3.3 Analysis of short-circuit fault in switch S_{11}

A short-circuit failure may occur during S_{11} conduction (intervals 4, 5 or 6) or S_{11} blocking (intervals 1, 2 and 3). Symptoms appear at the instants when S_{11} should be in blocking state. In any case, the switch protection circuit should send a fault signal to prevent the destruction of S_{12}. Short-circuits are then not analysed in this work.

3.4 Conclusions and discussion from waveform analysis

A brief description of the fault situations analysed in the previous sections can be found below:

(i) Diode open-circuit fault: Over-voltage at the transformer terminals which amplitude is limited by means of the capacitor in parallel with the faulty diode and a DC component in current i_L.
(ii) Transistor open-circuit fault: As the resonant circuit appears between C_{11}, C_{12} and L, oscillations occur in voltage v_{T1} and i_L. Furthermore, a DC component appears in current i_L.

From the previous analysis and results, it can be observed the incidence of open-circuit faults in diode and transistor on voltage v_{T1}, at the terminals of the high-frequency transformer, and in the current i_L.

Table 1 summarises the instants defined in Fig. 2 for which appear deformations in the transformer voltage waveform for the different fault situations corresponding to bridge B_1. The pairs of switches D_{11}–D_{14}, D_{12}–D_{13}, T_{11}–T_{14} and T_{12}–T_{13} produce the same symptoms if only i_L and v_{T1} are considered. Something similar occurs for bridge B_2, only if v_{T2} and i_L are considered, as shown in Table 2.

With the aim of individualise the faulty device, it is proposed to measure the voltage at points A, B, A' B', C and D, represented in Fig. 1, to analyse the v_{AC} and v_{BC} waveforms for bridge B_1, and $v_{A'D}$ and $v_{B'D}$ waveforms for bridge B_2.

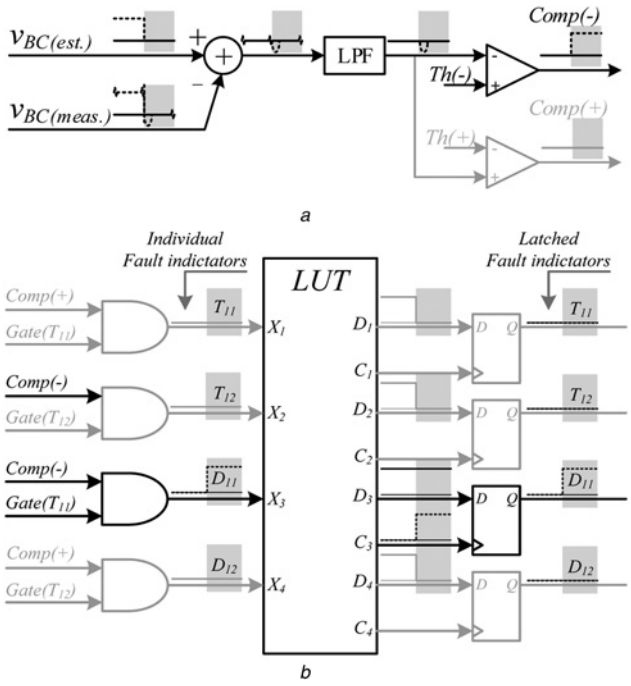

Fig. 6 *Fault diagnoser circuitry*

a Comparison stage of the fault diagnosis hardware
b Fault discriminator and latching stage

By analysing v_{AC} and v_{BC} waveforms, it can be observed that the deformations at the fault instants only affect one of the previously mentioned voltages, depending on the faulty device. Therefore, it is possible to identify the damaged semi-conductor by analysing the waveforms of v_{AC}, v_{BC} and i_L, for open-circuits faults in bridge B_1. On the other hand, Table 2 summarises the instants defined in Fig. 2 for which appear deformations in the transformer voltage waveform for the different fault situations corresponding to bridge B_2, and also those of $v_{A'C}$, $v_{B'C}$ and i_L, for open-circuit faults in bridge B_2.

3.5 Fault-detection and diagnosis scheme

This section presents a proposal for the detection and diagnosis of open-circuit faults in semi-conductors on bridge B_1 based on the measurement of voltages v_{AC} and v_{BC}.

The former explanation is presented for the open-circuit fault in S_{11} and S_{12}, corresponding to the measure of v_{BC}. The diagnosis for the faults in switches S_{13} and S_{14}, as well as the diagnosis of

Table 2 Open-circuit faults in bridge B_2

symptom/device	D_{21}	D_{22}	D_{23}	D_{24}	T_{21}	T_{22}	T_{23}	T_{24}
mean value of i_L	–	+	+	–	+	–	–	+
interval in which the failure appears in v_{T2}	3	6	6	3	5	2	2	5
interval in which the failure appears in $v_{A'D}$	3	6	WD	WD	5	2	WD	WD
interval in which the failure appears in $v_{B'D}$	WD	WD	6	3	WD	WD	2	5

faults in bridge B_2 are analog to the presented below, and then are not presented due to space reasons.

The diagnosis hardware is composed by two stages:

(i) The comparison stage.
(ii) The fault discriminator stage.

Fig. 6*a* shows the circuit of the comparison stage. The circuit function is to subtract the measured signal v_{BC} ($v_{BC(\text{meas.})}$) from an estimation of the same signal, $v_{BC(\text{est.})}$. The estimation $v_{BC(\text{est.})}$ is obtained using the measure of V_1 and the PWM signals of bridge B_1.

The result of this subtraction is then low-pass filtered (LPF) in order to eliminate switching noise that could be present in the signal. The output of the LPF block is then compared with a positive threshold, $Th(+)$, and a negative threshold, $Th(-)$.

The comparator output $Comp(+)$ will be activated if an open-circuit fault is present in D_{12} or T_{11}, whereas $Comp(-)$ will be activated if an open-circuit fault is present in D_{11} or T_{12}.

$Comp(+)$ and $Comp(-)$ and PWM signals for bridge B_1 are then connected to an array of four AND gates, whose outputs generate the individual-fault indicators, as shown in Fig. 6*b*. These signals are then passed through a logic function that prevents a false fault triggers once the primary fault is diagnosed. For example, the outputs D_1/C_1 are: $D_1 = \overline{(\overline{X_3}X_2 + X_3\overline{X_2} + \overline{X_1}X_4)}$ and $C_1 = \overline{X_1}X_4$.

Finally, the fault indicators are latched at the output of the device.

In Figs. 6*a* and 6*b* are highlighted the signal paths for an open-circuit fault in D_{11}.

A similar scheme is proposed for bridge B_2 of the DAB topology, based on measurements of $v_{A'C}$, $v_{B'C}$, V_2 and the switch activation signals in bridge B_2. This completes the fault-diagnosis scheme proposed for all the power semi-conductors of the DAB converter.

It must be noted that thresholds $Th(+)$ and $Th(-)$ cannot be set arbitrarily. In desaturation protection used in some driver circuitry, a value between 6 and 7 volts is used to determine if the switch is working properly [33]. In a first approach, it could be set the values $Th(+) = 7\ V$ and $Th(-) = -7\ V$.

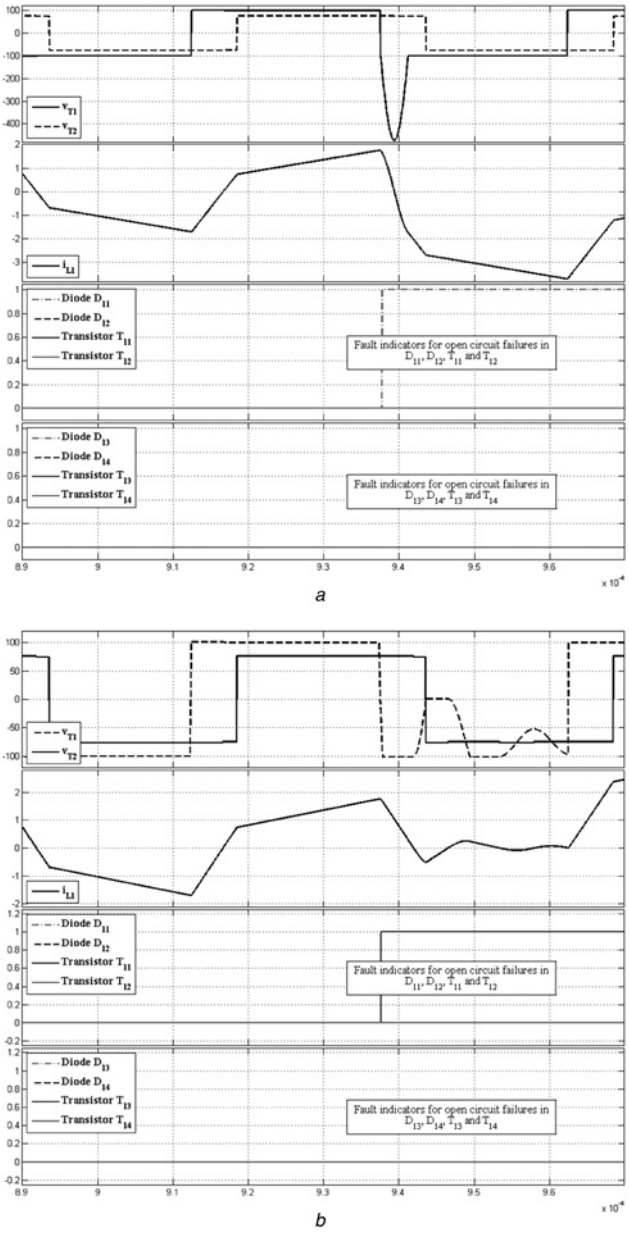

Fig. 7 *Simulation results waveforms of fault diagnoser*

a Diode D_{11} open circuit fault and properly detection
b Transistor T_{11} open circuit fault and properly detection

Table 3 DAB converter parameters

V_1	100 V
V_2	75 V
L	438.11 μH
C_{xy}	1.3 nF
$P_{0\ (\max)}$	1 kW
δ	43.2°

4 Fault diagnoser simulation results

To validate the proposed fault-diagnosis strategy, in this section are presented simulation results of the fault diagnoser. A DAB converter with a switching frequency of 20 Khz, $V_1 = 100\ V$, $V_2 = 75\ V$, $C_{xy} = 1.3\ nF$ and $L = 438$ μF was simulated under normal and faulty operation.

Fig. 7*a* shows the main waveforms of the DAB converter when a D_{11} diode open-circuit failure occurs. In this figures v_{T1}, v_{T2} and i_{L1} are depicted in the upper two subfigures, while the two remaining subfigures show the fault indicators of all B_1 switches.

The converter operates normally until $t = 0.93$ ms, when the diode D_{11} presents an open-circuit fault condition. As explained earlier, the device will show the fault symptoms when it must start conducting. In this case, it happens when v_{T1} changes from V_1 to $-V_1$. As Fig. 7*a* shows, the fault diagnoser indicates the presence of the fault.

Fig. 7*b* shows the main waveforms of the DAB converter when a T_{11} transistor open-circuit failure occurs. In this figure v_{T1}, v_{T2} and i_{L1} are depicted in the upper two subfigures, while the two remaining subfigures show the fault indicators of all B_1 switches.

The converter operates normally until $t = 0.93$ ms, when the transistor T_{11} presents an open-circuit fault condition. As explained earlier, the device will show the failure symptoms when it must start conducting. In this case, it happens when v_{T1} changes from V_1 to $-V_1$ and the current i_{L1} becomes negative. As Fig. 7*b* shows, the fault diagnoser indicates the presence of the fault immediately, and the other fault indicators are not affected.

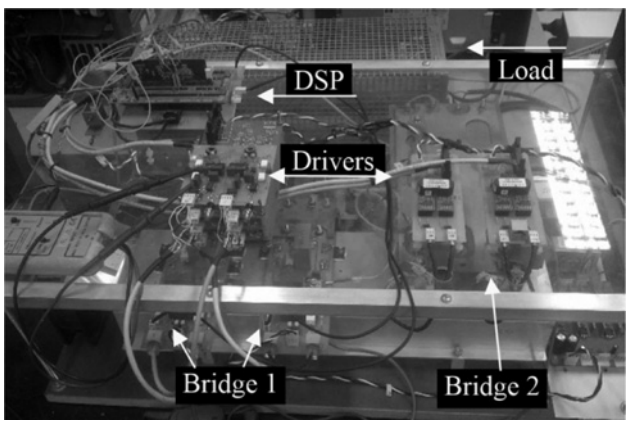

Fig. 8 *Experimental setup*

5 Experimental results

To validate the previous analysis, in this section some experimental results are presented.

The parameters of the DAB converter are resumed in Table 3. Fig. 8 shows a photograph of the actual prototype. As shown in Table 3, experimental results are obtained under low voltage and current levels to avoid damage in the converter components. The obtained results are discussed below.

5.1 Experimental results of open-circuit fault in diode D_{11}

Fig. 9*a* shows voltage v_{T1} and v_{T2} and current i_L waveforms when an open-circuit failure occurs in D_{11}.

Diode D_{11} is conducting normally until time t_0, when an open-circuit fault occurs. However, as discussed earlier, the symptoms associated to this fault will appear at the instant that D_{11} must start conducting, that is, when current should be transferred from T_{12}, at instant of t_1.

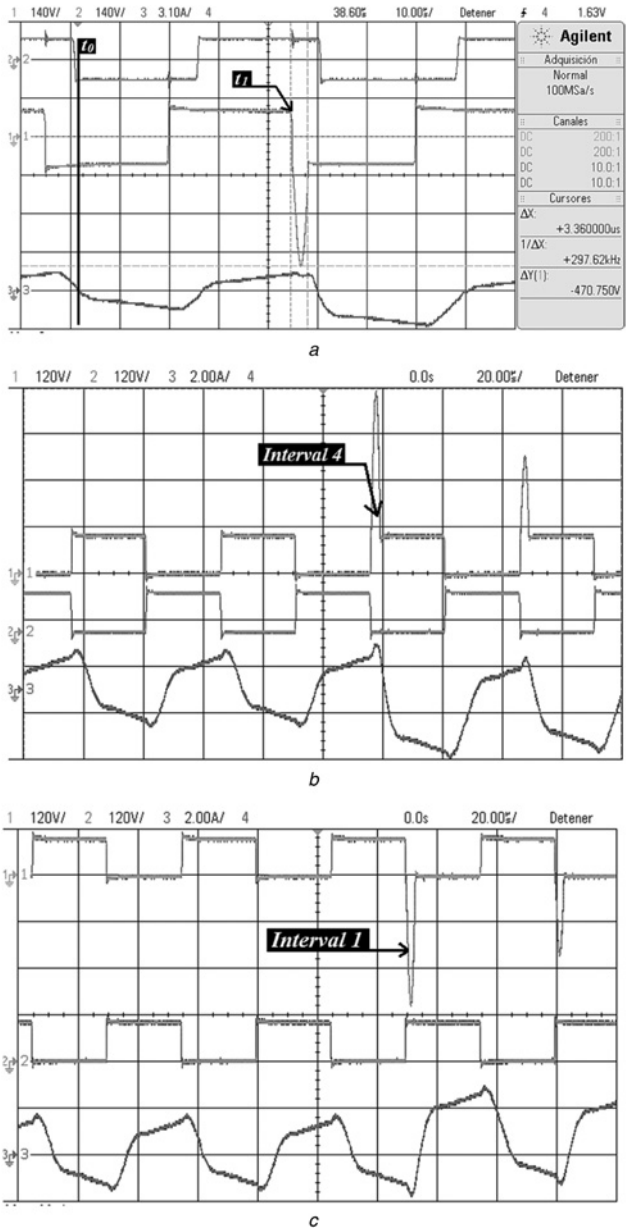

Fig. 9 *Experimental waveforms of a diode D_{11} open-circuit failure*

a Detail of v_{T1} over-voltage. Ch1 = v_{T1}, Ch2 = v_{T2}, Ch3 = i_L
b Experimental waveforms of a diode D_{11} failure. Ch1 = v_{BC}, Ch2 = v_{AC}, Ch3 = i_L
c Experimental waveforms of a diode D_{12} failure. Ch1 = v_{BC}, Ch2 = v_{AC}, Ch3 = i_L

In Fig. 9*a* shows the duration and the amplitude of the over-voltage (half-sinusoidal waveform) at v_{T1} terminals, being $\Delta X = T_r = 1/2f_0 = 3.36$ μs and $\Delta Y = 470.75$ V, respectively.

T_r can be calculated as follows

$$T_r = \frac{1}{2f_0} = \Delta X = \pi\sqrt{L(C_{11} + C_{12})} = 3.353\,\mu\text{s} \tag{3}$$

Whereas, the peak over-voltage in v_{T1} can be calculated using (1) and (2), then

$$\Delta Y = v_{C11_{\max}} + V_1 = 463.31\,\text{V} \tag{4}$$

The comparison of the calculated values with the measured ones shows that the results obtained are consistent with the previous analysis.

Fig. 9*b* shows v_{BC}, v_{AC} voltages and i_L current waveforms when an open circuit fault occurs in D_{11}, while Fig. 9*c* shows the same

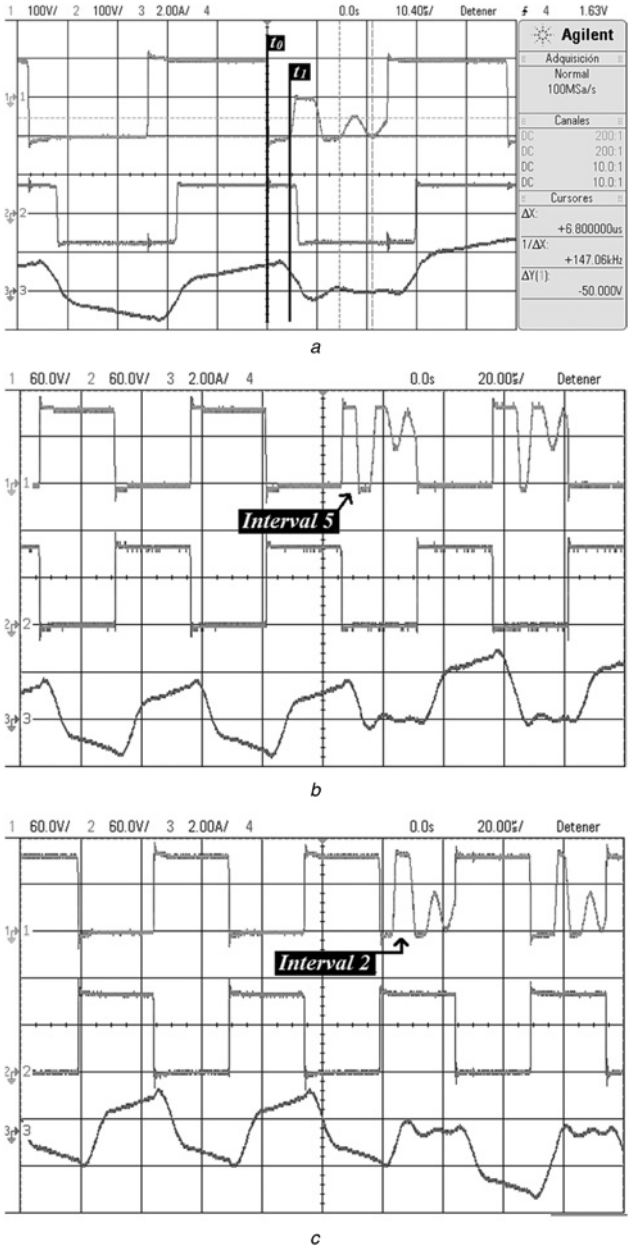

Fig. 10 *Experimental waveforms of a transistor T_{11} failure*

a Detail of voltage and current deformations. Ch1 = v_{T1}, Ch2 = v_{T2}, Ch3 = i_L
b Experimental waveforms of a transistor T_{11} failure. Ch1 = v_{BC}, Ch2 = v_{AC}, Ch3 = i_L
c Experimental waveforms of a transistor T_{12} failure. Ch1 = v_{BC}, Ch2 = v_{AC}, Ch3 = i_L

variables for an open circuit fault occurs in D_{12}. These figures show the occurrence of open circuit failures in D_{11} and D_{12} in different intervals, as it was explained in Section 3.4. This differentiation allows a fault detection and diagnosis scheme to be proposed, since the fault symptoms are well differentiated.

5.2 Experimental results of open-circuit fault in transistor T_{11}

Fig. 10*a* shows voltage v_{T1} and v_{T2} and current i_L waveforms when an open-circuit failure occurs in T_{11}, before it start conducting.

At t_0 the transistor T_{11} fails, remaining permanent in open-circuit. The failure symptoms will appear when the current i_L should be transferred from D_{11} to T_{11}, that is, at instant t_1.

In Fig. 10*a* is shown the period and the amplitude of the sinusoidal oscillations at v_{T1} terminals, being $\Delta X = 2T_r = 1/f_0 = 6.8$ μs and $\Delta Y = 50$, respectively.

$2T_r$ can be calculated as follows

$$2T_r = \Delta X = \frac{1}{f_0} = \pi\sqrt{L(C_{11} + C_{12})} = 6.7059\,\mu\text{s} \tag{5}$$

Whereas, ΔY can be calculated as follows

$$\Delta Y = 2\left(V_1 - V_2\right) = 2(100\,\text{V} - 75\,\text{V}) = 50\,\text{V} \tag{6}$$

The comparison of the calculated values with the measured ones shows that the results obtained are consistent with the previous analysis.

Fig. 10*b* shows v_{BC}, v_{AC} voltages and i_L current waveforms when an open circuit fault occurs in T_{11}, while Fig. 10*c* shows the same variables for an open circuit fault occurs in T_{12}. These figures show the occurrence of open circuit failures in T_{11} and T_{12} in different intervals, as it was explained in Section 3.4. This differentiation will allow proposing and completing a fault detection and diagnosis scheme, since the fault symptoms are well differentiated.

6 Conclusions

A dual active bridge DC–DC converter was analysed under normal and failure operating conditions of the power semi-conductors.

A complete analysis of the main waveforms of the converter was also presented. This analysis allows identifying the main symptoms of the converter when open-circuit faults in diodes and transistors are present.

It can be concluded that an open-circuit fault in a diode produces an overvoltage and a DC current component at the transformer terminals connected to the bridge containing the faulty device. Moreover, an open-circuit fault in a transistor produces deformation and oscillation in the voltage as well as a DC current component at the transformer terminals connected to the bridge containing the faulty device.

The transformer current, i_L, allows detecting a fault, but it does not allow identifying the faulty device and its location in the circuit. However, the analysis of voltage drop across the bottom switches, v_{AC} and v_{BC}, in bridge B_1, and $v_{A'D}$ and $v_{B'D}$ in bridge B_2, shows that are an enough information to determine and identify the faulty semi-conductor.

The analysis and conclusions presented above, allow propose a fault-detection scheme.

Finally, simulation and experimental results using a 1-KW prototype were presented in this paper. These results demonstrate and validate the practical feasibility of the theoretical proposal.

7 References

1 Luo, S.: 'A review of distributed power systems part I: DC distributed power system', *IEEE Aerosp. Electron. Syst. Mag.* , 2005, **20**, (8), pp. 5–16

2 Luo, S., Batarseh, I.: 'A review of distributed power systems. Part II. high frequency AC distributed power systems', *IEEE Aerosp. Electron. Syst. Mag.*, 2006, **21**, (6), pp. 5–14

3 Mansour, A., Faouzi, B., Jamel, G., *et al.*: 'Design and analysis of a high frequency DC–DC converters for fuel cell and super-capacitor used in electrical vehicle', *Int. J. Hydrog. Energy*, 2014, **39**, (3), pp. 1580–1592

4 Naayagi, R.T., Forsyth, A.J., Shuttleworth, R.: 'Bidirectional control of a dual active bridge DC–DC converter for aerospace applications', *IET Power Electron.*, 2012, **5**, (7), pp. 1104–1118

5 Emadi, A., Ehsani, M.: 'Aircraft power systems: technology, state of the art, and future trends', *IEEE Aerosp. Electron. Syst. Mag.*, 2000, **15**, (1), pp. 28–32

6 Florentsev, S., Izosimov, D., Makarov, L., *et al.*: 'Complete traction electric equipment sets of electro-mechanical drive trains for tractors'. 2010 IEEE Region 8 Int. Conf. on Computational Technologies in Electrical and Electronics Engineering (SIBIRCON), 2010, pp. 611–616

7 Boglietti, A., Cavagnino, A., Tenconi, A., *et al.*: 'The safety critical electric machines and drives in the more electric aircraft: a survey'. 35th Annual Conf. of IEEE Industrial Electronics, 2009. IECON '09, 2009, pp. 2587–2594

8 Rosero, J.A., Ortega, J.A., Aldabas, E., *et al.*: 'Moving towards a more electric aircraft', *IEEE Aerosp. Electron. Syst. Mag.*, 2007, **22**, (3), pp. 3–9

9 Sedaghati, F., Hosseini, S.H., Sabahi, M., *et al.*: 'Extended configuration of dual active bridge DC-DC converter with reduced number of switches', *IET Power Electron.*, 2015, **8**, (3), pp. 401–416

10 Sedaghati, F., Hosseini, S.H., Sabahi, M., *et al.*: 'Analysis and implementation of a modular isolated zero-voltage switching bidirectional dc-dc converter', *IET Power Electron.*, 2014, **7**, (8), pp. 2035–2049

11 Pires, V.F., Romero-Cadaval, E., Vinnikov, D., *et al.*: 'Power converter interfaces for electrochemical energy storage systems – A review', *Energy Convers. Manage.*, 2014, **86**, pp. 453–475

12 Li, H., Peng, F.Z.: 'Modeling of a new ZVS bi-directional dc-dc converter', *IEEE Trans. Aerosp. Electron. Syst.*, 2004, **40**, (1), pp. 272–283

13 Kumar, L., Jain, S.: 'Multiple-input DC-DC converter topology for hybrid energy system', *IET Power Electron.*, 2013, **6**, (8), pp. 1483–1501

14 Dixon, J.W., Ortuzar, M.E.: 'Ultracapacitors + DC-DC converters in regenerative braking system', *IEEE Aerosp. Electron. Syst. Mag.*, 2002, **17**, (8), pp. 16–21

15 De, D., Castellazzi, A., Lopez-Arevalo, S., *et al.*: 'SiC MOSFET based avionic power supply'. Seventh IET Int. Conf. on Power Electronics, Machines and Drives (PEMD 2014), 2014, pp. 1–6

16 Kheraluwala, M.N., Gascoigne, R.W., Divan, D.M., *et al.*: 'Performance characterization of a high-power dual active bridge DC-to-DC converter', *IEEE Trans. Ind. Appl.*, 1992, **28**, (6), pp. 1294–1301

17 Zhang, R., Wang, D., Mao, C., *et al.*: 'Dual active bridge synchronous chopper control strategy in electronic power transformer', *IET Electr. Power Appl.*, 2014, **8**, (3), pp. 88–97

18 Oggier, G.G., García, G.O., Oliva, A.R.: 'Analysis of the influence of switching related parameters in the DAB converter under soft-switching', *Latin Am. Appl. Res.*, 2013, **18**, pp. 121–129

19 Piris-Botalla, L., Oggier, G.G., Airabella, A.M., *et al.*: 'Power losses evaluation of a bidirectional three-port DC–DC converter for hybrid electric system', *Int. J. Electr. Power Energy Syst.*, 2014, **58**, (0), pp. 1–8

20 Song, Y., Wang, B.: 'Survey on reliability of power electronic systems', *IEEE Trans. Power Electron.*, 2013, **28**, (1), pp. 591–604

21 Yang, S., Bryant, A., Mawby, P., *et al.*: 'An industry-based survey of reliability in power electronic converters', *IEEE Trans. Ind. Appl.*, 2011, **47**, (3), pp. 1441–1451

22 Khan, F.H., Tolbert, L.M.: 'Bi-directional power management and fault tolerant feature in a 5-kW multilevel dc-dc converter with modular architecture', *IET Power Electron.*, 2009, **2**, (5), pp. 595–604

23 Nie, S., Chen, Y., Pei, X., *et al.*: 'A DSP-based diagnostic system for DC-DC converters using the shape of voltage across the magnetic components', IEEE Energy Conversion Congress and Exposition (ECCE), 2010, pp. 1908–1915

24 Kim, S.Y., Nam, K., Song, H.-S., *et al.*: 'Fault diagnosis of a ZVS DC-DC converter based on DC-link current pulse shapes', *IEEE Trans. Ind. Electron.*, 2008, **55**, (3), pp. 1491–1494

25 Pei, X., Nie, S., Chen, Y., *et al.*: 'Open-circuit fault diagnosis and fault-tolerant strategies for full-bridge DC-DC converters', *IEEE Trans. Power Electron.*, 2012, **27**, pp. 2550–2565

26 Ribeiro, E., Cardoso, A.J.M., Boccaletti, C.: 'Fault-tolerant strategy for a photovoltaic DC–DC converter', *IEEE Trans. Power Electron.*, 2013, **28**, (6), pp. 3008–3018

27 Santos Mendes, A.M., Abadi, M.B., Cruz, S.M.A.: 'Fault diagnostic algorithm for three-level neutral point clamped AC motor drives, based on the average current park's vector', *IET Power Electron.*, 2014, **7**, (5), pp. 1127–1137

28 Salehifar, M., Arashloo, R.S., Moreno-Eguilaz, M., *et al.*: 'Observer-based open transistor fault diagnosis and fault-tolerant control of five-phase permanent magnet motor drive for application in electric vehicles', *IET Power Electron.*, 2015, **8**, (1), pp. 76–87

29 Ribeiro, E., Cardoso, A.J.M., Boccaletti, C.: 'Fault analysis of dual active bridge converters'. in IECON 2012 – 38th Annual Conf. on IEEE Industrial Electronics Society, 2012, pp. 398–403

30 De Doncker, R., Divan, D.M., Kheraluwala, M.H.: 'A three-phase soft-switched high-power-density DC/DC converter for high-power applications', *IEEE Trans. Ind. Appl.*, 1991, **27**, (1), pp. 63–73

31 Mohan, N.: 'Power electronics. converters, application and design' (John Wiley & Sons, Inc., 2003, 3rd edn)

32 Oggier, G.G., García, G.O., Oliva, A.R.: 'Switching control strategy to minimize dual active bridge converter losses', *IEEE Trans. Power Electron.*, 2009, **24**, (7), pp. 1826–1836

33 Wu, Y., Sun, Y., Lin, Y.: 'Analysis and discussion of false triggering of Vce desaturation protection circuit in a T-type neutral point clamped inverter and its solutions', *IET Power Electron.*, 2014, **7**, (9), pp. 2242–2249