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Control of a three-stage medium voltage solid-state transformer

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ABSTRACT

This paper proposes the modeling and control of a Solid-State Transformer using a three-stage conversion topology. First, a rectification stage is used, where a three-phase high-voltage AC signal is converted to a DC level; this stage is then followed by a DC-DC converter, and finally an inverter is used to convert the DC into a three-phase low-voltage AC signal. The adopted topology is modeled using a simplified model for each stage, useful to design their controllers. Based on these models, the controllers are tuned to obtain a good performance to sudden load changes. This performance is tested through simulations.

1 Introduction

It is necessary to mention that this paper is an extension of work originally presented in [1]. This extension includes a detailed description of the proposed models and controllers. These models are used for tuning the controller parameters in order to obtain good performance in presence of sudden load changes.

Solid-State Transformers (SST) are emerging as a new technology capable of replacing power distribution transformers [2]. It is expected that the next generation of the power distribution transformers is based on power electronics semiconductor devices [3]. By using these semiconductors, it is possible to design an apparatus based on power converters with smaller and lighter high-frequency transformers. In this way, it is possible to obtain a smaller and lighter distribution transformer when compared with a traditional transformer of the same power rating. Roughly speaking, SSTs work as follows. In a first stage a sinusoidal signal of, typically, 50 or 60 Hz is converted to a high-frequency signal. Then, the amplitude of this signal is changed, by using a small high-frequency transformer, and finally in a third stage a new signal of the same frequency as the input signal but different amplitude is obtained.

Several topologies for the SST can be found in the literature, with their advantages and disadvantages [4]. In addition, it is possible to find some reviews dealing with the subject [5, 6]. Applications in transportation and smart grid can be found in [7]; whereas a topology based on SiC devices can be found in [8]. Also, a traditional transformer and an SST were compared in [9], and a procedure to obtain a detailed model of an SST topology can be found in [10].

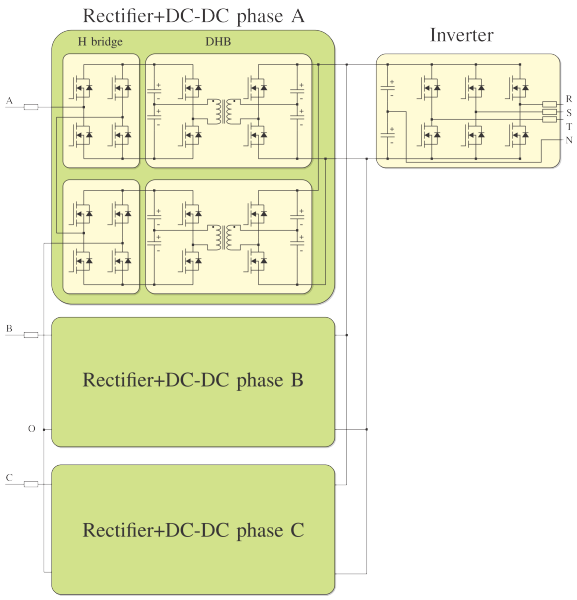

Figure 1: SST topology.

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A three-stage SST is considered in this paper [7]. Its topology is shown in Figure 1. The three stages are: a rectification stage, where a three-phase high voltage (HV) AC grid voltage is converted to a DC signal, a DC-DC converter stage (multiple stages in parallel) that provides isolation and performs the level adaptation, and finally, an inverter stage that converts the DC signal into a three-phase low voltage (LV) AC sinusoidal wave.

In this paper, simple models for each stage are proposed. Using these models, the required controllers are designed and their parameters are tuned to obtain a good performance in presence of sudden load changes. In order to test the performance of the proposed controllers, simulations results are introduced.

2 Proposed SST topology and model

Figure 2 shows a general diagram of the chosen topology. The SST is composed of a bidirectional multi-level HV three-phase converter, labeled Rectifier, six bidirectional isolated DC-DC converters, labeled DHB1 through DHB6, and a bidirectional LV three-phase converter with neutral, labeled Inverter. This topology has a great degree of modularity, allowing to consider the converters as decoupled systems and simplifying the design of the controllers [7].

Each converter and its simplified model is described below. Since the controllers are implemented using digital control techniques, the models are described in discrete time, assuming a sampling time T_s.

2.1 Rectifier

The rectifier is a three-phase AC-DC converter connected to the HV grid. As shown in Figure 2, the rectifier input port is modeled as a three-phase controlled voltage source $v_{rec} = [v_{reca}\ v_{recb}\ v_{recc}]^T$, coupled to the HV grid voltage $v_{hv} = [v_{hva}\ v_{hvb}\ v_{hvc}]^T$ through an inductor with current $i_{hv} = [i_{hva}\ i_{hvb}\ i_{hvc}]^T$. This coupling filter is modeled using complex vector notation (see Appendix). The zero order hold (zoh) discrete time model of the coupling filter results:

$$\vec{i}_{hv}[k+1] = \frac{T_s}{L_{rec}}\left(\bar{\vec{v}}_{hv}[k] - \vec{v}_{rec}[k]\right) + \vec{i}_{hv}[k], \qquad (1)$$

where $\bar{\vec{v}}_{hv}[k] = 0.5(\vec{v}_{hv}[k+1] + \vec{v}_{hv}[k])$ is the mean value of the HV grid voltage in the time interval $T_s k$, $T_s(k+1)$.

The output ports of the rectifier are modeled as current sources i_{iX}, with $X = 1\ldots6$. These currents are computed through power balance. Considering that both H bridges of each phase of the rectifier are given the same reference, it can be found that their currents are equal:

$$i_{i1}[k] = i_{i2}[k] = \frac{v_{reca}[k] i_{hva}[k]}{V_{busH1}[k] + V_{busH2}[k]}, \qquad (2)$$

$$i_{i3}[k] = i_{i4}[k] = \frac{v_{recb}[k] i_{hvb}[k]}{V_{busH3}[k] + V_{busH4}[k]}, \qquad (3)$$

$$i_{i5}[k] = i_{i6}[k] = \frac{v_{recc}[k] i_{hvc}[k]}{V_{busH5}[k] + V_{busH6}[k]}. \qquad (4)$$

Note that in this rectifier model, the independent variables (control inputs) are the three-phase components of $v_{rec}[k]$.

2.2 Dual Half Bridge (DHB)

Since there are six isolated DC buses in the rectifier, there are six DC-DC converters which are implemented using the DHB topology, which are modeled as current sources. The coupling between the output ports of the rectifier and the input port of each DHB is performed through a capacitor. The voltage across each of these capacitors is modeled through the difference equation:

$$V_{busHX}[k+1] = \frac{T_s}{C_H/2}\left(i_{iX}[k] - i_{oX}[k]\right) + V_{busHX}[k], \qquad (5)$$

with $X = 1\ldots6$. The DHBs themselves are controlled using a phase shift strategy. Therefore, each converter can be modeled through the algebraic equation for their average power transfer [11]:

$$P_{dhbX}[k] = \frac{V_{busHX}[k]\ m V_{busL}[k] \delta_X[k]\left(\pi - |\delta_X[k]|\right)}{8\pi^2 L_d f_{sw}^{dhb}}, \qquad (6)$$

where m is the DHB transformer relation, L_d is the total leakage of the transformer referred to the HV side, f_{sw}^{dhb} is the switching frequency of the DHB converter, and δ_X is the phase shift angle between the voltages generated at the HV and LV sides of the DHB under consideration. Dividing this power by $V_{busHX}[k]$, it results

$$i_{oX}[k] = \frac{m V_{busL}[k] \delta_X[k]\left(\pi - |\delta_X[k]|\right)}{8\pi^2 L_d f_{sw}^{dhb}}, \qquad (7)$$

which describes the relation between input port i_{oX} and the control action δ_X. The outputs of all the DHBs are connected in parallel, and feed the LV bus. The relation between the input signals and the output signals is obtained through power balance, as described in the following equation:

$$i_{dhbX}[k] = \frac{i_{oX}[k] V_{busHX}[k]}{V_{busL}[k]}. \qquad (8)$$

Note that in this DHB model, the independent variable (control input) for each DHB is δ_X.

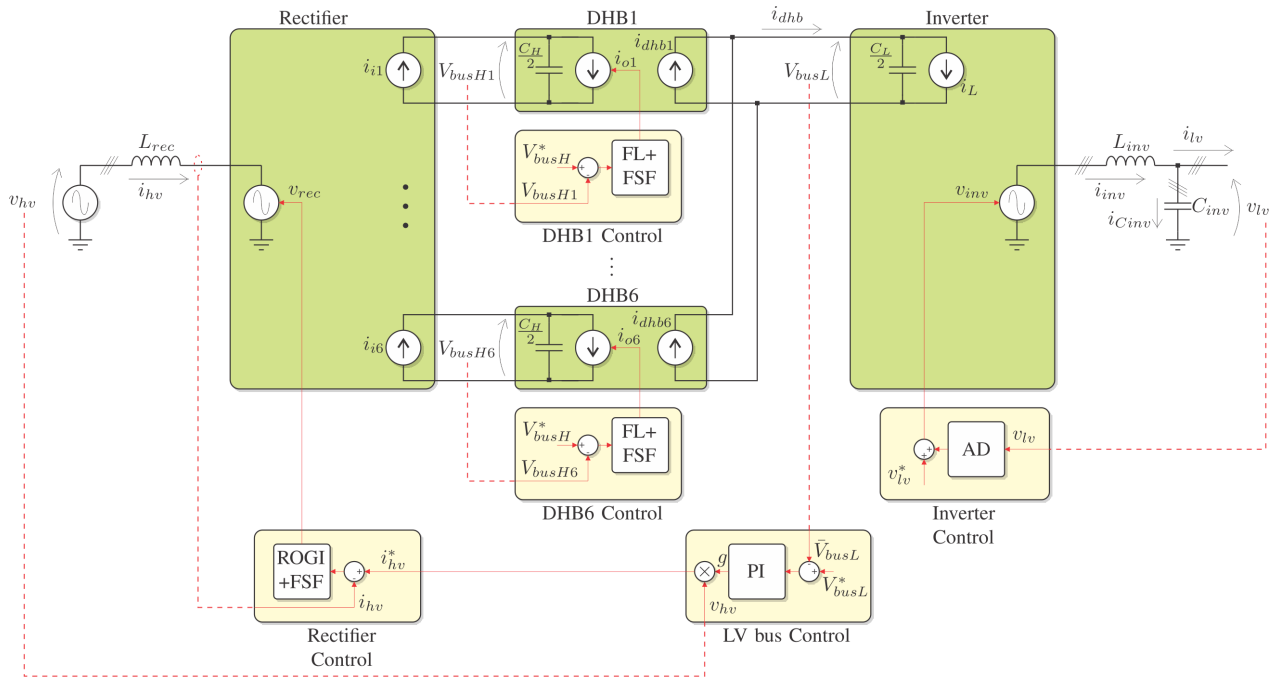

Figure 2: SST topology, model and general control scheme.

2.3 Inverter

The inverter is a three-phase DC-AC converter connected to the LV grid. The input port is modeled as a controlled current source i_L, and the output port is modeled as a three-phase controlled voltage source $v_{inv} = [v_{invr}\ v_{invs}\ v_{invt}]^T$. The load voltage and current are $v_{lv} = [v_{lvr}\ v_{lvs}\ v_{lvt}]^T$ and $i_{lv} = [i_{lvr}\ i_{lvs}\ i_{lvt}]^T$, respectively.

The coupling between the output ports of the DHBs and the input port of the inverter is performed through a capacitor. The voltage across this capacitor is modeled through the difference equation:

$$V_{busL}[k+1] = \frac{T_s}{C_L/2}\left(i_{dhb}[k] - i_L[k]\right) + V_{busL}[k], \quad (9)$$

where

$$i_{dhb}[k] = \sum_{X=1}^{6} i_{dhbX}[k]. \quad (10)$$

The coupling between the load and the output port of the inverter is performed by an LC filter. Since each leg of the inverter is controlled as a single phase converter, the zoh discretization of this filter is given for each phase of the inverter. This is denoted with subscript Y, which can be equal to r, s or t:

$$x_{invY}[k+1] = A_{inv}x_{invY}[k] + B_{inv}v_{invY}[k] + B_{inv1}i_{lvY}[k], \quad (11)$$

where $x_{invY}[k] = [i_{invY}[k]\ v_{lvY}[k]]^T$,

$$A_{inv} = \begin{bmatrix} \cos(\frac{T_s}{\sqrt{C_{inv}L_{inv}}}) & -\sqrt{\frac{C_{inv}}{L_{inv}}}\sin(\frac{T_s}{\sqrt{C_{inv}L_{inv}}}) \\ \sqrt{\frac{L_{inv}}{C_{inv}}}\sin(\frac{T_s}{\sqrt{C_{inv}L_{inv}}}) & \cos(\frac{T_s}{\sqrt{C_{inv}L_{inv}}}) \end{bmatrix}, \quad (12)$$

$$B_{inv} = \begin{bmatrix} \sqrt{\frac{C_{inv}}{L_{inv}}}\sin(\frac{T_s}{\sqrt{C_{inv}L_{inv}}}) \\ 1 - \cos(\frac{T_s}{\sqrt{C_{inv}L_{inv}}}) \end{bmatrix}, \quad (13)$$

$$B_{inv1} = \begin{bmatrix} 1 - \cos(\frac{T_s}{\sqrt{C_{inv}L_{inv}}}) \\ -\sqrt{\frac{L_{inv}}{C_{inv}}}\sin(\frac{T_s}{\sqrt{C_{inv}L_{inv}}}) \end{bmatrix}. \quad (14)$$

As in the previous converters, the relation between the input signals and the output signals is obtained through power balance, as described in the following equation:

$$i_L[k] = \frac{v_{inv}[k] \bullet i_{lv}[k]}{V_{busL}[k]}, \quad (15)$$

where the $\bullet$ operator denotes scalar product. Note that in this inverter model, the independent variables (control inputs) are the three-phase components of $v_{inv}[k]$.

3 Converter controller description

Figure 2 shows the simplified block diagrams of the proposed controllers for each converter. In this figure, dashed lines represent measured signals, and solid lines in the controllers represent control signals. In what follows, each individual controller is described.

3.1 Rectifier control

This controller is tasked to make the HV grid current i_{hv} to copy the current reference i^*_{hv}. This is

achieved through a full state feedback (FSF) control with the addition of a reduced order generalized integrator (ROGI) [12]. The ROGI is added to achieve zero steady state tracking error, since the current reference is a grid frequency positive sequence three-phase signal. Considering a one sample time processing delay, typical in digital implementations, complex vector notation, and space vector modulation (SVM), the control action is

$$v_{rec}[k] = v^*_{recSVM}[k-1], \tag{16}$$

$$v^*_{recSVM}[k] = v^*_{rec}[k] - v_{mc}[k], \tag{17}$$

$$v_{mc}[k] = 0.5\left(\max(v^*_{rec}[k]) + \min(v^*_{rec}[k])\right), \tag{18}$$

where max and min functions are computed between the *abc* components of $v^*_{rec}[k]$. Also,

$$\vec{v}^*_{rec}[k] = -K_{rec}\begin{bmatrix}\vec{i}_{hv}[k] - \vec{i}^*_{hv}[k]\\ \vec{v}^*_{rec}[k-1]\\ \vec{r}_1[k]\end{bmatrix}, \tag{19}$$

$$\vec{r}_1[k+1] = j(1-e^{j\omega T_s})\left(\vec{i}_{hv}[k] - \vec{i}^*_{hv}[k]\right) + e^{j\omega T_s}\vec{r}_1[k], \tag{20}$$

with K_{rec} a 1×3 complex gain vector, and $\vec{r}_1[k]$ represents the state of a ROGI tuned at fundamental grid angular frequency ω. As described in [12], gain vector K_{rec} can be found using the linear quadratic regulator method, or by pole placement using Ackerman's formula, and the matrix description of the system:

$$x_{rec}[k+1] = A_{rec}x_{rec}[k] + B_{rec}\vec{v}^*_{rec}[k], \tag{21}$$

where $x_{rec}[k] = [\vec{i}_{hv}[k]\ \vec{v}^*_{rec}[k-1]\ \vec{r}_1[k]]^T$,

$$A_{rec} = \begin{bmatrix}1 & -\frac{T_s}{L_{rec}} & 0\\ 0 & 0 & 0\\ j(1-e^{j\omega T_s}) & 0 & e^{j\omega T_s}\end{bmatrix}, \tag{22}$$

$$B_{rec} = [0\ 1\ 0]^T. \tag{23}$$

The reference i^*_{hv} is the output of the LV bus controller, and it is related to the instantaneous HV grid voltage through

$$i^*_{hv}[k] = g[k]v_{hv}[k], \tag{24}$$

where g is a scalar variable signal. Therefore, depending on the sign of g and assuming v_{hv} sinusoidal with no harmonic distortion, the rectifier will source or sink a three-phase sinusoidal current to the HV grid, with unity power factor. In this paper the closed loop poles are chosen to achieve a settling time of 4.5[ms].

3.2 DHB control

The objective of the DHBs is to transfer the pulsating power of each of the H bridges of the rectifier to the LV bus, where the resulting power is non-pulsating. To achieve this objective, the controller of each DHB is designed to keep its instantaneous voltage V_{busHX} at its reference level V^*_{busH} (which is the same for all six DHBs). As shown by (7), the relation between current i_{oX} and phase-shift angle δ_X is non-linear. In order to be able to apply linear control techniques, a feedback linearization (FL) is implemented. Then, the resulting linear system is controlled through FSF.

Considering a one sample time processing delay, the control action is

$$\delta_X[k] = \delta^*_X[k-1], \tag{25}$$

where

$$\delta^*_X[k] = 0.5\pi\left(1-\sqrt{1-32f^{dhb}_{sw}\frac{|i^*_{oX}[k]|}{mV_{busL}[k]}}\right)sign(i^*_{oX}[k]), \tag{26}$$

is obtained from (7) and it is the FL equation for the system. Assuming that $V_{busL}[k] \simeq V_{busL}[k-1]$ (slow varying signal), it can be numerically verified that for a given value of $i^*_{oX}[k-1]$, evaluating (26) at $k-1$, and replacing the result in (25) and (7) yields $i_{oX}[k] \simeq i^*_{oX}[k-1]$. Therefore, the linearized system is modeled by (5) and

$$i_{oX}[k] = i^*_{oX}[k-1]. \tag{27}$$

Adding a discrete time backward Euler integrator to achieve zero steady state error, the control action for each DHB is computed as follows:

$$i^*_{oX}[k] = -K_{DHB}\begin{bmatrix}V_{busHX}[k] - V^*_{busH}[k]\\ r_0[k]\\ i_{oX}[k]\end{bmatrix}, \tag{28}$$

$$r_0[k+1] = T_s\left(V_{busHX}[k] - V^*_{busH}[k]\right) + r_0[k], \tag{29}$$

where K_{dhb} is a 1×3 gain vector, and $r_0[k]$ represents the state of the discrete integrator. Once (28) is computed, the phase shift angle δ^*_X is obtained through (26) and applied to the converter.

Gain vector K_{dhb} can be found using the linear quadratic regulator method, or by pole placement using Ackerman's formula, and the matrix description of the linearized system:

$$x_{dhb}[k+1] = A_{dhb}x_{dhb}[k] + B_{dhb}i^*_{oX}[k], \tag{30}$$

where $x_{dhb}[k] = [V_{busHX}[k]\ r_0[k]\ i_{oX}[k]]^T$,

$$A_{dhb} = \begin{bmatrix}1 & 0 & -\frac{T_s}{C_H/2}\\ T_s & 1 & 0\\ 0 & 0 & 0\end{bmatrix}, \tag{31}$$

$$B_{dhb} = [0\ 0\ 1]^T. \tag{32}$$

This scheme makes each DHB source power to the LV bus if its HV bus voltage is higher than V^*_{busH}, or sink power from the LV bus if its HV bus voltage is lower than V^*_{busH}. In this paper the closed loop poles are chosen to achieve a settling time of 1[ms].

3.3 LV bus control

This controller is tasked to keep the mean value of the LV bus voltage ($\bar{V}_{busL}$ in Figure 2) at the reference level V^*_{busL}. In order to do so, signal V_{busL} is filtered (filter not shown in the figure) and then a proportional integral (PI) controller is used. The output of this controller is the variable gain g. This gain is used to properly scale the measured HV grid voltage, and generate the current reference for the rectifier, defined in (24). For this reason, the dynamics of the rectifier control loop and the LV bus control loop must be decoupled. This is achieved by making the bus control loop significantly slower than the rectifier and DHB control loops.

The LV bus voltage is modeled by (9). Since there is no controlled current source directly connected to the LV bus, the design of the controller assumes that i_{dhb} is the control action. Once the control action i_{dhb} is computed, gain g is obtained through power balance:

$$g[k] = \frac{i_{dhb}[k]\bar{V}_{busL}[k]}{3V^2_{nomhv}}, \tag{33}$$

where V_{nomhv} is the nominal rms value of the HV grid voltage. As stated at the beginning of this section, this controller is slow. Therefore, both the processing delay and the dynamics of the filter used to obtain $\bar{V}_{busL}$ can be ignored without significant error. Considering this, and adding a discrete time backward Euler integrator to achieve zero steady state error, the control action is computed as follows:

$$i_{dhb}[k] = -K_{LV}\begin{bmatrix}\bar{V}_{busL}[k] - V^*_{busL}[k] \\ r_{0LV}[k]\end{bmatrix}, \tag{34}$$

$$r_{0LV}[k+1] = Ts\left(\bar{V}_{busL}[k] - V^*_{busL}[k]\right) + r_{0LV}[k], \tag{35}$$

where K_{LV} is a 1×2 gain vector, and $r_{0LV}[k]$ represents the state of the discrete integrator. Once (34) is computed, gain g is computed through (33), and used to generate the HV grid current reference i^*_{hv} through (24).

Gain vector K_{LV} can be found using the linear quadratic regulator method, or by pole placement using Ackerman's formula, and the matrix description of the system:

$$x_{LV}[k+1] = A_{LV}x_{LV}[k] + B_{LV}i_{dhb}[k], \tag{36}$$

where $x_{LV}[k] = [V_{busL}[k]\ r_{0LV}[k]]^T$,

$$A_{LV} = \begin{bmatrix}1 & 0 \\ T_s & 1\end{bmatrix}, \tag{37}$$

$$B_{LV} = [\frac{T_s}{C_L/2}\ 0]^T. \tag{38}$$

In this paper the closed loop poles are chosen to achieve a settling time of 100[ms].

3.4 Inverter control

This controller implements the active damping (AD) of the output LC filter resonance. The implementation of the AD requires to measure the current through C_{inv}. To avoid this measurement, an estimator through high pass filter derivation is used. This estimator only requires the measurement of v_{lv}, and only slightly increases the settling time of the control loop. The LV grid voltage reference v^*_{lv} is added to the control action of the AD. This voltage reference is a three-phase balanced sinusoidal signal, which can be generated internally, or can be obtained through a synchronization algorithm in synchronism with the HV grid voltage.

Since each leg of the inverter is controlled independently, there are three equal controllers. In what follows, they are described with subscript $Y = r$, s or t. Considering a one sample processing time, the control action for the active damping strategy is $v_{invY}[k] = v^*_{invY}[k-1]$, where

$$v^*_{invY}[k] = -K_{lv}\begin{bmatrix}\hat{i}_{CinvY}[k] \\ v_{lvY}[k] \\ v^*_{invY}[k-1]\end{bmatrix} + K^* v^*_{lvY}, \tag{39}$$

where K_{lv} is a 1×3 gain vector, K^* is a gain, and $\hat{i}_{CinvY}[k]$ is the estimated capacitor current, obtained from the zoh discretization of a high pass filter:

$$\eta_Y[k+1] = (e^{-\omega_c T_s} - 1)v_{lvY}[k] + e^{-\omega_c T_s}\eta_Y[k], \tag{40}$$

$$\hat{i}_{CinvY}[k] = C_{inv}\omega_c\left(v_{lvY}[k] + \eta_Y[k]\right), \tag{41}$$

with ω_c the cut off frequency of the high pass filter, and η_Y the state of the filter.

Gain vector K_{lv} is obtained by pole placement to damp the LC filter resonance using Ackerman's formula, and the matrix description of the system:

$$x_{lv}[k+1] = A_{lv}x_{lv}[k] + B_{lv}v^*_{invY}[k], \tag{42}$$

where $x_{lv}[k] = [i_{invY}[k]\ v^*_{invY}[k-1]\ v_{invY}[k]]^T$,

$$A_{lv} = \begin{bmatrix}A_{inv} & B_{inv} \\ 0\ 0 & 0\end{bmatrix}, \tag{43}$$

$$B_{lv} = [0\ 0\ 1]^T. \tag{44}$$

Finally, gain K^* is included to compensate the magnitude of the LV grid voltage reference, and is obtained evaluating:

$$TF = C_{lv}(z\,I - A^{CL}_{lv})^{-1}B_{lv}\big|_{z=e^{j\omega T_s}}, \tag{45}$$

$$K^* = |1/TF|, \tag{46}$$

where $A^{CL}_{lv} = A_{lv} - B_{lv}K_{lv}$, I is the 3×3 identity matrix and $C_{lv} = [0\ 1\ 0]$. Note that the controllers for each phase use the same gain vector K_{lv} and gain K^*. In this paper the closed loop poles are chosen for optimal damping ($\zeta = 0.707$). This results in a settling time of approximately 2[ms].

4 Parameter selection criteria

This section gives criteria for choosing the values of the different parameters of each converter.

4.1 Rectifier coupling inductance L_{rec}

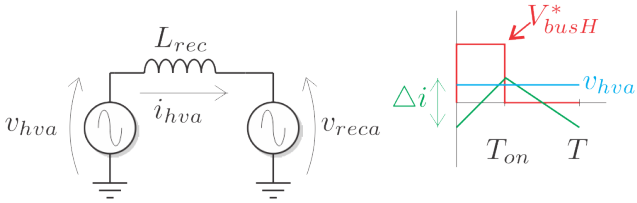

Figure 3: Rectifier phase a and switching interval variables.

The value of L_{rec} is chosen to obtain a desired current ripple Δi when injecting zero current to the HV grid. Due to the 5-level structure of the rectifier and the use of unipolar modulation, the effective switching frequency applied to L_{rec} is $4f^{rec}_{sw}$ [1]. Also, this multilevel structure ensures that the voltage difference applied to L_{rec} will never be larger than V^*_{busH} (assuming all the HV buses are kept at that level).

Taking phase a as a reference, Figure 3 shows one switching interval. The current variation in this interval is

$$\Delta i = \frac{T_{on}}{L_{rec}}(v_{hva} - V^*_{busH}). \tag{47}$$

Since zero current injection is assumed, in this interval

$$v_{hva} \simeq V^*_{busH} d, \tag{48}$$

where $d = T_{on}/T$. Therefore, replacing this in (47),

$$\Delta i = \frac{V^*_{busH}}{L_{rec} 4 f^{rec}_{sw}}(d^2 - d), \tag{49}$$

where $T = 1/(4f^{rec}_{sw})$ was used. The maximum Δi occurs for $d = 0.5$, therefore for this condition, from (49),

$$L_{rec} = \frac{V^*_{busH}}{\Delta i 16 f^{rec}_{sw}}. \tag{50}$$

From Table 1, choosing the peak current ripple $\Delta i/2 = 0.1(\sqrt{2}I_{nomhv})$, the inductance results $L_{rec} = 190$[mH]. From an additional analysis not included in this paper, considering commercially available cores, $L_{rec} = 200$[mH] is chosen.

4.2 DHB transformer leakage inductance L_d

From (6), assuming $V_{busHX}[k] = V^*_{busH}$ and $V_{busL}[k] = V^*_{busL} = V^*_{busH}/m$ the maximum power transfer occurs for $\delta_X[k] = \pi/2$ and results

$$P_{dhbMAX} = \frac{(V^*_{busH})^2}{32 L_d f^{dhb}_{sw}}. \tag{51}$$

Under nominal operation conditions, each DHB will have to transfer a mean power $\bar{P}_{dhb} = S_{nom}/6$. Taking a safety margin of $P_{dhbMAX} = 2\bar{P}_{dhb}$ to catch any transients, and replacing this in (51), the leakage inductance results

$$L_d = \frac{3(V^*_{busH})^2}{32 S_{nom} f^{dhb}_{sw}}. \tag{52}$$

Using the necessary parameters from Table 1 to evaluate (52), it results $L_d = 8.44$[mH]. From an additional analysis not included in this paper, designing L_d considering commercially available cores, it results $L_d = 8.8$[mH] .

4.3 HV bus capacitor C_H

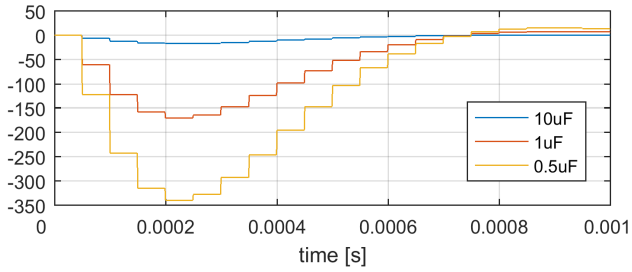

Figure 4: ΔV_{busH} [V] for a 10% HV grid voltage dip for different values of C_H.

During the event of dips or swells in the HV grid voltage v_{hv}, there will be a transient behavior in each of the HV buses. This can lead to unacceptable under/over voltages in V_{busHX}. The HV buses voltage variations during these transients are determined by the value of C_H, the settling time of each DHB control loop, and the magnitude of the dips or swells. Since the evaluation of these transients involves the DHB control loop, the process is iterative. For a given value of C_H, gain K_{dhb} must be computed. Then, the performance is evaluated through a simple simulation applying the desired dip or swell magnitude. Finally, the process is repeated until the desired performance is attained.

The evaluation is performed considering a step change in the magnitude of v_{hv}. In the following, the worst case scenario for V_{busH1} is analyzed, which is similar for the remaining buses.

The maximum instantaneous power variation in phase a occurs when the rectifier is sinking nominal current, and at the instantaneous peak of $v_{hva}[k]$ its magnitude changes Δv_{hv} volts. From (1), assuming that previous to the step $\vec{v}_{hv} \simeq \vec{v}_{rec}$, the magnitude of the change in the HV grid current is

$$\Delta i_{hv} \simeq \frac{T_s}{L_{rec}} \Delta v_{hv}. \tag{53}$$

From (2), assuming that previous to the step $V_{busH1} = V_{busH1} = V^*_{busH}$, the variation in current i_{i1} is

$$\Delta i_i = \frac{\sqrt{2} V_{nomhv} \Delta i_{hv}}{2 V^*_{busH}} = \frac{T_s}{L_{rec}} \frac{\sqrt{2} V_{nomhv} \Delta v_{hv}}{2 V^*_{busH}}, \tag{54}$$

where (53) was used for the last equality. Now the effect of $\triangle v_{hv}$ in V_{busH1}, defined as $\triangle V_{busH}$, is evaluated simulating the closed loop response of the linearized DHB (30)-(32):

$$\triangle x_{dhb}[k+1] = A^{cl}_{dhb}\triangle x_{dhb}[k] + B^{i_i}_{dhb}\triangle i_i, \quad (55)$$

$$\triangle V_{busH}[k] = [1\ 0\ 0]\triangle x_{dhb}[k], \quad (56)$$

where $B^{i_i}_{dhb} = [\frac{T_s}{C_H/2}\ 0\ 0]^T$ and $A^{cl}_{dhb} = A_{dhb} - B_{dhb}K_{dhb}$. Figure 4 shows simulation results for this system for $C_H = 10$ [μF], 1[μF] and 0.5[μF] when a 10% dip is simulated ($\triangle v_{hv} = -0.1V_{nomhv}$) for the DHB control designed with a settling time of 1[ms]. From the results $C_H = 1$ [μF] is chosen, since it results in a 2.5% voltage variation.

4.4 LV bus capacitor C_L

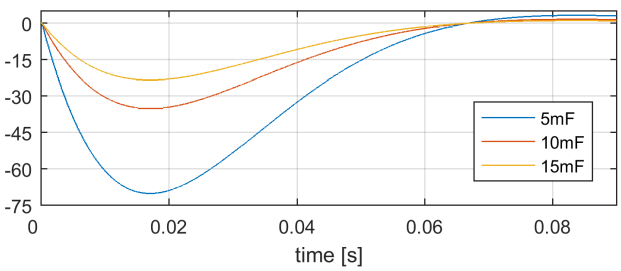

Figure 5: $\triangle V_{busL}$ [V] for a nominal load sudden connection and different values of C_L.

The value of capacitor C_L is chosen so that in the event of a sudden nominal load connection, the LV bus voltage does not go below the minimum value required for normal operation. The minimum LV bus voltage required for operation is

$$V_{busLMIN} = 2\sqrt{2}V_{nomlv} = 622V, \quad (57)$$

where the value is obtained from Table 1. Therefore, a conservative design criterion is to keep $V_{busL} > 700V$ when a nominal load is connected. This is equivalent to obtain a LV bus voltage variation $\triangle V_{busL} < 100V$.

To evaluate the LV bus voltage variation for different values of C_L, gain vector K_{LV} is computed for each given value, and then a simulation is performed. From (36)-(38), the following system is simulated:

$$\triangle x_{LV}[k+1] = A^{cl}_{LV}\triangle x_{LV}[k] + B^{cl}_{LV}\triangle i_L, \quad (58)$$

$$\triangle V_{busL}[k] = [1\ 0]\triangle x_{LV}[k], \quad (59)$$

where $A^{CL}_{LV} = A_{LV} - B_{LV}K_{LV}$, $B^{cl}_{LV} = -B_{LV}$ and $\triangle i_L = S_{nom}/V^*_{busL}$. Figure 5 shows simulation results for this system for $C_L = 5$ [mF], 10[mF] and 15[mF] when a nominal load is suddenly connected and the LV bus voltage control loop is designed with a settling time of 100[ms]. From the results all capacitor values meet the requirements, however $C_L = 10$ [mF] is chosen because of reduced ripple under unbalanced load conditions.

4.5 Inverter filter $L_{inv}C_{inv}$

The typical output impedance of a standard transformer is 2%-5% of its base impedance. Therefore, L_{inv} is chosen so that its impedance at angular frequency ω is 2% of the base impedance:

$$L_{inv} = 0.02\frac{3V^2_{nomlv}}{\omega S_{nom}} = 462\ [\mu H]. \quad (60)$$

On the other hand, capacitor C_{inv} limits the bandwidth of the output. Here, to obtain a fast transient response, the cut-off angular frequency of the output filter is chosen

$$\omega_{cut-off} = 20\omega. \quad (61)$$

Since the resonance frequency of the filter is approximately equal to the cut-off frequency,

$$\omega_{res} \simeq \omega_{cut-off} = \frac{1}{\sqrt{L_{inv}C_{inv}}}, \quad (62)$$

then

$$C_{inv} = \frac{1}{(20\omega)^2 L_{inv}} = 55\ [\mu F]. \quad (63)$$

5 Operation analysis of the control system and simulation results

This section presents simulation results of the proposed SST when a load is suddenly connected and disconnected. Additionally, results for sudden nonlinear load connection are included. The results are obtained using the switching models of all converters. The system parameter summary is shown in Table 1.

Table 1: System parameter summary

RECTIFIER AND LV BUS		
Param.	Value	Description
S_{nom}	20[kVA]	SST nominal power
V_{nomhv}	7621[Vrms]	HV nom. phase voltage
I_{nomhv}	0.875[Arms]	HV nom. phase current
f	50[Hz]	HV grid frequency
L_{rec}	200[mH]	HV filter inductance
V^*_{busL}	800[V]	LV bus reference
C_L	10[mF]	LV bus capacitor
f^{rec}_{sw}	8[kHz]	Switching frequency
DHB		
C_H	1[μF]	HV bus capacitor
C^{dhb}_L	56[μF]	LV DHB capacitor
L_d	8.8[mH]	DHB leakage ind.
V^*_{busH}	6000[V]	HV bus reference
m	7.5	Transformer relation
f^{dhb}_{sw}	20[kHz]	Switching frequency
INVERTER		
L_{inv}	461.2[μH]	LC filter ind.
C_{inv}	55[μF]	LC filter cap.
V_{nomlv}	220[Vrms]	LV phase voltage
f^{inv}_{sw}	20[kHz]	Switching frequency

The controllers were designed so that the rectifier control loop has a settling time of 4.5[ms], the DHB control loop has a settling time of 1[ms], and the LV bus voltage control loop has a settling time of 100[ms]. The settling time of the inverter AD loop is defined by the cutoff frequency of its LC output filter plus the estimation of the current through C_{inv}. This settling time results approximately 2[ms].

5.1 Sudden load connection

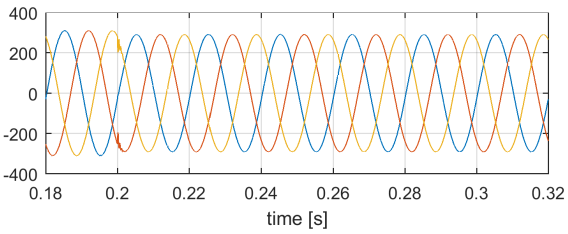

Figure 6: v_{lv} [V] sudden load connection.

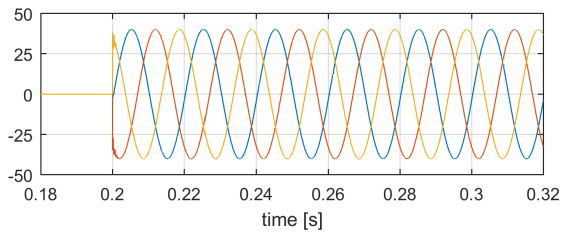

Figure 7: i_{lv} [A] sudden load connection.

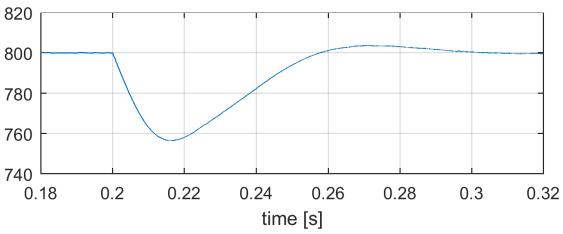

Figure 8: V_{busL} [V] sudden load connection.

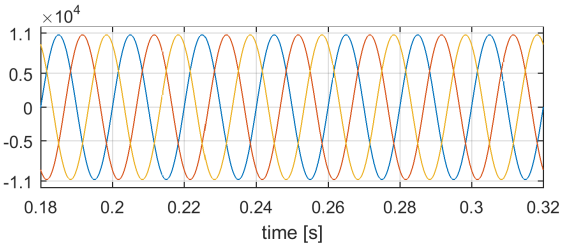

Figure 9: v_{hv} [V] sudden load connection.

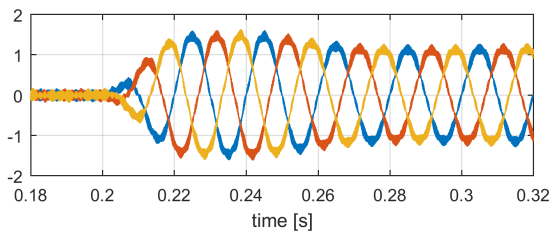

Figure 10: i_{hv} [A] sudden load connection.

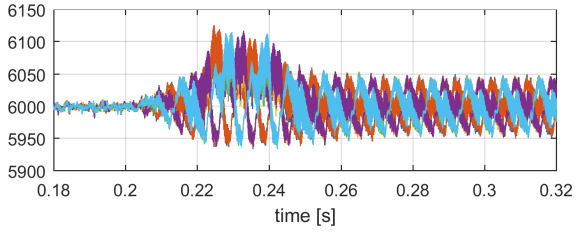

Figure 11: $V_{busH1} - V_{busH6}$ [V] sudden load connection.

The simulation results shown in Figures 6-11 start at $t = 0.18$[s] with the SST in steady state, with no load connected on the LV side. This means that the HV and LV buses start at their reference voltage levels and that a balanced three-phase sinusoidal voltage v_{lv} is generated without taking significant current i_{hv} from the HV grid.

At $t = 0.2$[s] a resistive nominal load is connected at the inverter output. The following sequence of events occurs (refer to Figure 2 for the definition of the variables):

- Figures 6 and 7 show v_{lv} and i_{lv}, respectively. As expected, when the load is connected v_{lv} has a short transient.
- Through power balance, current source i_L takes current from capacitor C_L, reducing voltage V_{busL} as shown in Figure 8. As can be seen, its settling time is approximately 100[ms], as designed.
- The LV bus voltage control loop detects the reduction of $\bar{V}_{busL}$, increasing in turn the value of g, resulting in $g > 0$. As a result, current reference i^*_{hv} magnitude increases.
- Commanded by its current controller, the rectifier sinks active power from the grid, with unity power factor. Figures 9 and 10 show v_{hv} and i_{hv}, respectively. Here the settling time of the current is tied to the settling time of g, defined by the LV bus control loop.
- Through power balance, the current source outputs of the rectifier charges capacitors C_H of the HV buses, increasing their voltage levels. The voltages of the HV buses is shown in Figure 11.
- The control loop of each DHB detects the increase in their respective HV bus voltage V_{busHX}. As a result, it commands each DHB to sink current i_{oX} in order to decrease the instantaneous value V_{busHX} to its reference value V^*_{busH} once again. This results in the short transient increase in the mean value of voltages V_{busHX} seen in Figure 11. Through power balance, each output current i_{dhbX} sources current to the LV bus, charging C_L to V^*_{busL} again, as shown in Figure 8.

By the end of this sequence, in steady state, the system is delivering power to the load and taking current with unity power factor from the HV grid.

5.2 Sudden load disconnection

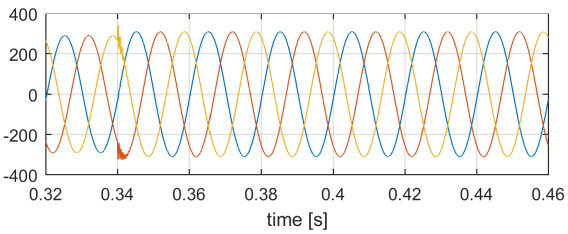

Figure 12: v_{lv} [V] sudden load disconnection.

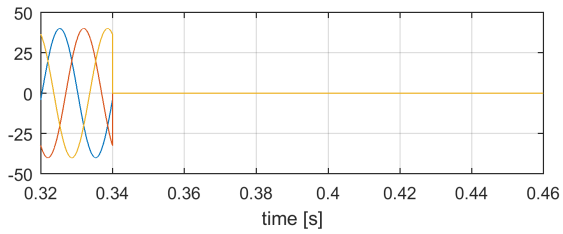

Figure 13: i_{lv} [A] sudden load disconnection.

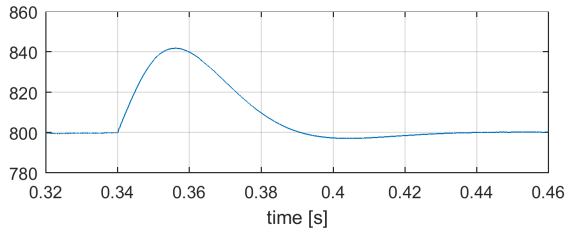

Figure 14: V_{busL} [V] sudden load disconnection.

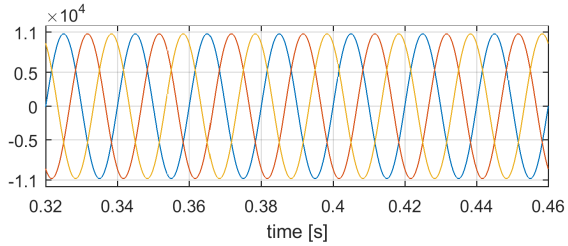

Figure 15: v_{hv} [V] sudden load disconnection.

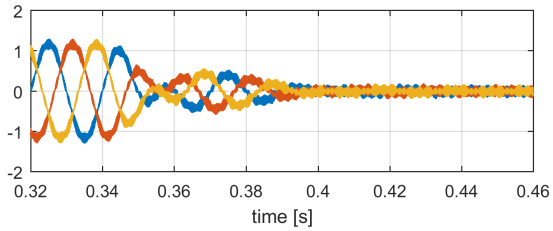

Figure 16: i_{hv} [A] sudden load disconnection.

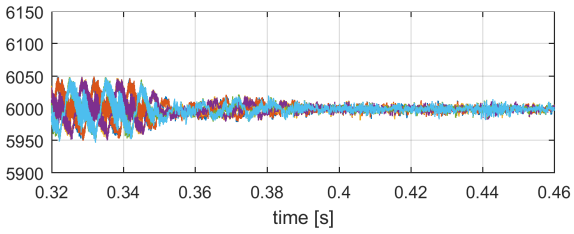

Figure 17: $V_{busH1} - V_{busH6}$ [V] sudden load disconnection.

Starting from the previous condition, if the load is now disconnected, the following sequence of events will occur:

- Figures 12 and 13 show v_{lv} and i_{lv}, respectively. As expected, when the load is disconnected v_{lv} has a short transient.
- Through power balance, current source i_L stops sinking current from capacitor C_L, which charges because the DHBs are still transferring power from the HV grid. This is seen in Figure 14.
- LV bus voltage control loop detects the voltage increase in $\bar{V}_{busL}$, decreasing in turn the value of g, resulting in $g < 0$. As a result, current reference i^*_{hv} magnitude decreases.
- Commanded by its current controller, the rectifier goes from sinking to supplying active power to the grid, with unity power factor. Figures 15 and 16 show v_{hv} and i_{hv}, respectively.
- Through power balance, the current source outputs of the rectifier discharge capacitors C_H of the HV buses, decreasing their voltage levels, as seen in Figure 17.
- The control loop of each DHB detects the decrease in their respective HV bus voltage V_{busHX}. As a result, it commands each DHB to source current i_{oX} in order to increase the instantaneous value V_{busHX} to its reference value V^*_{busH} once again. This results in the short transient decrease in the mean value of voltages V_{busHX} seen in Figure 17. Through power balance, each output current i_{dhbX} sinks current from the LV bus, discharging C_L to V^*_{busL} again, as shown in Figure 14.

By the end of this sequence, in steady state, the system has its buses at their reference values, and the inverter generates v_{lv} without sinking current i_{hv} from the HV grid.

5.3 Sudden non-linear load connection

The simulation of section 5.1 is repeated for the sudden connection of a balanced non-linear load. For each phase of the inverter, the load is composed of a single phase rectifier, feeding a 1[mH] inductor in series an RC load where R and C are in parallel (with R=19.5[Ω] and C=1[μF]). The results of this simulation are shown in Figures 18-23. As can be seen in these results, the proposed topology works well under highly non-linear load conditions.

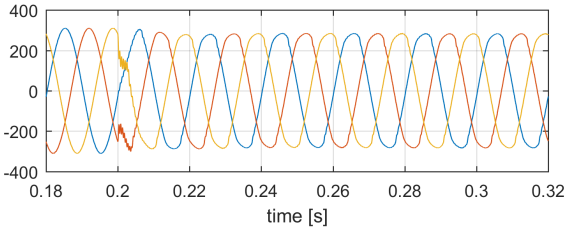

Figure 18: v_{lv} [V] sudden non-linear load connection.

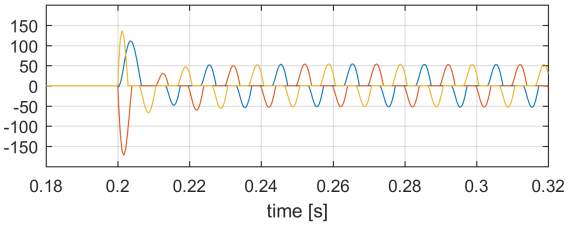

Figure 19: i_{lv} [A] sudden non-linear load connection.

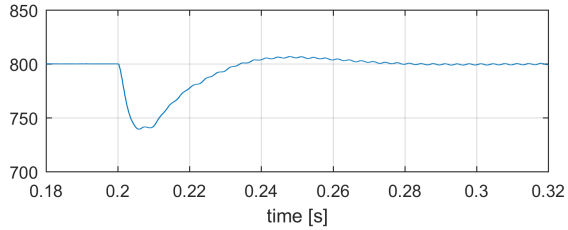

Figure 20: V_{busL} [V] sudden non-linear load connection.

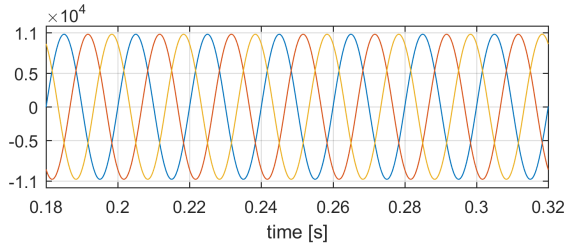

Figure 21: v_{hv} [V] sudden non-linear load connection.

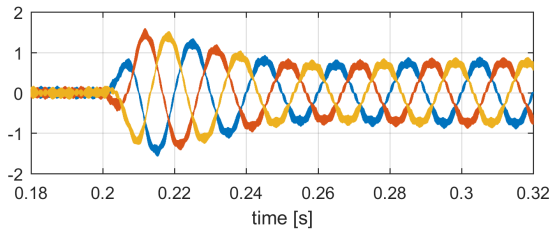

Figure 22: i_{hv} [A] sudden non-linear load connection.

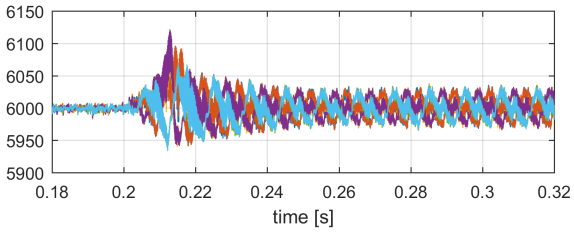

Figure 23: $V_{busH1} - V_{busH6}$ [V] sudden non-linear load connection.

5.4 Sudden non-linear unbalanced load connection

The simulation of the previous section is repeated, using the same non-linear load, but connecting these loads to only two of the three phases. The results of this simulation are shown in 24-29. As can be seen in these results, the proposed topology also works well for unbalanced non-linear loads.

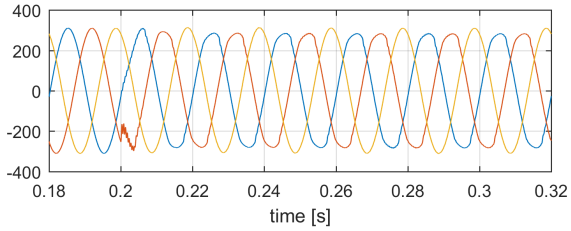

Figure 24: v_{lv} [V] sudden non-linear unbalanced load connection.

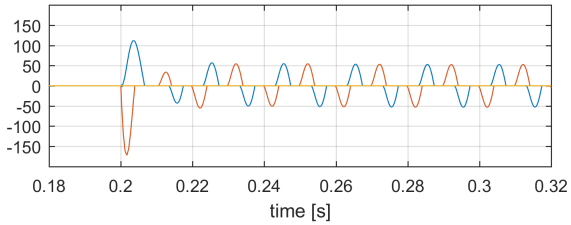

Figure 25: i_{lv} [A] sudden non-linear unbalanced load connection.

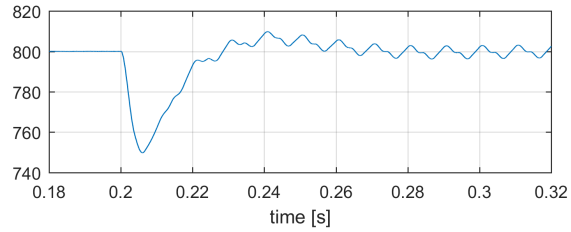

Figure 26: V_{busL} [V] sudden non-linear unbalanced load connection.

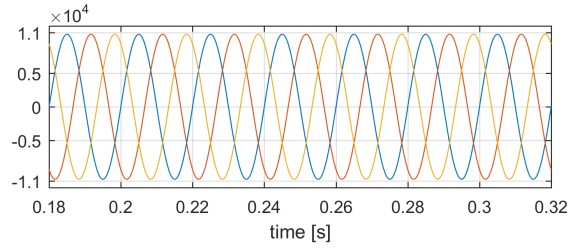

Figure 27: v_{hv} [V] sudden non-linear unbalanced load connection.

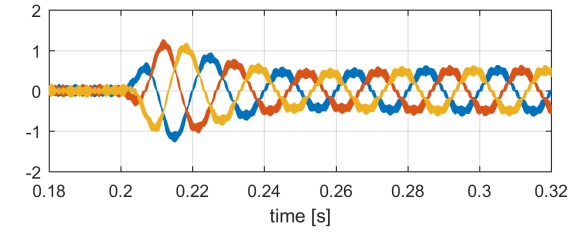

Figure 28: i_{hv} [A] sudden non-linear unbalanced load connection.

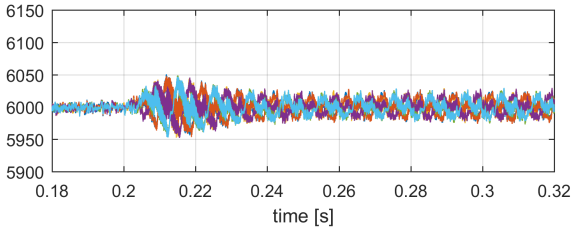

Figure 29: $V_{busH1} - V_{busH6}$ [V] sudden non-linear unbalanced load connection.

6 Conclusions

In this paper a model and a control strategy for an SST topology is proposed. The analyzed SST is designed using three separate stages: a rectifier, a DC-DC converter and an inverter. The proposed design approach is to model each stage using simple models. These simple models help to design and tune the controllers for each stage. The main focus of the tuning procedure is to obtain good performance to sudden load connections. Criteria to choose the main parameters of the SST are also given.

To validate the proposed method, simulation results are presented. The results show that the proposed topology and control strategies perform as expected from design conditions. Moreover, the staged design of the SST allows to decouple the HV side from the LV side in regard to load disturbances, which is an additional feature of the SST when compared to traditional transformers. Simulations were performed for both linear and non-linear loads. Moreover, a non-linear unbalanced load was also tested, with good performance results.

Acknowledgment The authors are grateful to CONICET, UNIVERSIDAD NACIONAL DEL SUR and ANPCyT for their institutional and economic support

Appendix

Given a three-phase signal $f = [f_a\ f_b\ f_c]^T$, its $\alpha\beta$ components are obtained through Clarke's transform:

$$\begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & \sqrt{3}/2 & -\sqrt{(3)}/2 \end{bmatrix}\begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix}. \tag{64}$$

Then, the complex vector $\vec{f}$ is defined as

$$\vec{f} = f_\alpha + j f_\beta, \tag{65}$$

where $j = \sqrt{-1}$.

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