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Active Current Mirrors for Low-Voltage Analog Circuit Design

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Abstract In this work, active current mirrors using sensing resistors and a pass transistor in a feedback loop will be examined in detail. First, several non-idealities in this family of circuits, such as offset, noise, output impedance, or bandwidth, are addressed, showing no performance degradation under certain circumstances. Then, the design and measurement results of a 10- μ A (nominal) active current mirror that can operate down to just 80 mV voltage drop are presented. Finally, two simple amplifier stages using classic and active current mirrors are compared, the latter operating almost at a third of the supply voltage. It is possible to conclude that active current mirrors can be a very valuable building block for low-voltage analog circuits.

Keywords Analog circuits · Low voltage · Active current mirror · Analog design

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1 Introduction

Current mirrors like the one in Fig. 1a are a basic building block in almost all analog circuits. The voltage drop in a current mirror is normally a few hundred mV because M_2 and M_3 must be saturated with a minimum drain-to-source voltage $V_{DS2} \approx 200\text{--}300\text{ mV}$. Furthermore, the gate-to-source voltage V_{GS3} can be even larger as M_3 enters in the moderate inversion (MI) and strong inversion (SI) regions or if the threshold voltage V_T is high. For example, $V_T \sim 900\text{ mV}$ in the case of some analog technologies usual in biomedical ASICs, resulting in a simulated $V_{GS} = 1.07$ for a drain current $I_D = 10\text{ }\mu\text{A}$ (for an arbitrary PMOS sized $W/L = 100\text{ }\mu\text{m}/4\text{ }\mu\text{m}$), which is not practical for a low-voltage circuit. In this work, the active current mirrors will be analysed as a useful option to overcome this problem reducing the minimum voltage drop in a current mirror to a few tens of mV if necessary, even at a relatively large current such as $10\text{ }\mu\text{A}$. An active current mirror will denote a circuit that copies a current to the output like in the traditional 2-transistor mirror, by means of a feedback loop. In Fig. 1b an active current mirror is presented, where the feedback loop is an OTA that equals the voltage drop through two equal or proportional resistors. (Instead of resistors, equal or proportional transistors can also be used.) The OTA adjusts the gate voltage V_{G1} of M_1 , making $V_X = V_Y$. The voltage drop V_{DroP} in the resistors can be very low, down to a few tens of mV if necessary, but what makes this current mirror so attractive for low-voltage applications is that M_1 in Fig. 1b can work in both the saturation region and the linear region, operating if necessary in the latter also

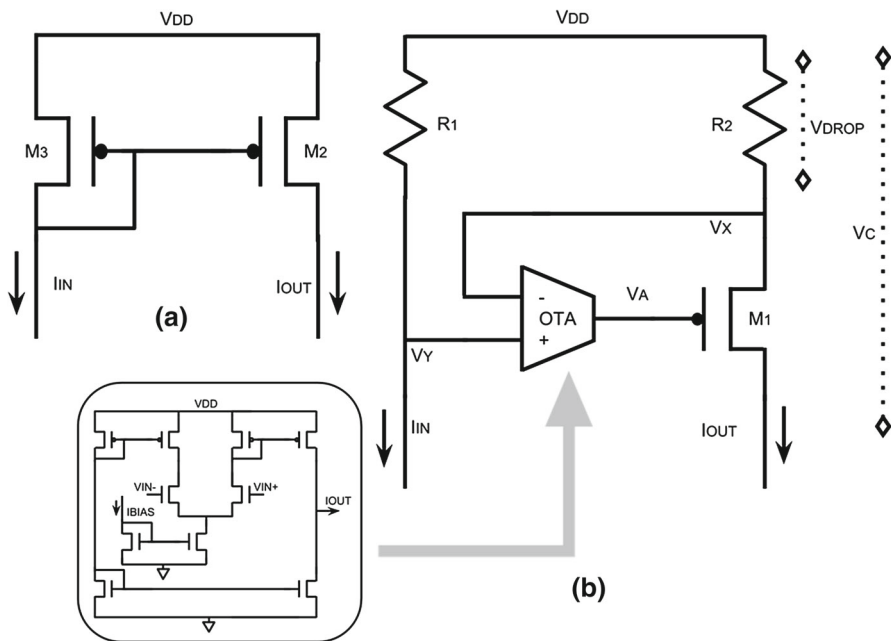


Fig. 1 a A classic 2-transistor current mirror. b Active current mirror

with a few tens mV voltage drop V_{DS1} . While M_1 can operate in linear region, this will not reduce the output impedance, as the active current mirror has to be examined as a whole, and the use of a feedback loop makes possible that the output impedance of the mirror can be orders of magnitude larger than that of M_1 . The active current mirror can substitute the classic one in Fig. 1a, but operating down to a much lower voltage drop V_C , for example as low as 50 mV. Another advantage is the high output impedance that tends to infinity in DC. This circuit block is thus very appropriate for the design of low-voltage analog circuits.

The topology in Fig. 1b is not new and sometimes has been referred to as ‘gain-booster’ mirror, but there exist other rather different circuits also under the same denomination, so the ‘active mirror’ denomination was preferred. In [9] an active mirror is proposed to control the current through a resistor, and several similar topologies are proposed in [4, 6, 7, 11], mostly using transistors instead of resistors, to improve either the output impedance or speed of a current mirror, as well as to reduce the supply voltage. From now an active current mirror will denote, for the sake of simplicity, a circuit with two resistors, a pass transistor, and a feedback amplifier imposing the same resistors’ voltage drop just like in Fig. 1b. The input and output currents are either the same, or the output is scaled by a factor N if $R_1 = N \cdot R_2$.

The active current mirror can substitute classic ones in critical places to reduce the supply voltage of an amplifier for example. In Fig. 2a a standard OTA amplifier stage is presented, while Fig. 2b shows the same OTA but using active current mirrors allowing a reduction in the supply voltage. Only very few references exist to practical embodiments of this idea in an integrated circuit. The problem is that the designer reasonably cares about the excess in power consumption and die area because of the presence of the feedback amplifier, about the noise and the offset of the new mirror, about the stability of the loop, about the impact of the active mirror in the CMRR or the PSRR of the circuit in Fig. 2b, and so on. But apart from the area, none of these non-idealities seem to be inherent to the active current mirror itself. In [8] a similar circuit is proposed, with extremely low voltage input and output requirements, but only simulations are presented and a complete analysis of all non-idealities is not present. Thus, it is necessary to study each one depending on the specific application. In our case the target application is the design of a low-voltage, low-noise biomedical instrumentation amplifier. Thus, the emphasis will be on the supply voltage reduction, the noise and the offset, but the active current mirror’s bandwidth, for example, is not a major problem in the case of the low frequencies of bio-signals ranging from DC to a few kHz [3]. But the same active mirror could be used in other low-voltage applications; for example [10, 12, 13] could be benefited with the use of active current mirrors.

In this work, active current mirrors using resistors will be examined in detail, showing their advantages and disadvantages, and considering trade-offs in noise, offset, power consumption, minimum supply voltage, etc. The work will be carried out through an analytical study, simulations, and measurements on fabricated circuits. In the next section the main active current mirror’s non-idealities such as offset, noise, output impedance, bandwidth are addressed, and some design criteria will be presented. It will be demonstrated that under certain circumstances, it is possible to design an active current mirror to substitute a classic two-transistor mirror, with a negligible

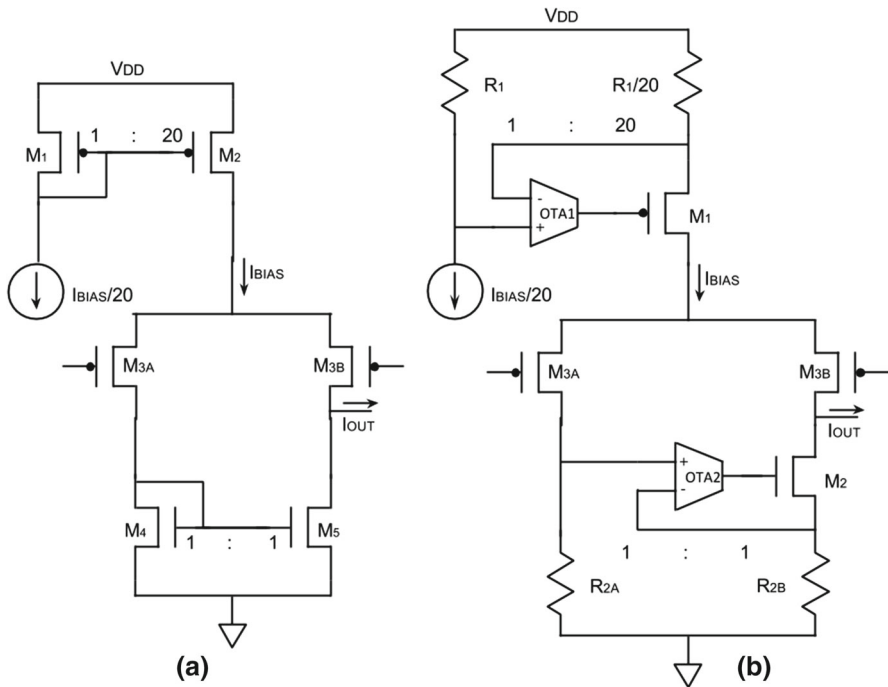


Fig. 2 **a** An OTA using traditional current mirrors. **b** The same OTA using active current mirrors

power consumption or area overhead, and with almost the same noise, offset, etc., but with the consequent advantages in voltage reduction. Then the design of a $10\text{-}\mu\text{A}$ (nominal) active current mirror is presented. The circuit was fabricated in a $0.6\text{-}\mu\text{m}$ technology (threshold voltages are $V_{TN} = 0.90\text{ V}$ and $V_{TP} = 0.95\text{ V}$) and tested, showing the expected low-voltage operation, a good precision in the copy due to a careful layout, and very high output impedance at low frequencies. The minimum voltage drop is only $V_{C(\min)} \sim 80\text{ mV}$, the measured offset was below 200 nA , and the measured output impedance was above $1\text{ M}\Omega$ at $f = 100\text{ Hz}$ and above $20\text{ k}\Omega$ at $f = 10\text{ kHz}$, which is enough for the target biomedical instrumentation amplifier. It should be pointed that this good performance was achieved with a feedback OTA powered with only 20 nA that is less than 1% of the nominal current of the mirror; such a low current was selected as a proof of concept to demonstrate that the excess power consumption can be truly insignificant, but still preserve mirror characteristics. It should be pointed that while the active current mirror operates down to a 80 mV voltage drop, the OTA is powered by the full supply voltage V_{DD} ; thus, it is important to reduce its current consumption. (V_{DD} nominal value is 3 V , but the OTA and active mirror were tested with no problems down to $V_{DD} = 1.8\text{ V}$.) At the end some conclusions are presented, including some simulations and measurements on a differential pair biased with the developed current mirror, showing that active current mirrors can be a valuable tool in the design of low voltage analog circuits.

2 Active Current Mirror Analysis

Several non-idealities can affect the performance of the current mirror in Fig. 1b, such as the limited bandwidth, noise, offset. In this section some of them are studied starting with offset and noise. The non-idealities will ultimately set the design criteria.

2.1 Offset

The input offset of the OTA as well as the resistors' mismatch in Fig. 1b will introduce a random inaccuracy in the output current $\Delta I = I_{\text{Out}} - I_{\text{In}}$ equal to:

$$\Delta I = \frac{V_{\text{osOTA}}}{R} + \frac{\Delta R \cdot I}{R + \Delta R} \approx \frac{V_{\text{osOTA}}}{R} + \frac{\Delta R \cdot I}{R}. \quad (1)$$

V_{osOTA} is the OTA's input referred offset, $R = R_1 \approx R_2 (N = 1)$, ΔR is the resistors' mismatch, and $I = I_{\text{Out}} \approx I_{\text{In}}$. Calculating the standard deviation (SD) on Eq. (1):

$$\frac{\sigma_{I_{\text{Out}}}}{I_{\text{Out}}} = \sqrt{\left(\frac{\sigma_{V_{\text{osOTA}}}}{R \cdot I_{\text{Out}}}\right)^2 + \left(\frac{\sigma_R}{R}\right)^2} = \sqrt{\left(\frac{\sigma_{V_{\text{osOTA}}}}{V_{\text{Drop}}}\right)^2 + \left(\frac{\sigma_R}{R}\right)^2}, \quad (2)$$

where $\sigma_R/R \approx 1-5\%$ depends on R_1, R_2 physical size and V_{Drop} is the DC voltage drop in the resistors as indicated in Fig. 1b. From our previous experience, V_{osOTA} is in the mV order with a careful design and layout of the OTA ($V_{\text{osOTA}} \sim 0.5-5$ mV in [7,8]). At this point it is worth mentioning that Eq. (2) sets up a basic design criterion: for a given acceptable error, the first term in Eq. (2) sets up a lower limit for V_{Drop} and thus the resistor value. In comparison with Eq. (2), for the standard mirror in Fig. 1a the current error is:

$$\frac{\sigma_{I_{\text{Out}}}}{I_{\text{Out}}} \approx \frac{g_m \cdot \sigma_{V_T}}{I} \approx 25\sigma_{V_T}, \quad (3)$$

where g_m is the transconductance of the transistors. The last approximation in Eq. 3 is for M_2, M_3 transistors in weak inversion (WI) as usual in low-voltage design. σ_{V_T} is the SD of the transistors' threshold voltage and is possible to assume that it is in the order of σ_{osOTA} . So, for a V_{Drop} down to 40 mV and using well-matched resistors, the expected offset of the active mirror is in the order of that of a classic 2-transistor current mirror.

2.2 Noise

Only white noise will be considered for the noise analysis, but it can be later extended to flicker noise also. There are three noise sources in the circuit shown in Fig. 1b: two resistors and the feedback OTA as depicted in Fig. 3. Each resistor's noise power spectral density (PSD) is:

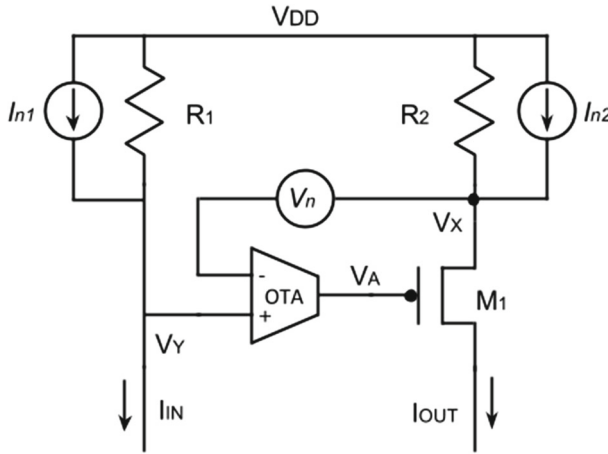


Fig. 3 Active mirror noise analysis

$$S_{IR} = \frac{4k_B T}{R}, \tag{4}$$

where k_B is the Boltzmann's constant and T is the absolute temperature. In the case of a symmetrical OTA like in Fig. 1b, the input referred noise S_{nOTA} is calculated assuming all the transistors in WI [5]:

$$S_{nOTA} = \frac{8\gamma n k_B T}{G_m}, \tag{5}$$

where the product $\gamma \cdot n \approx 4$ and G_m is the transconductance of the OTA. The noise PSD of the output current in the active mirror can be calculated propagating the noise sources in Fig. 3 to the output:

$$S_{IOut} = \frac{8k_B T}{R} + \frac{8\gamma n k_B T}{G_m R^2}. \tag{6}$$

In the circuit shown in Fig. 2b, apart from the differential pair, only the active current mirror at the bottom introduces noise. To determine whether the noise sources in Eq. (6) are relevant or not to this circuit, we can compare it to the noise current S_{Ipair} introduced by the differential pair of Fig. 2b:

$$S_{Ipair} = 2\gamma n k_B T g_{mpair}. \tag{7}$$

In the case of the resistors noise, assuming the differential pair in WI with $g_{mpair}/I_D \sim 25$ [9,10] and using Eq. (4):

$$\frac{S_{IR}}{S_{Ipair}} = \frac{1}{R I_D (g_{mpair}/I_D)} \approx \frac{1}{V_{Drop} \times 25}. \tag{8}$$

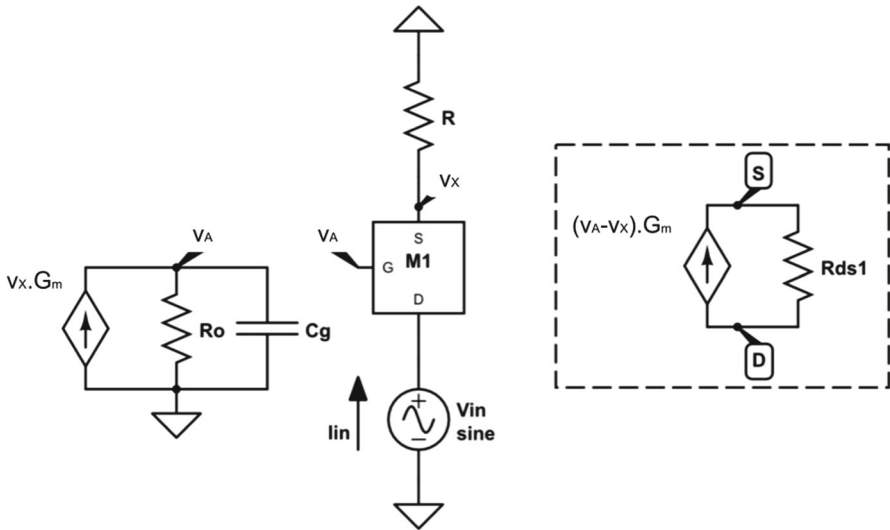


Fig. 4 Small signal equivalent of an active mirror, to calculate the output impedance. Using the proper values for g_{m1} and R_{DS1} , the model is valid for all the operating regions of M_1 from WI to SI and in the linear region

In the case of the noise in Eq. (5) introduced by the OTA:

$$\frac{S_{IOTA}}{S_{Ipair}} = \frac{2}{G_m R^2 g_{mpair}} = \frac{2\alpha}{(V_{Ddrop} \times 25)^2}. \tag{9}$$

Equation (9) assumes a factor $\alpha > 1$ relating the mirror current and the OTA's bias current $I = \alpha \cdot I_{biasOTA}$, with $\alpha \gg 1$ to make the power consumption of the OTA small in comparison with the active mirror. An important conclusion taking into account Eqs. (2), (8), and (9) is that both the offset and noise of the active current mirror are smaller with bigger V_{Ddrop} . But the impact of noise is not relevant for a reasonable V_{Ddrop} and α values.

2.3 Output Impedance, Bandwidth, Stability

The output impedance, bandwidth, and stability of an active current mirror can be studied by means of a small signal analysis. Figure 4 shows the small signal equivalent circuit to calculate the output impedance, with an auxiliary source at the output. The small signal output impedance is calculated as $z_{Out} = v_z/i_z$. The incoming current is calculated as follows:

$$i_z = -g_{m1} (v_A - v_X) + \frac{(v_{In} - v_X)}{R_{DS}}. \tag{10}$$

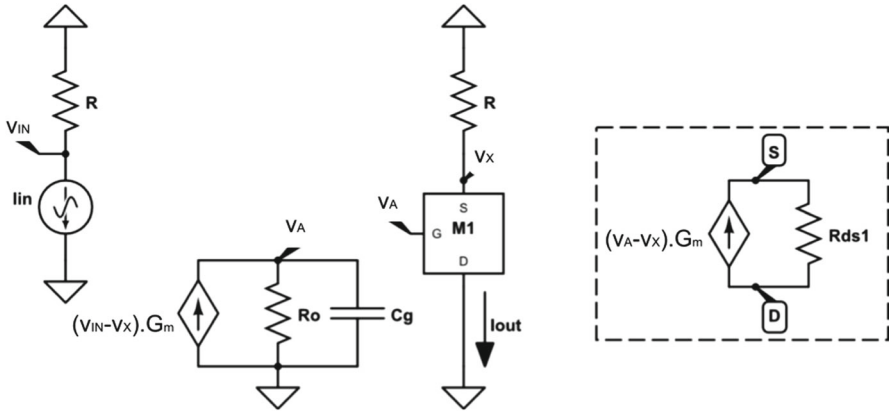


Fig. 5 Small signal analysis of an active mirror, to study the mirror's bandwidth

And the output impedance:

$$z_{Out} = R + R_{DS} + R \cdot R_{DS} \cdot g_{m1} \cdot \left(\frac{G_m \cdot R_o}{1 + R_o C_G s} - 1 \right), \quad (11)$$

where R_{DS} , C_G , and g_{m1} are, respectively, the small signal output resistance, gate capacitance, and gate transconductance of M_1 transistor. The problem to evaluate Eq. (11) is to calculate the small signal parameters R_{DS} , C_G , g_{m1} , because they are very different depending on whether the transistor M_1 operates in saturation region or in the linear region. Both conditions of M_1 are possible in an active current mirror. Although it is possible to consider a continuous model valid in all regions like the one in [8] to estimate R_{DS} , g_{m1} , C_G , etc., it was not possible to establish analytic design equations. Because of the wide different situations depending on the mirror current, the output voltage, and resistor values, it was not possible to further develop Eq. (11). On the other hand, it is clear in Eq. (11) that the active current mirror's output impedance is highly increased at low frequencies in comparison with that of a classic current mirror (in the order of R_{DS}). Later in this work some simulations will be presented to further illustrate the behaviour of the output impedance in an active current mirror.

The analysis of the mirror bandwidth is similar; Fig. 5 shows the small signal equivalent in this case with an auxiliary source at the input. The transfer function is calculated as:

$$\frac{i_{Out}}{i_{In}} = \frac{R \cdot g_{m1} \cdot A}{1 + \frac{R}{R_{DS}} + R \cdot g_{m1} \cdot (A + 1)}, \quad (12)$$

where $A = \frac{g_m \cdot R_{DS}}{1 + R_{DS} C_G s}$ is the feedback loop's gain. Since the product $g_m \cdot R_{DS}$ is large, $i_{Out} = i_{In}$ at low frequencies. Once again, while it was not possible to advance in a simple way on Eq. (12), simulations were preferred to evaluate the active current mirror bandwidth because of the wide different situations depending on the mirror current, the output voltage, and resistor values. Later in this work some simulations will be

presented to further illustrate the behaviour of the active current mirror's bandwidth. Finally, the open loop gain was calculated and simulated to check that the system is stable, showing a good phase margin in all the simulations performed at different bias conditions and operating regions for M_1 .

3 A 1:200, 10- μ A Output Active Current Mirror

A 10- μ A (output-nominal) 1:200 active current mirror was designed, fabricated, and measured; a schematic is shown in Fig. 6. Initial specifications are as follows: the total voltage drop V_C must be 100 mV or less, the total current consumption of the feedback OTA must be less than 1% the nominal output current, and the mirror bandwidth must be larger than 5 kHz. Such a low OTA current is arbitrary, and it was selected that low as a proof of concept, to demonstrate the operation of the active mirror with a negligible extra power consumption. This current mirror is aimed at substituting a current source like the upper one in Fig. 2b; thus, a large copy factor was selected to reduce the current consumption on the left branch in Fig. 6. With the large 1:200 copy ratio, it requires only 50 nA at the input to achieve a 10- μ A output.

The resistors' values were selected to have a voltage drop $V_{Drop} = 50$ mV for $I_{Out} = 10 \mu\text{A}$, as a good trade-off between reducing the voltage drop and current copying error as per Eq. (2). M_1 was designed to have an equivalent resistance of 1.2 k Ω (linear region) when $V_A = V_{DD}/2$ which allows a very small voltage drop V_{DS1} of only 12 mV in the transistor in the worst-case condition. The final M_1 size was $W_1/L_1 = 100 \mu\text{m}/4 \mu\text{m}$. The feedback OTA is a symmetrical OTA like in Fig. 1 consuming only 20 nA.

The circuit was implemented in a 0.6- μm CMOS technology, occupying a total area of 0.1 mm². Approximately 2/3 of the area corresponds to the OTA, because large input transistors are necessary to reduce the input referred offset to the range of 1 mV [1], [2], and the rest of the area are the resistors and M_1 transistor. A microphotography of the circuit is shown in Fig. 7.

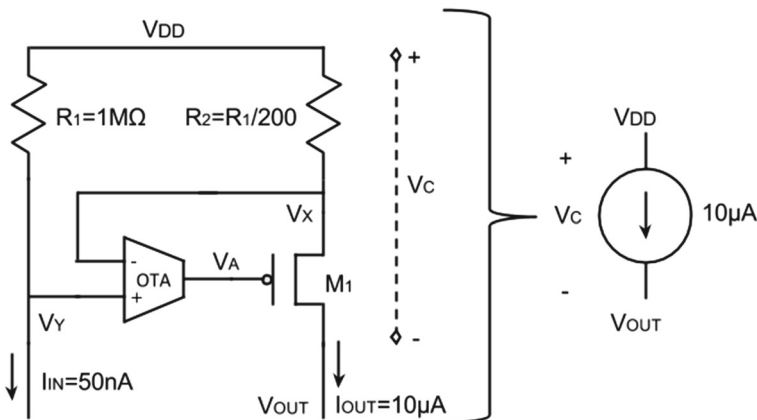


Fig. 6 Implementation of the current mirror with a 200:1 relation between currents

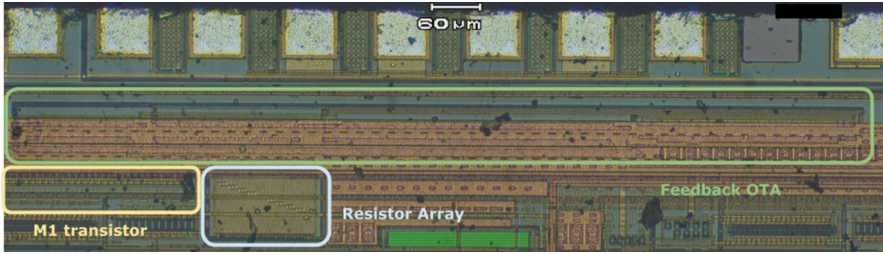


Fig. 7 Microphotography of the active mirror

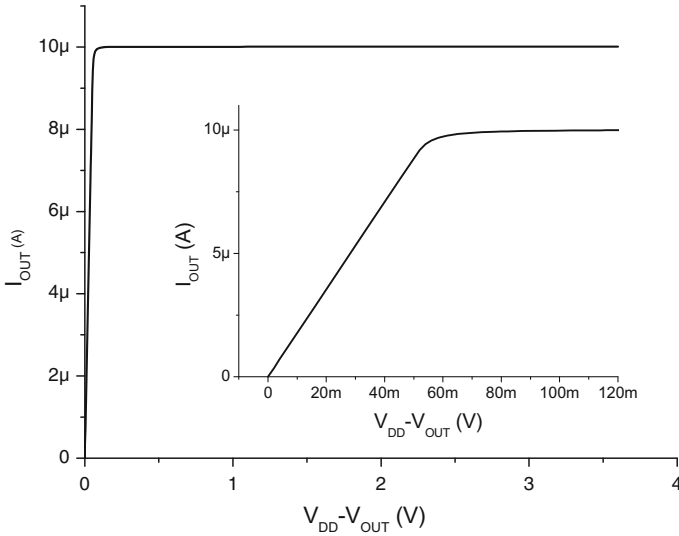


Fig. 8 Simulated output current as a function of the voltage drop $V_C = V_{DD} - V_{OUT}$ in the current mirror

To reduce mismatch, it is very important to properly match R_1 and R_2 resistors. Therefore, both were implemented with an interleaved array of unitary resistors, extending the series–parallel association of transistors in [2] to the resistor case. R_2 was implemented using 10 unitary resistors $R_u = 50 \text{ k}\Omega$ in parallel, and R_1 with 20 unitary resistors in series. Using Eq. (2), and the mismatch models provided by the foundry, the expected variation is $\sigma_{I_{Out}}/I_{Out} = 2\%$. Figure 8 shows the simulated output current as a function of the total voltage drop V_C at the output. It should be pointed out that in the simulation just 65 mV is necessary for the active mirror to accurately copy the input to the output (in comparison with a few hundred mV in the case of a classic current mirror). The measured output current as a function of the total voltage drop V_C is shown in Fig. 9; in this case, a voltage drop $V_C \geq 85 \text{ mV}$ is necessary for the active mirror to operate.

The output impedance depends on the voltage drop V_C and is much higher near DC than in a classic mirror, being especially noticeable for a low drop V_C . In Fig. 10 several simulated plots are shown comparing the output impedance for both the designed

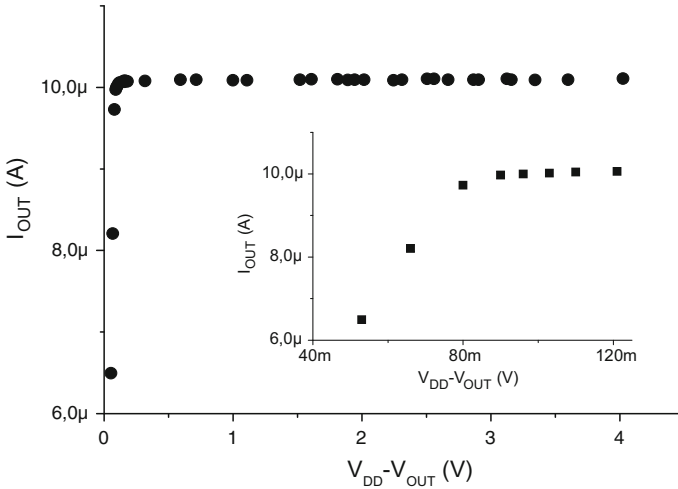


Fig. 9 Measured output current as a function of the voltage drop $V_C = V_{DD} - V_{OUT}$ in the current mirror. It works correctly with just 85 mV

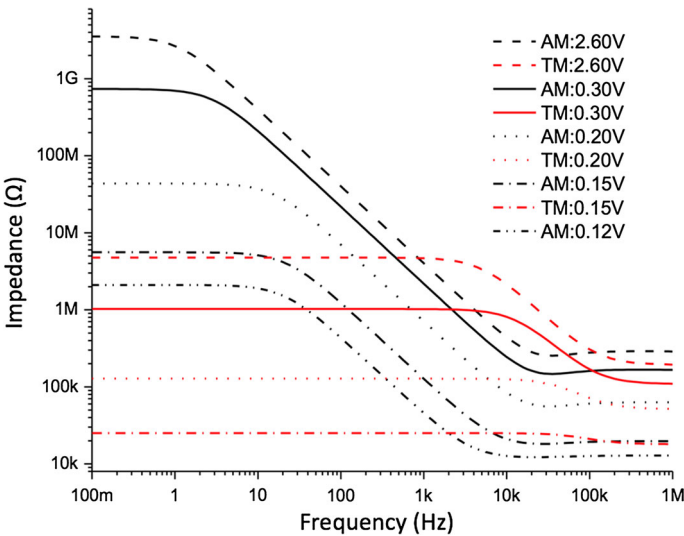


Fig. 10 Output impedance z_{OUT} as a function of frequency and V_C for both an active mirror (AM) and a 2-transistor mirror (TM)

active mirror (AM) and a classic 2-transistor mirror (TM), the latter using $W/L = 100 \mu\text{m}/4 \mu\text{m}$ transistors. Each plot is the result of a different AC SPICE simulation while varying V_C .

In the case of the active mirror, a simple way to enhance the output impedance at the higher frequencies is to increase the bias current of the OTA, as depicted in Fig. 11. Also the OTA transconductance value determines the bandwidth of the active current mirror, because it determines the speed of the OTA to charge/discharge the gate of the

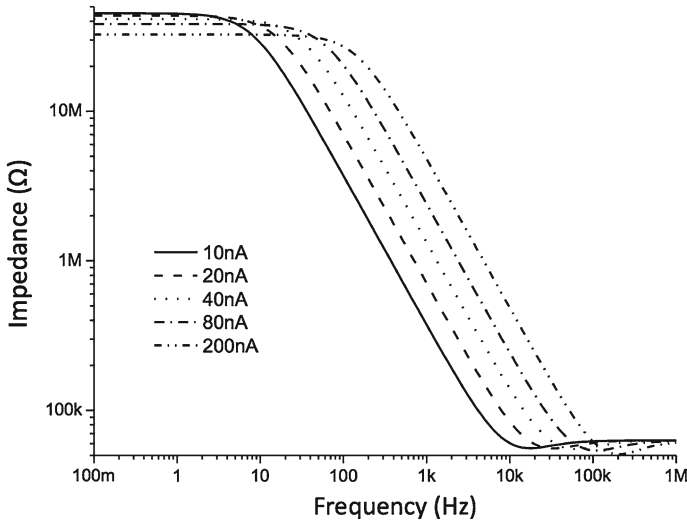


Fig. 11 Output impedance versus frequency for different OTA total current consumption values

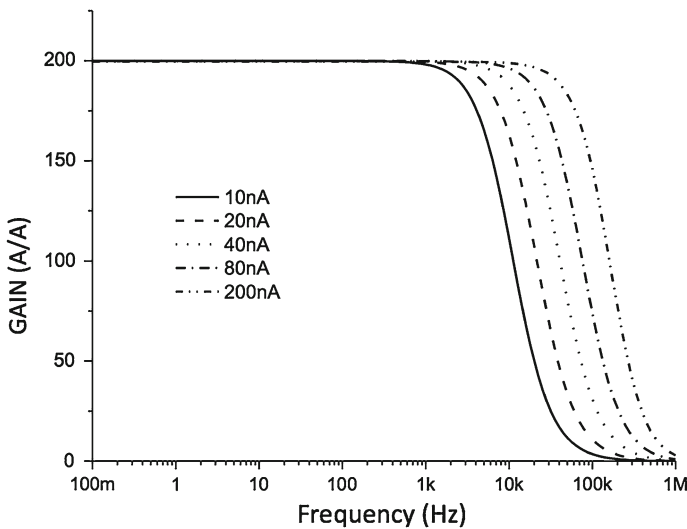


Fig. 12 Gain versus frequency for different OTA total current consumption values

pass transistor M_1 . In Fig. 12 a simulation of the transfer function of the current mirror is presented while varying the OTA bias current, showing its effect on the bandwidth. For a bandwidth of 10 kHz, only 20 nA of total consumption is necessary.

Finally, in Fig. 13 the measured output impedance at different frequencies is presented for a small drop V_C of only 125 mV, showing a good degree of agreement with the corresponding plot in Fig. 10. Figure 14 shows the measured output current for different input currents. The linear approximation of this particular sample has a gain of 196 A/A with a $R^2 = 0.998$.

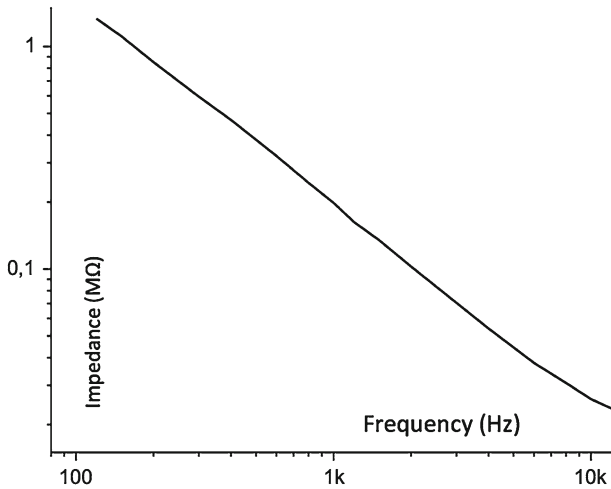


Fig. 13 Output impedance for a voltage drop V_C of just 125 mV

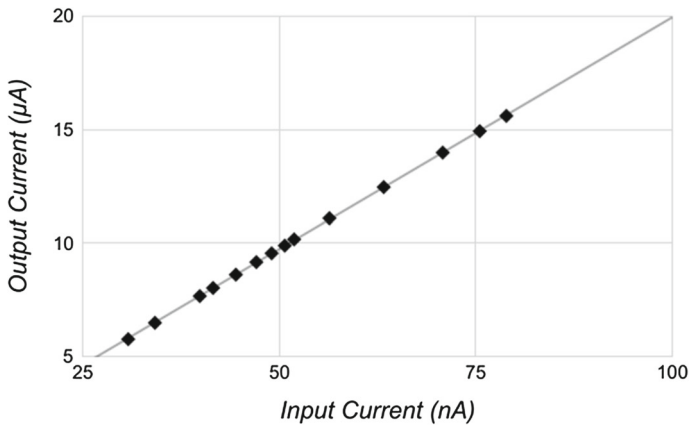


Fig. 14 Output current for different input currents. In this sample the current gain is 196 A/A, while $R^2 = 0.998$

4 A Low-Voltage OTA Using Active Current Mirrors

Two similar $200 \mu\text{A/V}$ (nominal) active transconductors are compared in this section: the first one is a standard symmetrical OTA with a $20 \mu\text{A}$ bias current and using classic current mirrors, and the second one replacing all the mirrors with active ones, the latter is shown in Fig. 15. The differential pair is the same in both circuits, using NMOS transistors sized $W/L = 400 \mu\text{m}/2 \mu\text{m}$ operating in WI, while the classic and active current mirrors were designed to reduce the current copy error below 2% to preserve a reduced offset. Figure 16 shows the comparison of the layout of both OTAs. (The circuits were fabricated and measured, but there is no available photograph.) Symmetrical feedback OTAs like in Fig. 1 were used in the active mirrors consuming

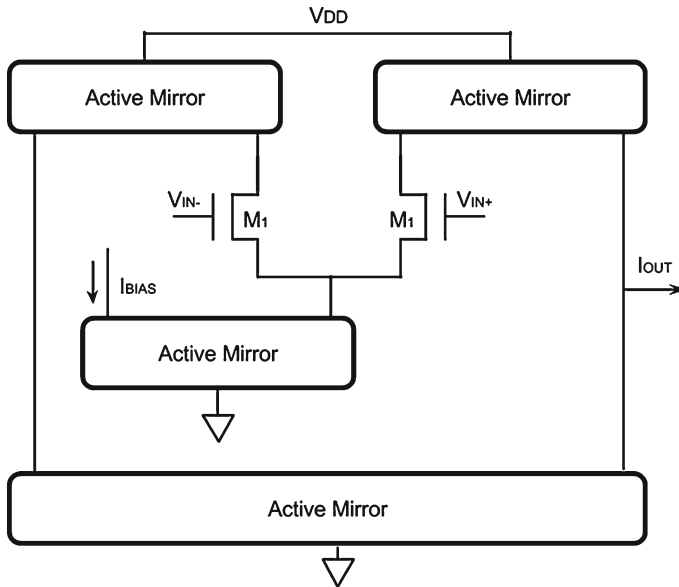


Fig. 15 Schematic of the symmetrical OTA with active mirrors

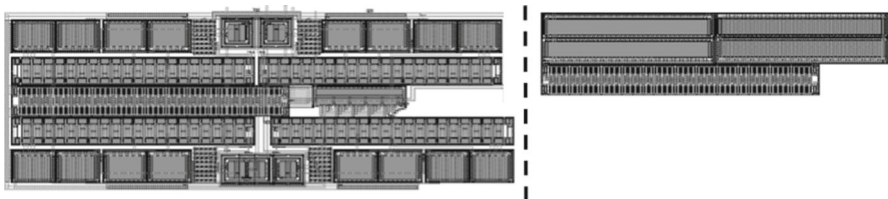


Fig. 16 Layout image of the symmetrical OTA using active mirrors (*left*) and classic mirrors (*right*). The first OTA on the *left* requires 3 times more area

100nA each. (For the active mirrors connected to GND, PMOS input OTAs were used.) In Fig. 17, the simulated total harmonic distortion (THD) of both OTAs is presented, for different supply values. There is, in practice, no difference for a high enough supply voltage, which suggests the main contributor is the differential pair, but for lower voltages, the standard OTA has higher distortion, while the active mirror OTA continues to have the same THD for much smaller supply voltages. The circuits were fabricated and measured. Table 1 shows a comparison including measured and simulated results for both circuits. The transconductance, current consumption, and input referred offset are almost the same in both cases. The area is much smaller in the case of the transconductor using classic current mirrors, but there is a noticeable increase in the CMRR in the case of the active current mirrors due to the higher output impedance of the mirrors. But the most important result is that the transconductor using active current mirrors operates down to a 650mV supply voltage (a criterion of a reduction of less than 10% in the transconductance was selected as an indication of the OTA still working correctly), which is almost a third of the case of the first

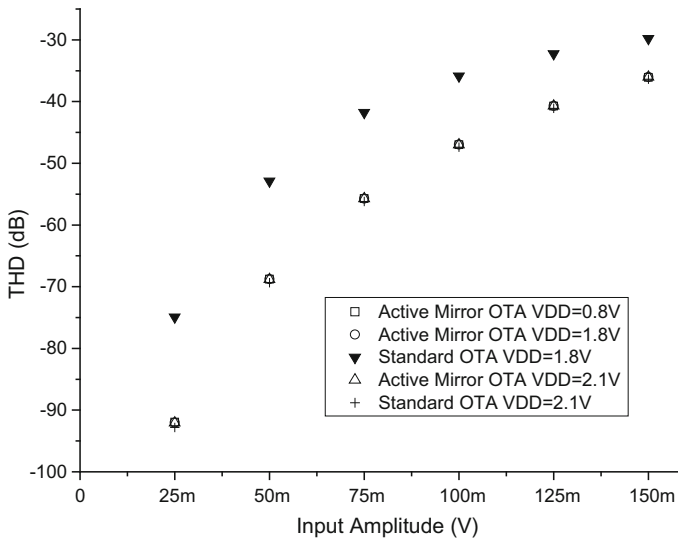


Fig. 17 Simulated total harmonic distortion (THD) of both OTAs. There is almost no change for a high supply voltage, suggesting the THD is introduced by the differential pair. For low supply values only the active mirror OTA continues to work correctly

Table 1 Measured (M) and simulated (S) characteristics of both OTAs

	Standard OTA	Active mirror OTA
Transconductance (M)	205 μ S	212 μ S
Current consumption (M)	40 μ A	40.5 μ A
Area	0.05 mm ²	0.15 mm ²
CMRR @ 1 kHz (S)	146 dB	193 dB
Minimum V_{DD} (M)	1.80 V	0.65 V
Offset voltage (M)	350 μ V	250 μ V

transconductor using the 2-transistor mirrors. These results prove that the active mirror is a very useful block to implement low-voltage circuits.

5 Conclusions

While the introduction of a really new circuit technique is very rare nowadays, there are still some under explored issues in analog design, an example being the use of active current mirrors with resistors to reduce the supply voltage of analog circuits. The performance trade-off in the design of active current mirrors was investigated, including an analytical study, simulations, and measurements on fabricated circuits. It is possible to conclude that active current mirrors are a valuable circuit block to implement very low voltage circuits even in CMOS technologies with a high threshold voltage. First, the impact of some non-idealities such as noise, offset, output impedance, bandwidth

was estimated, showing that under certain circumstances it is possible to substitute a classic two-transistor mirror by an active current mirror, with a negligible loss of performance, but with the consequent advantages in supply voltage reduction. Active current mirrors exhibit also a gigantic output resistance near DC, but on the other hand cannot be implemented with a minimum area. It was demonstrated that the mirror's current noise and offset are related to the voltage drop V_{Drop} in the sensing resistor R_2 and that a drop as low as $V_{\text{Drop}} \approx 40$ mV is enough (combined with well-matched resistors) to reduce the noise and offset to those of a classic 2-transistor current mirror. Furthermore, the pass transistor can operate in both saturation and linear regions; thus, the total voltage drop of an active current mirror can be less than 100 mV.

Some design criteria for active current mirrors were presented, as well as the design of a 10- μA (nominal) active current mirror. The circuit was fabricated in a 0.6- μm technology with threshold voltages $V_{\text{TN}} = 0.90$ V and $V_{\text{TP}} = 0.95$ V for the NMOS and PMOS, respectively. The circuit was tested, showing the expected low-voltage operation down to a minimum total voltage drop of almost 80 mV and very high output impedance at low frequencies. The measured offset was less than 200 nA, and the measured output impedance was 2 M Ω at $f = 100$ Hz. The feedback OTA consumes only 20 nA from the battery; while such a low current limits the overall mirror bandwidth to 20 kHz, it serves to demonstrate that an active current mirror can be implemented with a negligible additional power consumption. The 20 kHz bandwidth is more than enough to the target biomedical amplifier where the active current mirror is intended to be used.

Finally, a few simulations and measurements of the differential input stage of an amplifier, where the 2-transistor mirrors were substituted by a 20- μA active mirror, were presented. At a 20 μA bias current both exhibit similar characteristics, but the circuit using active mirrors was measured to properly work down to $V_{\text{DD}} = 0.65$ V supply voltage, in comparison with a much larger minimum $V_{\text{DD}} = 1.80$ V in the case using the classic current mirrors.

The design of classic current mirrors is rather trivial in comparison with an active current mirror and probably will occupy a small die area in comparison with its active equivalent. But despite that, critical current mirrors in an analog circuit (especially those copying a large current) can be implemented utilizing the active topology with a remarkable supply voltage reduction, and perhaps an output impedance gain or noise reduction.

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