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Deep electron traps in HfO_2-based metal-oxide-semiconductor capacitors

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ABSTRACT

Hafnium oxide (HfO_2) is currently considered to be a good candidate to take part as a component in charge-trapping nonvolatile memories. In this work, the electric field and time dependences of the electron trapping/detrapping processes are studied through a constant capacitance voltage transient technique on metal-oxide-semiconductor capacitors with atomic layer deposited HfO_2 as insulating layer. A tunneling-based model is proposed to reproduce the experimental results, obtaining fair agreement between experiments and simulations. From the fitting procedure, a band of defects is identified, located in the first 1.7 nm from the Si/HfO_2 interface at an energy level $E_t = 1.59$ eV below the HfO_2 conduction band edge with density $N_t = 1.36 \times 10^{19}$ cm^{-3}. A simplified analytical version of the model is proposed in order to ease the fitting procedure for the low applied voltage case considered in this work.

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1. Introduction

In recent years, much effort has been made in order to improve the program/erase performance and data retention of nonvolatile Flash memories beyond the 30 nm generation. The incorporation of high-κ dielectrics seems essential to this purpose. Particularly, hafnium oxide (HfO_2) was proposed as interpoly dielectric in replacement of SiO_2 in order to increase the control gate-floating–gate coupling ratio without reducing the oxide thickness, and thus avoiding the increase in leakage current [1–3].

Due to the stress-induced leakage current, cell-to-cell parasitic interference, and the need to wrap-around the floating-gate, the conventional floating-gate Flash memories would be replaced by charge-trapping nonvolatile memories [4], in which the charge is stored in discrete traps located inside a trapping layer. In this case, HfO_2 was proposed to replace SiO_2 as tunnel layer, which favors the charge injection due to the 1.5 eV electron tunneling barrier compared to the 3.2 eV in the case of SiO_2 [5]. HfO_2 was also considered to replace SiO_2 as blocking layer [5–7], ensuring an adequate capacitance value without reducing the oxide thickness. The combination of the two previous proposals results in the TaN/HfO_2/Ta_2O_5/HfO_2/Si structure [5]. However, since HfO_2 has an electron trap density many orders of magnitude higher than that of SiO_2 [8,9], the data retention could be seriously affected by low-field leakage current due to trap-assisted tunneling [10]. To solve this problem, a TaN/Al_2O_3/Ta_2O_5/HfO_2/Si structure was proposed, which has a better blocking efficiency due to the Al_2O_3 much larger barrier height [5].

HfO_2 was also proposed as trapping layer in charge-trapping memories as a replacement of conventional Si_3N_4, giving place to the metal/Al_2O_3/HfO_2/SiO_2/Si [11,12], showing a superior charge-storage capability at low voltages, faster programming, and less over-erase problems compared to conventional poly-Si/SiO_2/Si_3N_4/SiO_2/Si devices [13].

This paper contributes with experimental results through constant capacitance voltage transient (CCVT) measurements. This technique allows sensing deep traps and prevents the generation of new traps inside the dielectric. A physical model, previously developed for the study of electron traps in Al_2O_3 is used to get information on the energetic and spatial distributions of the deep electron traps inside the dielectric.

2. Experimental details

2.1. Samples description

Metal-oxide-semiconductor (MOS) capacitors with HfO_2 grown by atomic layer deposition (ALD) as insulating layer were studied. The samples were fabricated on an n-type silicon wafer with resistivity of

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1–12 Ω cm (phosphorous doping concentration of 4×10^{14} – 5×10^{15} at/cm^3). A field oxide of 400 nm was grown by thermal oxidation at 1100 °C and windows were opened for the HfO_2 ALD by photolitography and wet etching. Before deposition, the samples were first cleaned for 10 min with H_2O_2/H_2SO_4 followed by a 10 s dip in HF. The deposition equipment was a Cambridge NanoTech Savannah 200. The ALD process was performed at 225 °C and consisted in 100 ALD cycles, using tetrakis dimethylamido-hafnium (TDMAH) and water (H_2O) as precursors. Each ALD cycle was composed of a H_2O pulse of 30 ms, a N_2 purge for 6 s, a TDMAH pulse of 150 ms and a N_2 purge for 5 s. The process resulted in an oxide thickness of 10.5 nm, as measured by ellipsometry. Next, metalization with Al/(0.5%)Cu was performed. After patterning the metal layer by photolithography and wet etching, the back of the wafers was also metalized with aluminum for electrically contacting the silicon substrate. Finally, the wafers underwent a forming gas (N_2/(10%)H_2) annealing step at 350 °C for 20 min. The area of the obtained device was 3.24×10^{-4} cm^2. Fig. 1 shows a schematic cross-section of the fabricated device structure. The samples were characterized by transmission electron microscopy. The capacitance equivalent thickness of the HfO_2 layer was 3.4 nm [14]. A SiO_x interfacial layer (IL) was reported as a sub-product of ALD growth on Si [15]. We could not detect its presence through microscopy; we could neither exclude its presence.

2.2. Measurement technique and results

Successive cycles of capacitance–voltage (C–V) measurements at 1 MHz were performed with a computer controlled HP 4277A LCZ meter. Each C–V cycle consists of a first sweep from inversion at an applied bias (V_G) of −0.5 V to accumulation (V_G = 1 V) and back in the opposite direction. Fig. 2 shows the obtained curves along the first three cycles for a virgin device or after a sufficiently long (about 1 day) rest at room temperature.

The hysteresis is interpreted as electron capture in preexisting defects, also called hysteresis traps [16], inside the insulator during the sweep from inversion to accumulation, and the corresponding detrapping in the opposite direction. An interface states density of ~10^{12} cm^{-2} eV^{-1} was obtained through the stretch-out of the C–V curves.

The fact that the first sweep from inversion to accumulation differs from subsequent sweeps in the same direction implies that a fraction of electrons captured during the first C–V cycle are not discharged when the device reached the minimum voltage (V_G = −0.5 V), at the end of the sweep from accumulation to inversion. If the device is left unbiased for approximately 24 h, this fraction of electrons is detrapped and the subsequent sweep from inversion to accumulation results in the first cycle curve again. It is observed that while the accumulation to inversion C–V curve is the same regardless the number of C–V cycles performed, leading to the assumption that no new defects are generated during C–V cycles; the accumulation to inversion C–V curve

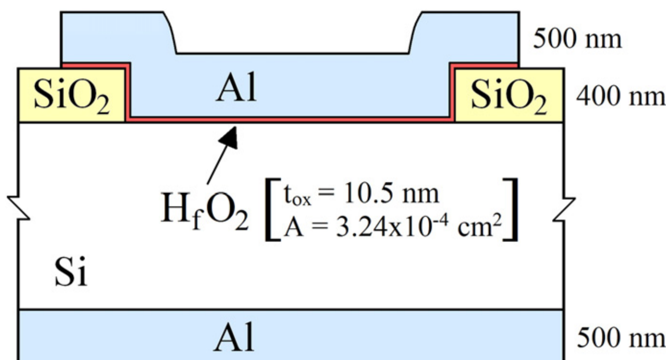

Fig. 1. Schematic cross-section of Al/HfO_2/Si stack.

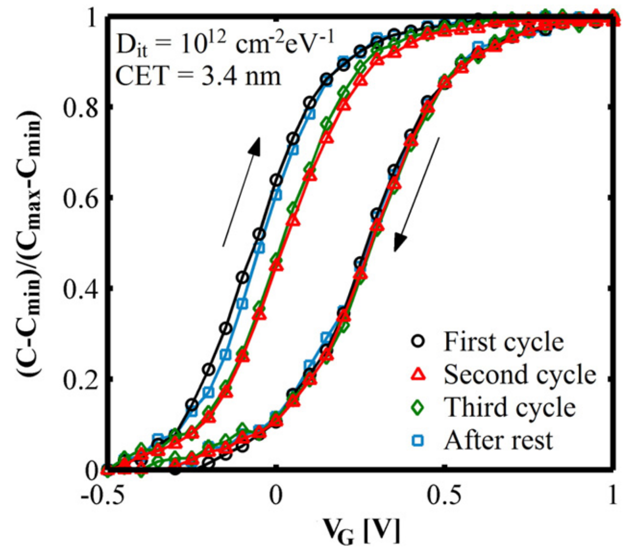

Fig. 2. Experimental first three C–V cycles for a virgin device or the corresponding one after a sufficiently long rest (one day at room temperature).

depends on the maximum voltage reached at the end of the inversion to accumulation sweep (Fig. 3), as reported by other groups [17,18]. This voltage dependence would be a consequence of an energetic distribution of electron traps, so that as bias increases, the Fermi level approaches the silicon conduction band edge, allowing for traps at higher energy levels to be filled by tunneling. Another possible explanation for this dependence is related to the fact that when the maximum voltage applied at accumulation increases, the sweep takes longer, which implies that tunneling affects traps far from the interface with the substrate. The latter possibility should be neglected for two reasons. First, the sweep time increases linearly with the maximum applied voltage, so that the hysteresis depends linearly with time. This dependence is not consistent with the usual log(t) dependence for the kinetics of tunneling processes (see Fig. 5 below). Moreover, from modeling (see Section 3), the discharges of traps filled during sweeps from different maximum applied voltages cover the same spatial region.

In order to gather information about the trapping/detrapping kinetics a complementary experiment was performed consisting of tracking the evolution of the voltage corresponding to a fixed capacitance (V_C)

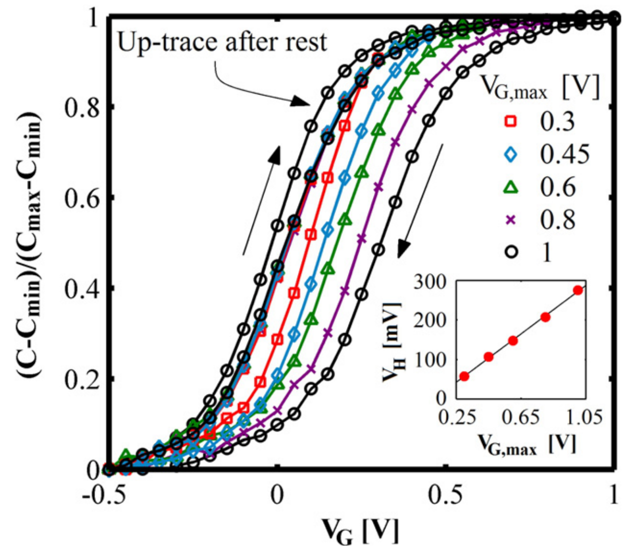

Fig. 3. C–V cycles with different maximum voltages $V_{G,max}$ at accumulation. It is observed that the hysteresis value V_H increases as $V_{G,max}$ increases, following a linear dependence as shown in the inset.

with time until its stabilization. The experiment was performed starting a C–V curve once at $V_G = -0.5$ V and the others at 0.2, 0.6, and 1 V until the capacitance reached the reference value when the tracking begins (Fig. 4). As the applied bias is very low during these measurements, only traps fairly aligned with the substrate Fermi level are charged/ discharged and no trapping at shallow defects occurs. This allows us to confirm the presence of deep electron traps within the dielectric. Additionally, low electric field prevents the generation of new defects inside the dielectric. However, as bias is limited to the high-derivative region of the C–V curve, this technique is not adequate to acquire the trap distribution in a wide energy range, as other measurement techniques do, as pulsed I–V [16,17], charge injection and sensing (CIS) [19], two-pulse C–V [20,21], and discharge-based multipulse [22]. As a comparison, the two-pulse C–V technique allows to extract the energetic distribution of electron traps below silicon conduction band edge, but it requires several stress stages during which the electron traps are filled, which can generate new defects. The discharge-based multipulse technique overcomes the problem of the stress because traps are filled one time and extends the probing region to energies lying both below and above silicon conduction band edge.

Fig. 5 shows the resulting $\Delta V_C(t)$ curves for the CCVT measurements. As one can see from this figure, the transient after the device is biased in inversion ($V_G = -0.5$ V) has a positive ΔV_C value indicating the charging of the electron traps, while the other three $\Delta V_C(t)$ curves, all of them after the device is biased in accumulation ($V_G = 0.2$, 0.6, and 1 V), have the opposite sign, indicating the discharging of the electron traps. Despite the direction, all the dynamics converge to the same final ΔV_C value, indicating that a steady-state condition exists for a given capacitance value.

Besides, for short times, the four $\Delta V_C(t)$ curves exhibit a slope linear with log(t), which is consistent with the tunneling front theory [23,24]. The same behavior was previously observed by other groups [25,26].

3. Modeling

3.1. Theory

To reproduce the experimental results, a physical model previously used for describing electron trapping in Al_2O_3 layers is considered [27].

The density of trapped electrons $n_t(x,E_t,t)$ evolves according to

$$\frac{d}{dt}n_t(x,E_t,t) = \tau^{-1}(x,E_t)[N_t(x,E_t)f_s(x,E_t) - n_t(x,E_t,t)] \quad (1)$$

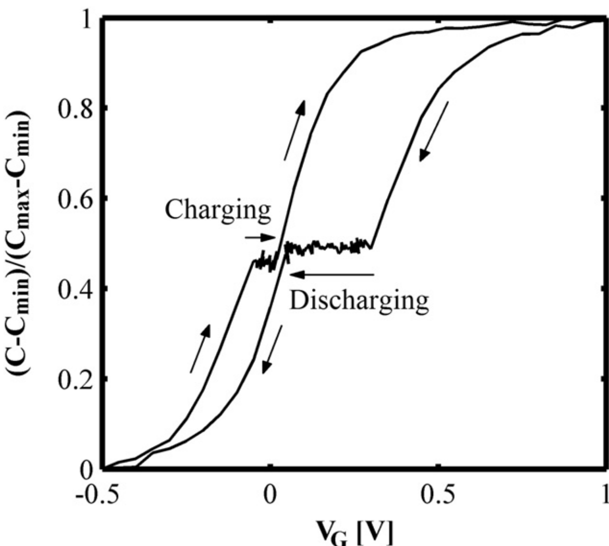

Fig. 4. The constant capacitance voltage transient measurements in the capacitance–voltage representation.

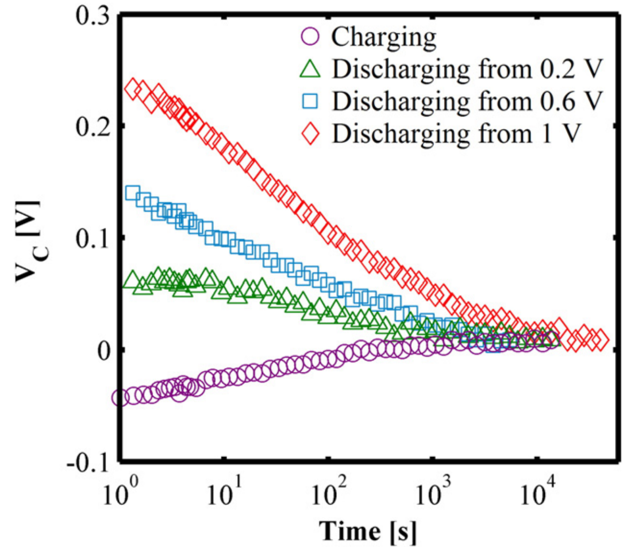

Fig. 5. Experimental V_C evolution with time for the charging and discharging processes.

where $N_t(x,E_t)$ is the density of traps, x is the position of the trap from the substrate–insulator interface, E_t is the absolute value of the energy level of the trap referred to the conduction band edge of the insulator, $f_s(x,E_t)$ is the Fermi–Dirac occupation probability according to the Fermi level at the substrate, and $\tau(x,E_t)$ is the tunneling time constant between the electronic states in the substrate and the electron traps, which can be evaluated using Bardeen's method [28], resulting in [29]

$$\tau(x,E_t) = \tau_0(x,E_t)\exp\left(2\int_0^x K(x')dx'\right) \quad (2)$$

where

$$K(x) = \sqrt{\frac{2m_{ox}E_t(x)}{\hbar^2}} \quad (3)$$

and m_{ox} is the effective mass of the electrons in HfO_2 and $\hbar$ is the reduced Planck constant. The prefactor $\tau_0(x,E_t)$ was reported to be relatively insensitive to applied fields [29], and was taken as a constant. A single trap level was assumed as a simplification to a narrow energy distribution.

We only considered interface states as the charge reservoir which interacts with the electron traps within the dielectric. Then, electron transitions from/to the silicon conduction band by some inelastic process, such as lattice relaxation multiphonon emission, are not considered. More details about that will be considered in Section 4.3.

Considering the exponential dependence of the tunneling time constants on the tunneling distance, and that the traps involved in the processes are distributed close to the Si/HfO_2 interface it is natural to neglect the tunneling contribution of the metal gate. This is the case for the experiments performed in this work as shown at the end of the next section.

Under the above simplification, Eq. (1) predicts that in steady-state condition, the traps in the insulator are in thermodynamic equilibrium with the substrate, sharing a unique Fermi level.

As mentioned in Section 2.1, a very thin IL could be present in our samples. It would affect the results by introducing an attenuation in the tunneling probability between substrate and traps. This attenuation would be almost constant along the low range of electric fields involved in our experiments, being absorbed in the prefactor τ_0 which is a fitting parameter of the model.

3.2. Simulations

A routine was developed in order to simulate the trapping/detrapping evolution according to the above theory. In each time step, the program uses the currently applied voltage and the spatial and energetic distribution of trapped electrons to update the two key parameters for the dynamic of the traps: the occupation probability and the tunneling time constant. With these inputs, a new spatial and energetic distribution of trapped electrons and the corresponding constant capacitance voltage shift are calculated and reinserted as entry values for the next step time. The simulation finishes when the simulation time reaches the duration of the experiments.

The following measured values were inputs for the model: The insulator capacitance per unit area $C_{ox} = 1.05 \times 10^{-6}$ F/cm^2, and the HfO_2 thickness $t_{ox} = 10.5$ nm. From the literature, we assumed for the conduction band offset $\Phi_C = 1.4$ eV [17,30–34], and for the effective electron mass in HfO_2 a value $m_{ox} = 0.18\ m_0$ [35–38]. A similar value $m_{ox} = 0.2\ m_0$ was also reported [17].

To determine the initial conditions, the hysteresis value was assumed as a measure of the trapped charge profile at the beginning of each CCVT measurement, with the inversion to accumulation curve from $V_G = -0.5$ V corresponding to all the traps emptied and the accumulation to inversion curve from $V_G = 1$ V to all the traps filled.

Fig. 6 shows the experimental ΔV_C vs. time curves together with the simulated ones exhibiting a good agreement.

The fitting procedure yields the values corresponding to the physical parameters involved in the trapping/detrapping processes: traps uniformly distributed in the first 1.7 nm close to the Si/HfO_2 with a density $N_t = 1.36\text{x}10^{19}$ cm^{-3} and an energy level $E_t = 1.59$ eV below the HfO_2 conduction band edge. Two different values were obtained for the pre-exponential factor τ_0, depending on whether the measurement begins in inversion (charging process, $\tau_0 = 0.1$ s) or accumulation (discharging processes, $\tau_0 = 0.7$ s). Fig. 7 shows the time evolution of the density of electrons in the traps during the charging process shown in Fig. 6(a).

4. Discussion

4.1. Simplified tunneling model

For a better understanding of the effects each physical parameter has on the charging/discharging dynamic, it is useful to have an analytical approximation relating the $\Delta V_C(t)$ curves with these parameters.

In view of the similarity of the results shown in Figs. 6 and 7 with the tunneling front theory, the model can be simplified under the following hypothesis:

- The applied voltage and the density of trapped electrons are low enough to neglect the electric field within the dielectric layer.
- The electron traps are uniformly distributed from the Si/HfO_2 interface up to a distance x_f into the dielectric.

The first hypothesis implies that the occupation probability and the tunneling time constant do not change significantly during the experiments. The second takes the form

$$\tau(x, E_t) = \tau_0 e^{2K(E_t)x} \quad (4)$$

With that, the solution of (1) can be approximated as

$$\Delta n_t(x, E_t, t) = N_t(x, E_t)\Delta f_s\left(1 - e^{\frac{t}{\tau(x,E_t)}}\right) \quad (5)$$

where Δf_s is the change in the occupation probability of the traps when the voltage is applied on the structure at the start of a CCVT measurement.

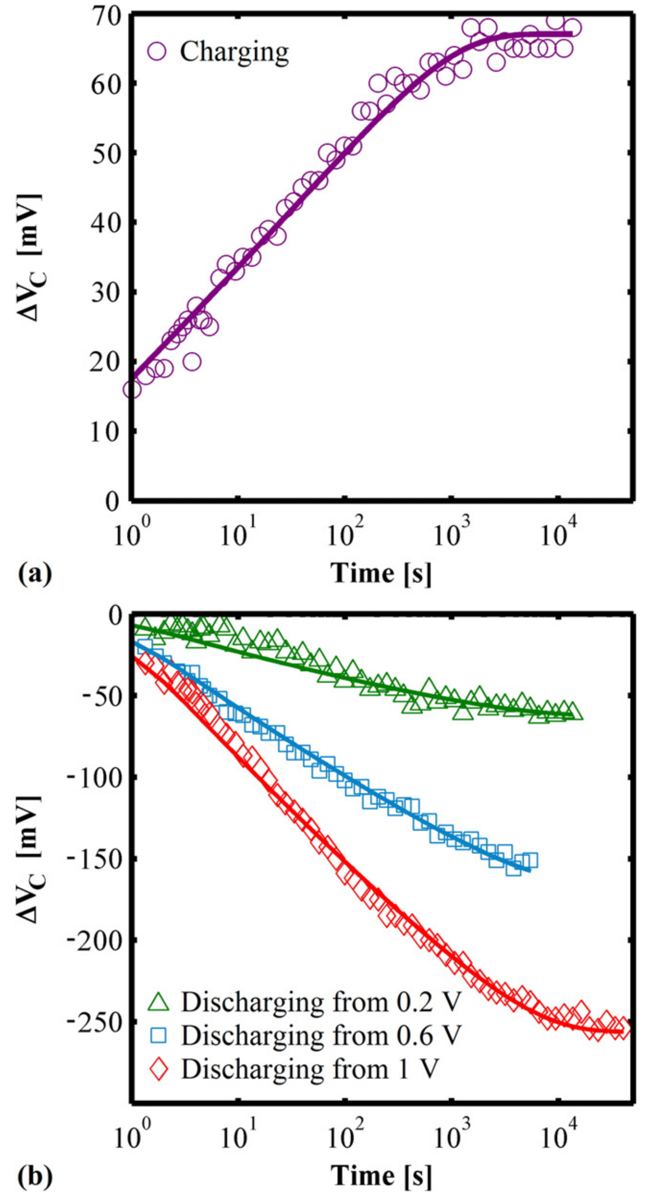

Fig. 6. Comparison between the experimental (symbols) and simulated (lines) ΔV_C vs. time curves for: (a) sweep beginning in inversion ($V_G = -0.5$ V); and (b) sweeps beginning in accumulation ($V_G = 0.2$, 0.6, and 1 V).

Considering the second hypothesis, the voltage shift for a constant capacitance $\Delta V_C(t)$, can be expressed as

$$\Delta V_c(t) = \frac{qN_t\Delta f_s}{C_{ox}}\int_0^{x_f}\left(1 - e^{\frac{t}{\tau(x,E_t)}}\right)\left(1 - \frac{x}{t_{ox}}\right)dx \quad (6)$$

According to the tunneling front theory, defining $x_m(t)$ as the position at which the tunneling rate is maximum at time t, and assuming that traps between x_m and the interface are filled, while traps on the other side of x_m are empty, the integral solves analytically, and replacing

$$x_m(t) = \frac{1}{2K}\ \ln\left(\frac{t}{\tau_0}\right) \quad (7)$$

we obtain

$$\Delta V_C(t) = \frac{qN_t\Delta f_s}{C_{ox}}\left[\frac{1}{2K}\ \ln\left(\frac{t}{\tau_0}\right) - \frac{1}{8K^2 t_{ox}}\ \ln^2\left(\frac{t}{\tau_0}\right)\right] \quad (8)$$

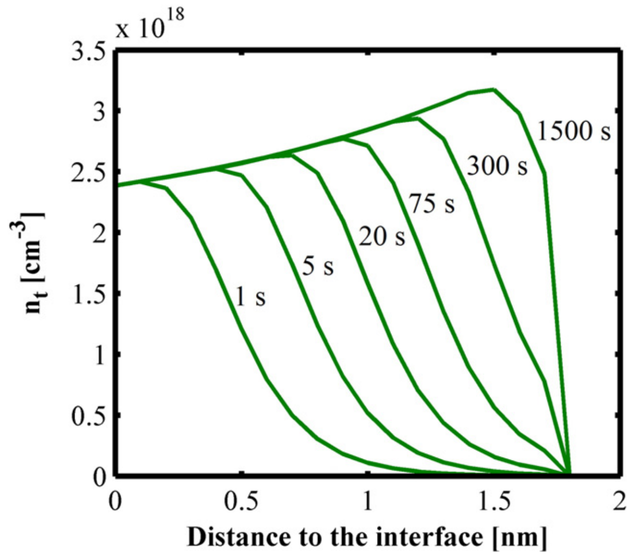

Fig. 7. Time evolution of the density of electrons trapped during the simulation of the charging dynamic.

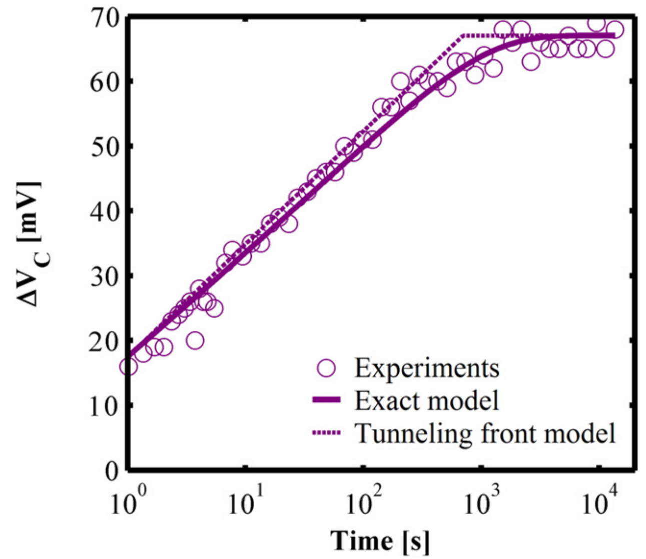

Fig. 8. Experimental ΔV_C vs. time charging curve fitted with the exact model presented in Section 3 and with a tunneling front model.

which is valid from $t = \tau_0$ until $t = \tau_f$, the time that the tunneling front takes to reach the distance x_f, when the dynamics saturate. As deduced from (8), when the traps are located close to the interface with the semiconductor in a thin area, the second term is negligible with respect to the first, and the expression can be simplified to

$$\Delta V_C(t) \cong \frac{qN_t\Delta f_s}{2KC_{ox}} \ln\left(\frac{t}{\tau_0}\right) \tag{9}$$

which predicts the observed log(t) behavior.

Eq. (9) is, therefore, a good resource to obtain first values for the physical parameters. From the experimental curves, three parameters can be obtained: The initial and final times, and the slope. However, four physical parameters must be determined: N_t, E_t, x_f, τ_0. We can identify τ_0 as the initial time. The slope is represented by the relation $N_t\Delta f_s/K$, which is proportional to the relation $N_t\Delta f_s/E_t^{1/2}$, due to (3). The final time t_f is represented by the factor Kx_f, or equivalently $E_t^{1/2}x_f$.

Out of the pre-exponential factor τ_0, which can be determined unambiguously, in order to obtain the other three physical parameters we need to fix one of them. Taking into account that the applied voltage during the experiment is relatively low, to maintain the density of traps lower than 10^{20} cm^{-3}, the trap energy level could be taken in the range $E_t = E_F \pm 4kT$, where E_F is the Fermi level in the semiconductor, thus $E_t = 1.63 \pm 0.1$ eV. This energy range includes the obtained trap energy level from the simulations in Section 3 ($E_t = 1.59$ eV).

Fig. 8 shows the experimental $\Delta V_C(t)$ curve from the charging process together the fitting by both the exact model and the tunneling front model. As shown, the tunneling front-based model also reproduces the experiment, except around t_f. From the fitting procedure, assuming $E_t = 1.63$ eV, the density and width of traps result in $N_t = 1.34 \times 10^{19}$ cm^{-3}, and $x_f = 1.61$ nm, respectively. Both values are very similar to the ones obtained from the exact model ($N_t = 1.36 \times 10^{19}$ cm^{-3} and $x_f = 1.7$ nm).

To validate this simplified model, we analyze in Fig. 9 the time evolution of the tunneling time constant and the occupation probability for a trap at 1 nm to the Si/HfO_2 interface during the simulation of a charging process, as shown in Fig. 6(a). Both parameters were assumed to be almost constant from the first hypothesis of the tunneling front model. Effectively, the change during all the time range was 0.18% and 4.8% for the tunneling time constant and the occupation probability, respectively, which are low enough to justify the tunneling front model.

4.2. The spatial distribution of electron traps

The extent of the trapping region in HfO_2 layers is controversial in the literature. While some works report electron trapping all over the dielectric [12,17,37–43]; in [37,38] a 3.2 nm HfO_2 layer was studied and the scanning distance was only 1.2 nm; and in [16,35] the trap density determined by modeling was approximately constant up to 1 nm (for 3 nm HfO_2 thickness) and 2.5 nm (for 4.5 nm HfO_2 thickness), from where it starts to decrease. These results are in some agreement (less than 1 nm of difference) with our 1.7 nm trapping region.

Besides, it is worthy noticing that our result is further supported by the following consideration: one of the parameters of the simplified model presented above is the product of the trapping region width times $E_t^{1/2}$, which represents the final time t_f. Thus, in order to consider that the traps are distributed all over the dielectric ($t_{ox} = 10.5$ nm), the trap energy level should be $E_t \approx 41$ meV. Under the voltages applied in our experiments, this shallow level corresponds, as pointed out in

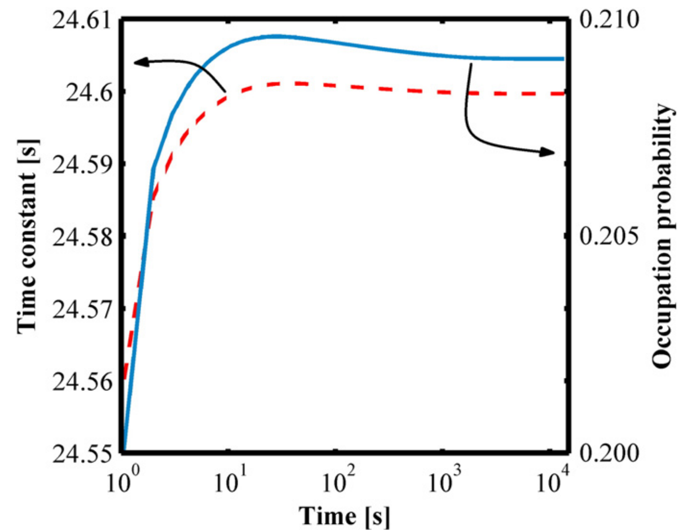

Fig. 9. Time evolution of the tunneling time constant and the occupation probability for a trap at 1 nm to the Si/HfO_2 interface during a simulation of a CCVT corresponding to the charging process shown in Fig. 6(a).

Section 4.1, to a negligible value for the steady-state occupation probability. Therefore, in this case, a meaningless giant value for the density of electron traps would be required to fit the actual amount of trapped charge responsible for the measured V_C-shifts.

Another possibility is the trapping region we obtained corresponds with the SiO_x IL. This was reported to be substoichiometric, which would lead to a higher density of electron traps compared to SiO_2 [44,45]. Considering the possible presence of an IL reported in HF cleaned samples as ours [46], the $E_t^{1/2}x_f$ product ($x_f = 0.3$ nm from [46]), yields a trap energy depth of 6.8 eV, higher than the reported ~6 eV HfO_2 band gap [30,47].

Recent results [48] were interpreted in terms of two types of traps: one type characterized by a thermal energy of 0.5 eV and located in the bulk of the HfO_2 layer, and the other with 0.34 eV of thermal energy and located close to the SiO_2/HfO_2 interface. Within this framework, the traps sensed in our work could be considered as part of the second group, but with a different energy level than that reported in [48].

4.3. The trap energy level

Regarding the energy distribution of the defects, most groups have reported shallow bulk electron traps with energy E_t of approximately 0.30–0.35 eV which are responsible for the fast trapping process, with characteristic times of the order of the μs [41,42,49]. As we had mentioned above, in our case tunneling transitions at this shallow energy level requires a density of available traps much higher than the maximum density with physical meaning.

Our measurement technique allows revealing only deeper traps, and, in fact, modeling our results yields an energy trap level of 1.59 eV. This value is close to 1.5 eV reported by Zhu et al. [50], consistent with the results in Vandelli et al. [51,52], where trap energy level was in the range $E_t = 1.4$–2.7 eV, and Wu et al. [37,38], where a trap energy band between 0.8 eV and 1.6 eV below the HfO_2 conduction band edge was considered. Wu et al. observed that trap density exponentially increases with the decreasing trap energy depth, in agreement with Zheng et al. [22], who reported that only a 10% of the traps are below Si conduction band edge.

A possible uncertainty about the trap energy level would appear because we considered only elastic transitions assisted by interface states neglecting any interaction with the substrate conduction band by multiphonon emission/absorption. It was reported that lattice relaxation multiphonon emission is involved in the electron trapping in HfO_2 samples [51,52]. Regarding this issue, considering the trap energy level is about 1.6 eV below the oxide conduction band, the question is about what is the energy level in the substrate involved in the trapping/detrapping processes. One possibility is to consider only elastic tunneling transitions, then interface states in the silicon bandgap supply the electrons to be trapped. In this case we followed the hypothesis that for the long times involved in our measurements the interface states reach equilibrium in a time much lower than the lowest trapping time constant of a bulk trap, then we considered interface states simply as a charge reservoir. The other possibility is that the traps communicate directly with the substrate conduction band. In this case the nonradiative multiphonon theory [51] predicts that an electron can be injected at an energy higher than the energy level of the trap. To decide between the two possibilities we appealed to the geometrical factor proposed by Veksler et al. [53] to compare the interface states contribution to the voltage instability with the contribution of conduction band states. For typical interface states densities of 10^{11} to 10^{12} cm^{-2} eV^{-1}, he obtained a geometrical factor value of 10^{-3} to 10^{-4}. In our case, for the applied bias during the charging process (circles in Fig. 5), the Fermi–Dirac occupation probability of electrons in the conduction band edge is as low as 10^{-7}. Taking into account the Veksler approach, tunneling from/to interface states appears as the dominant mechanism. Additionally, multiphonon theory gives a detrapping time constant to trapping time constant ratio of $exp(n\hbar\omega/kT)$, where $\hbar\omega$ is the single phonon energy and n is the number of phonons involved in the electron detrapping [51]. Considering only transitions with the conduction band edge, and taken into account the 1.6 eV value obtained from our simulations for the trap energy level and the Si/HfO_2 conduction band offset $\Phi_C = 1.4$ eV, the detrapping time constant would be three orders of magnitude higher than the trapping one. This result is also in contradiction with our τ_0 values for both trapping and detrapping processes, which are of the same order of magnitude. Thus, for the very low applied bias conditions of our experiments, the interface states seem to be the source of tunneling electrons. Besides, the detrapping time constant to trapping time constant ratio of 7 obtained by simulations gives an energy difference of ~50 meV. This would be an estimation of the uncertainty in energy in our model because it neglects relaxation after trapping.

Some works reported that oxygen vacancies would be the defects responsible for electron trapping in HfO_2 layers [42,49,54–56]. From theoretical calculation [57], the V^{2+} state has a trap energy depth of 0.3 eV, consistent with the reported shallower traps, while the energy levels for V^+ and V^0 states are 1.3 and 1.6 eV, respectively. The obtained trap energy of 1.59 eV is thus consistent with transitions involving the V^+/V^0 states.

5. Summary and conclusions

In this paper, the electron trapping and detrapping at deep energy levels in n-type MOS capacitors with HfO_2 as insulating layer were studied. The hysteresis phenomenon in the capacitance–voltage (C–V) characteristic and its dependence with the applied voltage and the number of C–V cycles was characterized. The time dependence of the trapping/detrapping processes was studied through a constant capacitance voltage transient technique. This technique allows sensing deep traps and prevents the generation of new traps inside the dielectric.

A physical model based on tunneling transitions between electronic states in the substrate and the electron traps inside the dielectric was presented in order to reproduce the V_C-shift observed during charging and discharging processes. Fitting the experimental results with the proposed model yields an electron trap density of $N_t = 1.36 \times 10^{19}$ cm^{-3} located in the first 1.7 nm close to the Si/HfO_2 interface at an energy level $E_t = 1.59$ eV below the HfO_2 conduction band edge.

The presence of deep traps confirmed in this work should be complemented with the results of other techniques in order to get a wider description of the energy distribution of the traps in the dielectric gap.

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