Repetitive Control With Adaptive Sampling Frequency for Wind Power Generation Systems

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***Abstract*— This paper presents a novel repetitive control (RC) for wind power generation systems (WPGS), which achieves optimal performance in steady-state conditions due to a variable sampling/switching period technique (VSPT). The main objective of VSPT is to obtain an integer number of samples per grid period, which solves the main problem of RC, i.e., the loss of rejection to periodic disturbances due to grid frequency drift. The sampling/switching frequency is adjusted with a variable sampling period filter phase-locked loop, which also adds robustness to the system due to its inherent tolerance to grid voltage distortion and unbalances, and events such as frequency steps and faults. The control and synchronism subsystems are described, designed, and verified experimentally in a 10-kW WPGS. The results obtained prove the accuracy of the proposed control even under severe disturbances, typical in grids with high WPGS penetration, providing ancillary functions to enhance reliability and reduce operational costs.**

***Index Terms*— Grid-tie current-controlled three-phase inverters, power quality, repetitive control (RC), wind energy, wind power generation systems (WPGS).**

I. Introduction

WIND power generation systems (WPGS) play a key role in the distributed power generation scenario worldwide [1]. Modern variable-speed WPGS are connected to the grid through a current-controlled three-phase voltage-source inverter (CC-VSI) [2], [3], as shown in Fig. 1. Phase currents injected to the grid must comply with strict power quality standards, such as [4], which demand a total harmonic distortion (THD) of the injected currents below 5%. Given the increasing penetration of WPGS, even more strict limits are expected to be needed in the near future. Moreover, new grid codes are requiring additional features. Known as ancillary functions, they enhance robustness, safety, and reliability of the grid through reactive power injection, fault ride-through capabilities, compensation of harmonic currents generated by nearby nonlinear loads, and mitigation of asymmetrical loads, among others [5]–[7].

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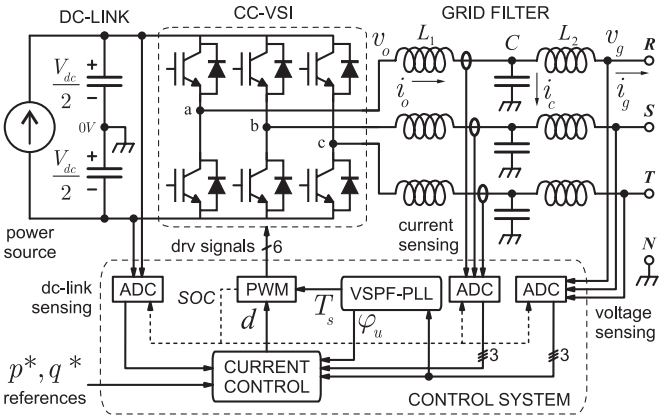

Fig. 1. Block diagram of the proposed control system within a CC-VSI for WPGS application. The power source represents the energy supplied by the wind generator.

A key part of a WPGS is the CC-VSI current control and synchronism subsystems, which are entirely responsible for meeting all the aforementioned requirements. This is a complex task considering the multiple disturbance sources affecting the system. In addition to grid voltage fluctuations, unbalances and harmonics, inverter nonlinearities (e.g., dead times, voltage drops of semiconductor switches, inductance variations, etc.) are major causes of current distortion. In particular, when employing IGBTs oversized to improve the reliability of the WPGS and running at high switching frequency to reduce the size and cost of reactive components, disturbances induced by dead times become high in magnitude and rich in harmonic content, so low THD currents are difficult to obtain [8].

Classic control strategies for WPGS are proportional-integral (PI) [9]–[11] and proportional-resonant (PR) control [12]–[14]. PI control is the defacto strategy due to its low computational cost and simplicity, and is typically implemented in the synchronous reference frame (SRF). This control adds a resonant pole in the open-loop transfer function at the grid fundamental frequency, f_g, ensuring zero steady-state error at such frequency; grid phase/frequency information is implicit in the *abc-dq* transformation. However, inverter nonlinearities and unbalanced/distorted grid voltages generate errors not only at fundamental, but also at harmonic frequencies of the grid. The limited open-loop bandwidth obtained with PI controllers results in low disturbance rejection capability and, hence, distorted line currents. On the other hand, PR control,

which is typically implemented in the stationary reference frame, performs better since it places poles at fundamental and selected harmonic frequencies. Nonetheless, a dedicated resonant regulator is required for each selected frequency. This increases significantly control complexity and computational cost when disturbances with high harmonic content are present. Moreover, the resonant regulator coefficients depend on f_g, and hence they must be updated on line to keep the resonant poles exactly on the desired frequencies; otherwise, excessive current distortion may appear even with small f_g drifts.

An alternative method is to enhance the steady-state performance of a classic current controller (proportional (P), dead-beat predictive (DBP), state feedback (SFB), etc.) by attaching a repetitive controller. Repetitive control (RC), which is based on the internal model principle [15], [16], has been employed in uninterrupted power supplies [17], [18], active power filters [19]–[21], power factor correction converters [22]–[24], and the output active/reactive power of distributed power generation systems [7], [25]–[28]. In the plug-in scheme, the classic controller closes an inner loop providing fast response to grid disturbances and reference changes, while the RC ensures zero steady-state error by placing resonant poles at fundamental and every harmonic frequency of the grid up to the Nyquist frequency. A key feature of RC is its simple and computationally efficient algorithm, which enables perfect tracking/rejection of signals with very high harmonic content. In addition, RC can be designed in any reference frame (abc, $\alpha\beta$, dq) without modifying its structure. However, as with PI and PR control, RC is susceptible to grid frequency variations [20], [29]. If the sampling/switching frequency, f_s, is not an integer multiple of f_g, the RC poles no longer lie on the desired locations, and high current distortion may appear even with small frequency changes. This problem was addressed in [26]–[28] by adding considerably complexity to the RC structure, increasing the computational cost, and losing the main benefit of RC over other proposals.

This paper proposes an alternative solution, which consists in changing f_s adaptively so $f_s = Nf_g$, where N is a fixed integer number. This is achieved by a variable sampling/switching period technique (VSPT), while retaining the simple structure of the original RC with a fixed number of samples per grid period. VSPT is implemented with a variable sampling period filter phase-locked loop (VSPF-PLL) presented in [30], which also provides system immunity against grid voltage unbalances, distortion, and faults.

The presentation is organized as follows. Section II reviews the current control and the VSPF-PLL. Section III develops a control system model for stability and dynamic analysis. System design is dealt with in Section IV. Section V verifies experimentally the proposed method with a 10-kW WPGS. Some simulations are also presented to complement the experimental results. Finally, Section VI concludes this paper.

II. Control Structure and Principles

The WPGS control system can be observed in Fig. 1, where the VSPF-PLL output governs the sampling/switching period

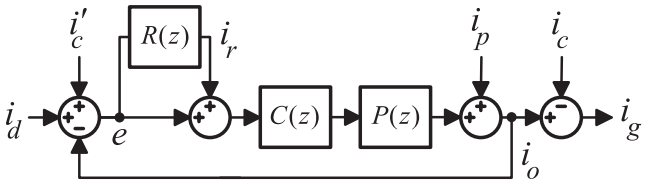

Fig. 2. Block diagram of the control system.

value, $T_s = 1/f_s$, which feeds the pulsewidth modulator (PWM). This in turn generates the start-of-conversion signal for the analog-to-digital converters (ADCs). Thus, the whole system operates with a frequency f_s that is an exact multiple of f_g, $f_s = Nf_g$. During normal operation, grid frequency drifts are small (e.g., $\leq 2\%$), so f_s keeps close to its nominal value. As a consequence, the variation over time in the spectral content due to f_s is negligible, hence switching losses are approximately the same and the grid filter design can be left unchanged.

A. Current Control

A block diagram of the control structure adopted is shown in Fig. 2. Due to the VSPT, the sampling time T_s follows the grid period T_g, which changes slowly. This small and slow drift allows to treat the variable-time discrete system of Fig. 2 as a fixed-time one with negligible error [29]. A further discussion and stability analysis due to the variable sampling frequency is performed in Section IV-E. $P(z)$ is the plant transfer function comprised by the modulator, the inverter, the LCL filter, and the grid. Signal i_g is the current injected into the grid, i_o is the inverter output current, and i_c is the capacitor current. Notice from Fig. 1 that $i_g = i_o - i_c$. In Fig. 2, i_d is the reference (desired) current. Since only i_o is measured, i_g will only follow i_d if i_c is effectively compensated by the feedforward term i_c', which is added to i_d. The exogenous signal i_p represents the multiple disturbances affecting the output current: grid voltages not completely canceled by feedforward techniques [31], and inverter nonlinearities such as dead times [8], among others. Spectral components of i_p are assumed to be at fundamental and harmonic multiples of the grid frequency. $C(z)$ is a current regulator closing an inner loop to provide fast response to transients, typically within a few milliseconds. Classic control strategies, such as proportional, DBP or SFB controllers are typically employed. From Fig. 2, the resulting inner closed-loop transfer function is

$$H(z) = \frac{I_o(z)}{I_d(z)} = \frac{C(z)P(z)}{1 + C(z)P(z)}. \tag{1}$$

A plug-in repetitive controller $R(z)$ can be attached to $C(z)$ in a cascaded structure, as in Fig. 2, to improve the control loop disturbance rejection. According to the internal model principle [32], $R(z)$ must add poles to the open-loop transfer function at dc ($z = 1$), fundamental, and harmonic frequencies of the grid to ensure that i_p is completely rejected in steady state.

Remark 1: For stability reasons, it is convenient that $C(z)$ does not contain poles at dc ($z = 1$), fundamental, and

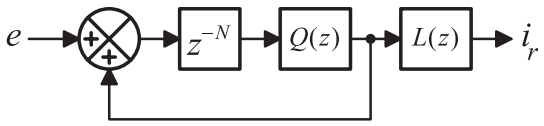

Fig. 3. Block diagram of the proposed repetitive controller in a plug-in structure.

harmonic frequencies of the grid. This is because $R(z)$ already adds poles in such locations. Classic controllers such as P, DBP, and SFB do not typically add such poles.

Remark 2: Design of $C(z)$ is easier when using a plug-in RC, since now $R(z)$ is responsible for rejecting disturbances and, hence, the inner loop bandwidth does not need to be maximized.

Following the internal model principle, the minimum expression synthesizing the required RC poles is:

$$R(z) = \frac{z^{-N}}{1 - z^{-N}} \tag{2}$$

where N is a fixed integer calculated as $N = T_g/T_s$ using nominal values for T_g and T_s. The algorithm in (2) is straightforward to implement in a digital signal processor (DSP) and implies low computational cost due to its reduced amount of operations. Nevertheless, the simple form (2) leads to instabilities due to the open-loop phase shift caused by $P(z)$ above the crossover frequency of $H(z)$. Stability is improved by adding two blocks into the RC structure, $Q(z)$ and $L(z)$, as shown in Fig. 3. The resulting transfer function is

$$R(z) = L(z)\frac{z^{-N}Q(z)}{1 - z^{-N}Q(z)}. \tag{3}$$

Both $Q(z)$ and $L(z)$ have different effects on control dynamics. At medium to high frequencies (typically above the inner-loop crossover frequency), $L(z)$ compensates system phase shifts, improving stability without affecting rejection capability. However, at very high frequencies (close to Nyquist frequency $f_s/2$), phase shifts are too large to be compensated by $L(z)$. This is solved with $Q(z)$ but at the expense of reducing rejection at such frequencies, which is a reasonable tradeoff considering that disturbances have usually very small amplitude in that part of the spectrum. $L(z)$ is typically implemented as a phase-lead compensator, while designing $Q(z)$ as an FIR filter of three to 10 taps usually yields good results [32]. A detailed design of $Q(z)$ and $L(z)$ is presented in Section IV.

The tracking error transfer functions with and without the RC reveal some interesting properties of this system. From Fig. 2, the tracking error without the RC is

$$B(z) = Z\{b(kT_s)\} = \frac{I_d(z) - I_p(z)}{1 + C(z)P(z)} \tag{4}$$

and after attaching the RC the error becomes

$$E(z) = Z\{e(kT_s)\} = B(z)\frac{1 - Q(z)z^{-N}}{1 - \alpha(z)z^{-N}} \tag{5}$$

where

$$\alpha(z) = [1 - L(z)H(z)]\,Q(z). \tag{6}$$

If $L(z)$ is chosen so $L(z)H(z) = 1$, then according to (6), all the poles in the denominator of (5) are located at $z = 0$. In addition, $Q(z) \approx 1$ (except at very high frequencies), which simplifies (5) to

$$E(z) = B(z)\left[1 - z^{-N}\right]. \tag{7}$$

Notice from (7) that:

1) during the first grid period after a transient, the error is $e(kT_s) = b(kT_s)$; a properly designed $C(z)$ reduces the inner-loop error $b(kT_s)$ and hence the transient error;
2) the RC places N transmission zeros (infinite attenuation) on the unit circle at multiples of the grid frequency ensuring zero tracking error in steady state;
3) the error signal goes to zero after the first grid cycle; however, it may take more grid cycles to converge when $L(z)H(z) \neq 1$.

B. Comparison With Other RC Approaches

An important drawback of RC is its gain loss when the grid frequency varies, which, in turn, reduces the control loop disturbance rejection and reference tracking capability [20]. This occurs because the order N of the RC is not equal to the ratio T_g/T_s, and hence the RC poles no longer lie at multiples of f_g. Several approaches have been proposed in the literature to deal with this issue, the most common being the introduction of a fictitious sampler operator [26]. A recent and more sophisticated approach uses an FIR filter with variable coefficients within the RC algorithm to emulate the fractional delay produced by the frequency drift [27]. A similar approach is found in [28], which employs a simple first-order low-pass filter, cascaded with the RC delay line, with adjustable cutout frequency. This is much simpler than the FIR filter in [27], hence the computational cost is reduced at the expense of a degraded performance. In both cases, the filter coefficients must be accurately updated online to avoid additional loss of performance; the proposed RC does not require any parameter update. In addition, both [27] and [28] suffer from coefficient quantization errors. In the proposed strategy, the VSPT allows the use of the simple RC algorithm (3) consisting of a delay and simple filters in $Q(z)$ and $L(z)$ (which are presented in detail in Section IV), where the aforementioned numerical errors are nonexistent since all the coefficients are one or powers of two.

Fig. 4 shows the gain of several RC algorithms, operating with fixed $T_s = 100\,\mu$s and for a grid frequency of 49.38 Hz, a 1% variation from the nominal value of 50 Hz. The static RC, described by (2) and using a fixed order $N = 200$, exhibits the worst performance under grid frequency changes. The adaptive RC reduces the gain loss by setting online the order N to the nearest integer of the estimated signal period. The adaptive RC with linear interpolation further reduces the gain loss, for which a precise estimation of the grid frequency is required to update the algorithm coefficients. In all the cases described, notice the significant reduction in the RC gain, which may lead to high distortion in the output currents. For high-order harmonics, the RC could even amplify disturbances (negative gain in decibels), which is the case for the static RC in Fig. 4.

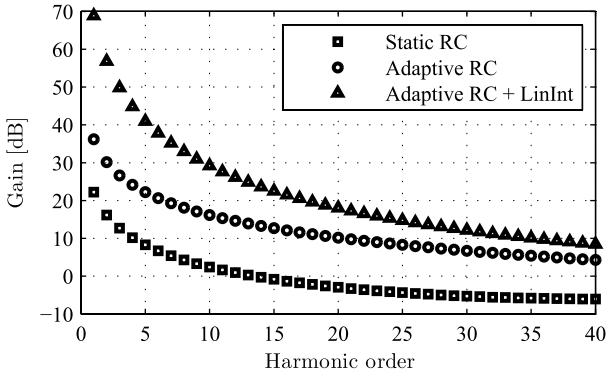

Fig. 4. Gain of several RC approaches for $f_g = 49.38$ Hz.

The solution proposed here uses a fixed integer value for N, while T_s is adaptively adjusted to ensure $N = T_g/T_s$ by the VSPF-PLL proposed in [30] and briefly reviewed in the following. This allows to use the simple structure of the static RC, without parameter adaptation and low computational cost, but with infinity gain at all the multiples of f_g.

C. Variable Sampling Period Filter Phase-Locked Loop

The three-phase VSPF-PLL [30] operates with a variable sampling period technique. As shown in Fig. 1, the PLL receives the sampled three-phase voltages, which are transformed to the SRF, and the q component is used as an estimate of the phase error. A sliding-window filter (SWF) is applied to reject signals different from the fundamental positive sequence. This feature provides robustness to the VSPF-PLL against grid voltage distortions, unbalances, and faults. After the SWF, a lead-lag compensator with integral action is used to obtain a stable closed loop with zero steady-state error. The output of this compensator is the value of T_s, which is updated in the PWM for the next period. A reference phase, φ_u, is internally generated by adding a phase step equal to $2\pi/N$ on each new sampling period. φ_u is employed to transform the sampled voltage to the SRF, so the loop will increase or reduce T_s to match φ_u to the actual positive sequence phase. φ_u is also sent to the control block to generate the current reference signals. The VSPF-PLL mathematical model, together with the design of the lead-lag compensator and the SWF, is described in detail in [30].

The VSPF-PLL distinctive component is the SWF, whose transfer function is

$$G_{\mathrm{SWF}}(z) = \frac{1 - z^{-N_{\mathrm{SWF}}}}{1 - z^{-1}} \tag{8}$$

which shares some properties with the RC, clearly visible by comparing it with (2). While (2) places N poles equally spaced along the unitary circle, (8) places N_{SWF} zeros in the same places. Parameter N_{SWF} is chosen as N or $N/2$ whether even harmonic components are significant or not in the grid voltages. If they are not, $N_{\mathrm{SWF}} = N/2$ can be used, reducing memory positions by half. Notice that the zero in $z = 1$ is canceled by a pole in such place, allowing to pass only the dc component of the estimated phase error, which is the positive sequence phase error. As deduced from (8), the SWF converges in one grid cycle if $N_{\mathrm{SWF}} = N$, and in half cycle if $N_{\mathrm{SWF}} = N/2$. In addition, both (8) and (2) require that $f_s = Nf_g$ to operate without error in steady state. As in (2), (8) bears low computational cost if compared with adding the required zeros with other methods (e.g., PR filters). Finally, in both (8) and (2), all the coefficients are unitary, eliminating coefficient roundoff errors and reducing memory requirements.

III. Dynamic Model for Stability Analysis

This section develops a new discrete-time system model, sampled at frequency f_g, derived from the original model sampled at f_s. The new model enables a straightforward analysis of system stability and dynamics. First, it is assumed that f_s has been stabilized and thus a fixed ratio $N = T_g/T_s$ has been achieved. The tracking error signals with and without the RC are $e(kT_s)$ and $b(kT_s)$, as defined in (5) and (4), respectively. If time is split in slots of duration T_g, these signals can be expressed as

$$\begin{aligned} b(kT_s) &= \sum_{i=-\infty}^{\infty} b_i(kT_s) \\ e(kT_s) &= \sum_{i=-\infty}^{\infty} e_i(kT_s) \end{aligned} \tag{9}$$

where $b_i(kT_s)$ and $e_i(kT_s)$ are defined for each respective ith time slot, $iN \le k < (i+1)N$. If $B_i(z) = Z_k\{b_i(kT_s)\}$ and $E_i(z) = Z_k\{e_i(kT_s)\}$, where $Z_k\{\cdot\}$ is the operator Z-transform of the argument in the variable k, then

$$\begin{aligned} B(z) &= \sum_{i=-\infty}^{\infty} B_i(z) \\ E(z) &= \sum_{i=-\infty}^{\infty} E_i(z). \end{aligned} \tag{10}$$

Replacing (10) in (5) yields

$$\begin{aligned} &\left(\sum_{i=-\infty}^{\infty} E_i(z)\right) + \alpha(z)\left(\sum_{i=-\infty}^{\infty} E_i(z)\right) z^{-N} \\ &\quad = \left(\sum_{i=-\infty}^{\infty} B_i(z)\right) - Q(z)\left(\sum_{i=-\infty}^{\infty} B_i(z)\right) z^{-N}. \end{aligned} \tag{11}$$

Notice that

$$\left(\sum_i E_i(z)\right) z^{-N} = \sum_i E_{i-1}(z)$$

and

$$\left(\sum_i B_i(z)\right) z^{-N} = \sum_i B_{i-1}(z)$$

so (11) can be rewritten as

$$\begin{aligned} &\sum_{i=-\infty}^{\infty} E_i(z) + \alpha(z) E_{i-1}(z) \\ &\qquad = \sum_{i=-\infty}^{\infty} B_i(z) - Q(z) B_{i-1}(z) \end{aligned} \tag{12}$$

which not necessarily implies the arguments of the sums on both sides are equal. However, notice that $E_i(z)$ must depend only on $E_{i-1}(z)$, $B_i(z)$, and $B_{i-1}(z)$, since the system memory can store values of up to one grid cycle before. Hence, the arguments on both sides in (12) must be equal

$$E_i(z) + \alpha(z)E_{i-1}(z) = B_i(z) - Q(z)B_{i-1}(z). \quad (13)$$

This is a difference equation in the discrete variable i with sampling time T_g, where z is only a complex parameter. Setting $z = e^{j\omega}$, the model is analyzed for each frequency $0 \leq \omega < \pi$. To simplify notation, $E_i(z = e^{j\omega})$ is written as $E_i(\omega)$, and the same applies to any other function of z: $\alpha(\omega)$, $B_i(\omega)$, $Q(\omega)$, and so on. Then, (13) becomes

$$E_i(\omega) + \alpha(\omega)E_{i-1}(\omega) = B_i(\omega) - Q(\omega)B_{i-1}(\omega). \quad (14)$$

When specifying a value for ω, $\alpha(\omega)$ and $Q(\omega)$ become coefficients with complex values, and $E_i(\omega)$ and $B_i(\omega)$ are functions only of the variable i. Then, the Z-transform in the variable i, $Z_i\{\cdot\}$, can be applied to (14), yielding

$$\frac{\xi(\lambda)}{\beta(\lambda)} = \frac{1 - Q(\omega)\lambda^{-1}}{1 - \alpha(\omega)\lambda^{-1}} \quad (15)$$

where λ is the variable in the new transformed domain, $\xi(\lambda) = Z_i\{E_i(\omega)\}$, and $\beta(\lambda) = Z_i\{B_i(\omega)\}$. Notice that $E_i(\omega)$ gives the frequency content of the error signal in the ith grid cycle. Hence, (15) represents infinite transfer functions, one for each value of ω, describing how the error for that particular frequency evolves through successive grid periods. The dynamic behavior of the system can be fully analyzed by considering all these infinite transfer functions for $0 \leq \omega < \pi$.

Transfer function (15) contains a single zero in $Q(\omega)$ and a single pole in $\alpha(\omega)$. In general, $\alpha(\omega)$ is complex but only its magnitude is meaningful to determine stability and convergence speed. Stability is guaranteed if $\alpha(\omega)$ lies within the unit circle of the λ-plane for each frequency ω, that is

$$|\alpha(\omega)| < 1, \ 0 \leq \omega < \pi \quad (16)$$

which means that the error will be smaller than in the previous grid cycle, converging to zero asymptotically. If $\alpha(\omega) = 0$ for some ω, then the error converges to zero in a single grid period (dead-beat behavior) for that particular frequency. This condition, which represents an optimum behavior in terms of convergency, is hard to achieve in practice for a wideband range of ω. However, it is desirable to keep $|\alpha(\omega)|$ as small as possible for two reasons: 1) to obtain a fast convergence speed and 2) to be far away from the stability limit $|\alpha(\omega)| = 1$. According to (6), this can be done with $|Q(\omega)| \approx 0$ or $L(\omega)H(\omega) \approx 1$. The former directly affects the rejection capability of the loop to harmonic disturbances: RC is not effective for any ω at which $Q(\omega) = 0$. Instead, rejection capability is less sensitive to the form of $L(z)$. However, obtaining $L(z) = H(z)^{-1}$ is not always possible due to uncertainties in the plant, specially at high frequencies; notice that when $|L(\omega)H(\omega)| \approx 1$ and $\phi(L(\omega)H(\omega)) \approx 180°$ then $|\alpha(\omega)| \approx 2$, and the loop becomes unstable, so phase shifts must be carefully considered. A corollary of the aforementioned conclusions is that $Q(z)$ should be designed to be zero only at high frequencies, in which very high rejection is not necessary, while $L(z)$ tries to match the inverse of the internal loop transfer function from low to mid frequencies.

TABLE I
SYSTEM PARAMETERS

Nominal output power	10 kW
Grid phase voltage L-L (rms)	380 V
Nominal output current (rms)	15.2 A
DC-link voltage, V_{dc}	850 V
Grid frequency, f_g	50 Hz ($\pm 2\%$)
Frequency ratio, $N = f_s/f_g$	200
Switching frequency, f_s	10 kHz ($\pm 2\%$)
Grid filter parameters	$L_1 = 2$ mH, $L_2 = 0.5$ mH, $C = 15\,\mu$F, $R_C = 1.5\,\Omega$
Equivalent series filter, L_s-R_s	$L_s = 2$ mH, $R_s = 1.0\,\Omega$

IV. CONTROL SYSTEM DESIGN

The control and synchronism subsystems are designed taken an example case of a WPGS whose main parameters are listed in Table I, which correspond to the experimental prototype employed in Section V. To control each phase independently to allow the injection of asymmetrical currents, the VSI has the neutral point of the load connected to the dc link, as shown in Fig. 1. As a consequence, the inverter driving signals are generated by three independent PWM modulators, and the control is preferably developed in the natural reference frame (abc coordinates). Nevertheless, it is worth mentioning that the proposed control and methodology are valid for any reference frame (abc, $\alpha\beta$, and dq), as pointed out in Section I.

A. Inner Loop Design

The first step in designing the control system is to obtain a model for $P(z)$ and to close a stable and fast internal loop with $C(z)$. A discrete-time model for the plant, considering the modulator reference duty cycle $D(z)$ and current $I_o(z)$ as the input and output variables, is presented in [31]

$$P(z) = \frac{I_o(z)}{D(z)} = \frac{V_{dc}}{2}\frac{T_s}{L_s}\frac{(1-\delta)z + \delta}{z - e^{-R_s T_s/L_s}}z^{-2} \quad (17)$$

where the integer delay z^{-2} is due to the PWM and the digital implementation of the controller, while δ is a fractional delay due to the acquisition/filtering of the output current ($0 \leq \delta < 1$) plus computational delays. For this paper case, it is assumed that $\delta = 0.7$, in accordance with the antialiasing analog and digital filters employed. In (17), the LCL filter dynamics (parameters L_1, C, and L_2) is simplified with an equivalent series model (parameters L_s and R_s). This approximation yields good results when the filter capacitor C is small enough, as in this case.

The inner loop is closed with a proportional controller

$$C(z) = K_p / V_{dc,m} \quad (18)$$

which features minimal computational cost and offers an acceptable transient response. The measured dc link voltage, $V_{dc,m}$, is updated on line so it cancels off with the actual

V_{dc} value in (17). This ensures that dc-link fluctuations will not affect loop dynamics. Proportional gain K_p is adjusted considering parameter variations, which are assumed to be $+25/-50\%$ for L_s and $\pm 30\%$ for R_s. Considering the worst case ($L_s - 50\%$, $R_s - 30\%$), a stable closed-loop with a minimum phase margin of $PM \approx 30°$ is obtained with $K_p = 4$.

B. RC Design

Section III showed that optimum results are achieved if the inner loop dynamics is completely canceled, which is achieved with $L(z) = 1/H(z)$. Nonetheless, due to plant uncertainties and parameter variations, achieving this task is not trivial. Another, more practical approach is to only compensate phase shifts in the frequency regions where stability is compromised. Notice that $H(\omega) \approx 1$ for frequencies below the inner loop crossover frequency, so adopting $L(\omega) = 1$ leads to $\alpha(\omega) \approx 0$. Above the crossover frequency, the magnitude of $H(\omega)$ decreases and its phase rotates negatively, so the factor $1 - L(\omega)H(\omega)$ in (6) may be > 1 (unstable system). To compensate this phase shift, the following linear phase-lead compensator is employed [32]:

$$L(z) = K_r z^m \tag{19}$$

where K_r is the so-called repetitive gain and m is an integer, being usually $0 < K_r < 2$ and $m \ll N$ [33]. Here, it is set as

$$K_r = \frac{1}{|H(z=0)|} \tag{20}$$

to compensate the dc-gain loss of the inner loop. Nominal plant parameters and $K_p = 4$ yield $|H(z=0)| \approx 0.67$ and hence $K_r = 1.5$.

Regarding $Q(z)$, the following first-order moving-average low-pass filter is adopted [32]:

$$Q(z) = \frac{1}{4}z^{-1} + \frac{1}{2} + \frac{1}{4}z. \tag{21}$$

This simple FIR filter adds a zero phase shift to the delay block z^{-N} in the RC, which otherwise would degrade its performance, and provides proper attenuation at the highest frequencies.

An optimum value of m is obtained with the aid of Fig. 5, which plots $|\alpha(\omega)|$ for several values of m in (19). Fig. 5(a) is for $Q(z) = 1$, and it can be observed that for any m, $|\alpha(\omega)| > 1$ (or very close to one) in the high-frequency range, so the system is always unstable. The curves in Fig. 5(b) were obtained for $Q(z)$ as in (21), and show that the system is stable for $m > 2$. Notice how the curve peak lowers with successive increments of m until $m = 4$, after which peaks start to rise. Hence, the optimum value for this system is $m = 4$.

Fig. 6 plots step responses for the error $e(kT_s)$ to illustrate the effect that the selected Q and L filters have on the system stability. Fig. 6(a) shows the case for $Q(z) = L(z) = 1$, showing that the system is unstable, as shown by Fig. 5. Fig. 6(b) shows the case for the selected filters (19) and (21), showing a stable system. The error converges to zero in the second grid cycle for the low-frequency components (deadbeat behavior). However, it takes several grid cycles for the high-frequency components, resulting in the sharp and short pulses observed during the first three cycles.

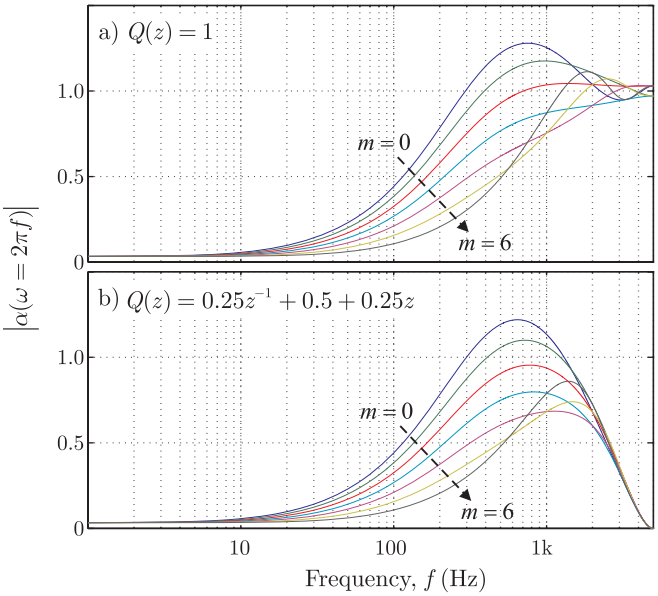

Fig. 5. Plots of $|\alpha(\omega)|$ for $m = 0, 1, \ldots, 6$ with (a) $Q(z) = 1$ and (b) $Q(z) = 0.25z^{-1} + 0.5 + 0.25z$.

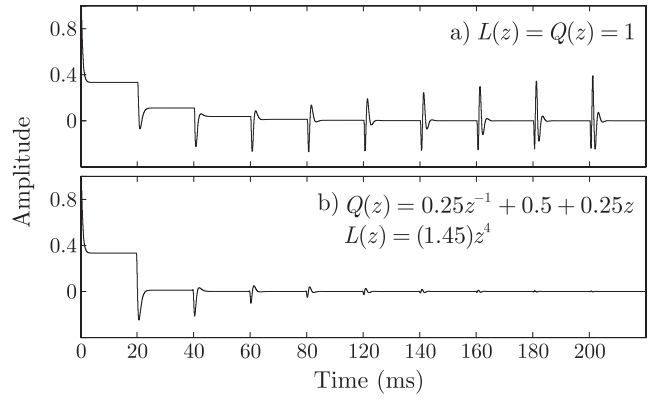

Fig. 6. Unitary-step response of the system error showing stability improvement by proper choice of filters Q and L.

Finally, notice that both Q and L have noncausal operators. However, they can be combined with the delay block z^{-N} to obtain an implementable difference equation. Replacing (19) and (21) in (3) results in

$$R(z) = \frac{(1.5)z^{-N+m+1}(0.25z^{-2} + 0.5z^{-1} + 0.25)}{1 - z^{-N+1}(0.25z^{-2} + 0.5z^{-1} + 0.25)} \tag{22}$$

which is causal. Notice that (22) can be implemented with a few simple operations, making it suitable for low-cost digital platforms. In addition, since the coefficients in (21) are powers of two, $Q(z)$ can be implemented with binary shift operations without coefficient roundoff errors.

C. PLL Design

The VSPF-PLL mathematical model and design method are presented in [30]. The proposed compensator used to close the PLL in the cited work has two zeros, a pole in $z = 1$ and

a gain for stability purposes. In addition, this transfer function favors the settling time at an expense of fast fluctuations in the sampling period during transients. However, to provide an adequate performance for the RC, the following simpler transfer function is adopted:

$$G_C(z) = K\frac{(z-a)}{(z-1)} \tag{23}$$

which results in a smooth dynamic response under grid events. Following the design method from [30], the zero location and gain in (23) are tuned to $a = 0.9968$ (5.1 Hz) and $K = 2.154 \times 10^{-7}$ (-133 dB), respectively. Thereby, a phase margin of 45° and an open-loop crossover frequency of 11.5 Hz are obtained.

D. Capacitor Current Feedforward Cancelation

As shown in Figs. 1 and 2, the injected current i_g will follow i_d only if the feedforward term effectively compensates the capacitor current i_c. This is mainly imposed by the grid voltage, i.e., $i_c \approx C dv_g/dt$. Hence, grid voltage harmonics will produce harmonic currents through C, increasing i_g distortion. The feedforward compensation term is calculated as

$$i_c'(k) = \frac{C}{T_s}\left(v_g(k) - v_g(k-1)\right) \tag{24}$$

which is an approximation that yields good results when the grid-side impedance is small enough, as in the case of this paper.

E. Stability Analysis Under Variable Sampling Frequency

Rather than employing the robust control approach proposed in [29] for stability analysis under variable sampling frequency, a more straightforward and easier-to-apply method is presented in the following. Grid frequency variations over time may occur within several seconds at worst [34], while the RC response in closed loop is within a few grid cycles. Hence, the whole system can be treated as a quasi-static one, as in [30], meaning that the dynamic models (18), (17), and (22) remain the same, with T_s acting only as a slowly varying parameter. It can be observed that T_s is only present in the plant model $P(z)$ in (17), where the factor T_s/L_s affects both its gain and the pole location at $z = e^{-R_s T_s/L_s}$. Fig. 7 shows a set of plots for $|\alpha(\omega)|$ (as in Fig. 5 but with $m = 4$), for different values of $(T_s/L_s)_{\text{norm}}$ (normalized to nominal value), defined as the ratio between a specified T_s/L_s and the nominal $(T_s/L_s)_{\text{nom}} = 0.05$ s/H (according to Table I). Plots in Fig. 7(a) are for $(T_s/L_s)_{\text{norm}} \leq 1$, where it can be noticed that the system is always stable. Yet, a severe worsening in the dynamic response for values of 1/3 and lower can be observed. Plots in Fig. 7(b) are for $(T_s/L_s)_{\text{norm}} \geq 1$, and show that the system becomes unstable for $(T_s/L_s)_{\text{norm}} \geq 4$. To find the worst case value for T_s leading to instability, the minimum L_s value is considered, which is assumed to be 50% from nominal (as stated in Section IV-A). Then, the critical period and frequency are $T_s = 200\,\mu$S and $f_s = 5$ kHz, respectively. With this and the fact that f_s and f_g are proportional, it is concluded that the grid frequency limit to ensure stability is 25 Hz, 50% lower than the nominal frequency. This is far beyond normal frequency limits (e.g., the ±6% limit requested by [34] for fault ride-through capability), and thus stability is guaranteed.

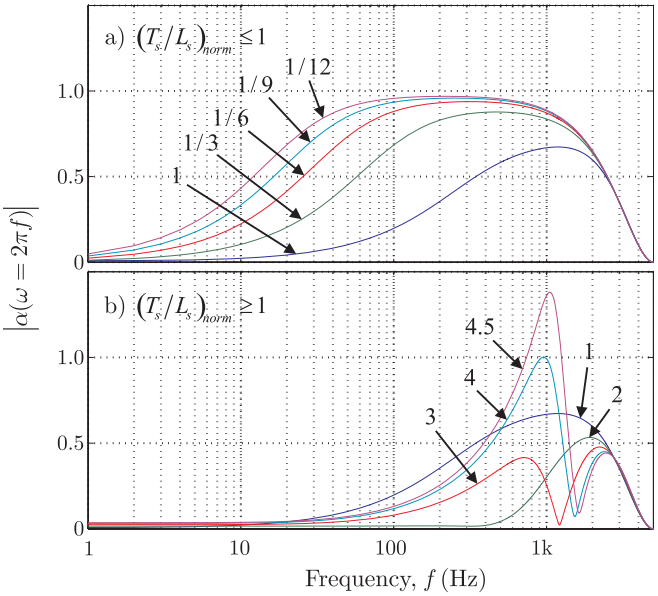

Fig. 7. Plots of $|\alpha(\omega)|$ for different values of T_s/L_s.

Fig. 8. Experimental setup.

V. Proposal Validation

A. Experimental Setup

The proposed control was experimentally tested to assess both its steady-state and dynamic performances in a small urban WPGS, shown in Fig. 8 (left). This H-rotor type wind turbine is suitable for locations with structural limitations and low-weight low-cost requirements. The WPGS is coupled to the grid through a three-phase four-wire grid-connected VSI (Fig. 1). The experimental prototype is shown in Fig. 8 (right). The main system parameters are listed in Table I. The inverter switches are implemented with Semikron SKM75GB176D IGBTs for improved ruggedness. The configured dead time for these switches is 2.5 μS, which ensures safe operation under any condition. On the other side, such high dead times (2.5% of T_s) have a noticeable impact on the output currents [8].

The digital control framework is composed of a custom board based on a Texas Instruments' microcontroller (μC)

TMS320F28335, which is a state-of-the-art device highly employed in power applications. All the control algorithms were implemented using 32-bit floating-point arithmetics. The 12-bit ADCs integrated onto the μC chip was used to sample all the control variables. A 16-bit enhanced digital 3PH-PWM (ePWM) module was employed to drive the power stage. To implement the variable sampling/switching frequency technique, the ePWM was configured to update its period and duty cycle with the new values only after the current period ends, ensuring the correct operation of control algorithms. This is possible because the ePWM features special buffer registers, which can be written at any time with the new values. An interrupt at the beginning of each PWM period synchronizes both control tasks and AD conversions. Notice that neither complex hardware nor additional software is required to implement a variable sampling/switching frequency.

The total calculation time required to implement the control tasks in the μC was 19 μs, from which 4 μs are for the processing of AD conversions, and the current control and synchronism algorithms employ only 15 μs. This proves the high computational efficiency of the method.

B. Steady-State Performance

Steady-state results are shown in Fig. 9, where the proposed control is compared against other proposals: a robust predictive current controller (RPCC) presented in [31], [35], and [36], and a classical PR controller with harmonic compensation (PR + HC) [14] (harmonic orders: $n = 3, 5, 7, 9, 11$). A sinusoidal current reference i_d of 20 A peak synchronized with the positive sequence of the grid was generated to inject 9.3 kW of active power. The feedforward term (24) was added to compensate the undesired LCL-filter capacitor current, as in Fig. 2. The grid phase voltage v_g is also shown, which exhibited high harmonic content ($\text{THD}_v = 4.8\%$) as expected for a weak urban grid.

Current is very distorted for the RPCC [Fig. 9(a)], with a THD higher than the standard limit of 5% [4]. Computational cost for the RPCC was 11 μs, this is 4 μs lower than the proposed RC. A significant reduction in THD is achieved by the PR + HC [Fig. 9(b)], however THD is very close to the limit. Moreover, computational cost resulted in 18 μs, which is 3 μs higher than the proposed RC. In both results, the high harmonic content produced by dead-time effects and the distorted grid voltage is clearly visible. This is not the case with the proposed RC [Fig. 9(c)], which achieves a THD$<$1%. Finally, to verify the effect of the capacitor current compensation (24), the feedforward term was removed from the reference signal (i.e., $i'_c = 0$), and the results are shown in Fig. 9(d). The THD reduction from Fig. 9(d) to (c) is possible because the RC can accurately track a reference of high harmonic content.

C. Power Transient Performance

Power flow adjustment in the grid-connected VSI of a WPGS is not only important but also a requirement of many standards that focus on integrating energies from renewable sources into the grid. Fast tracking of the active power

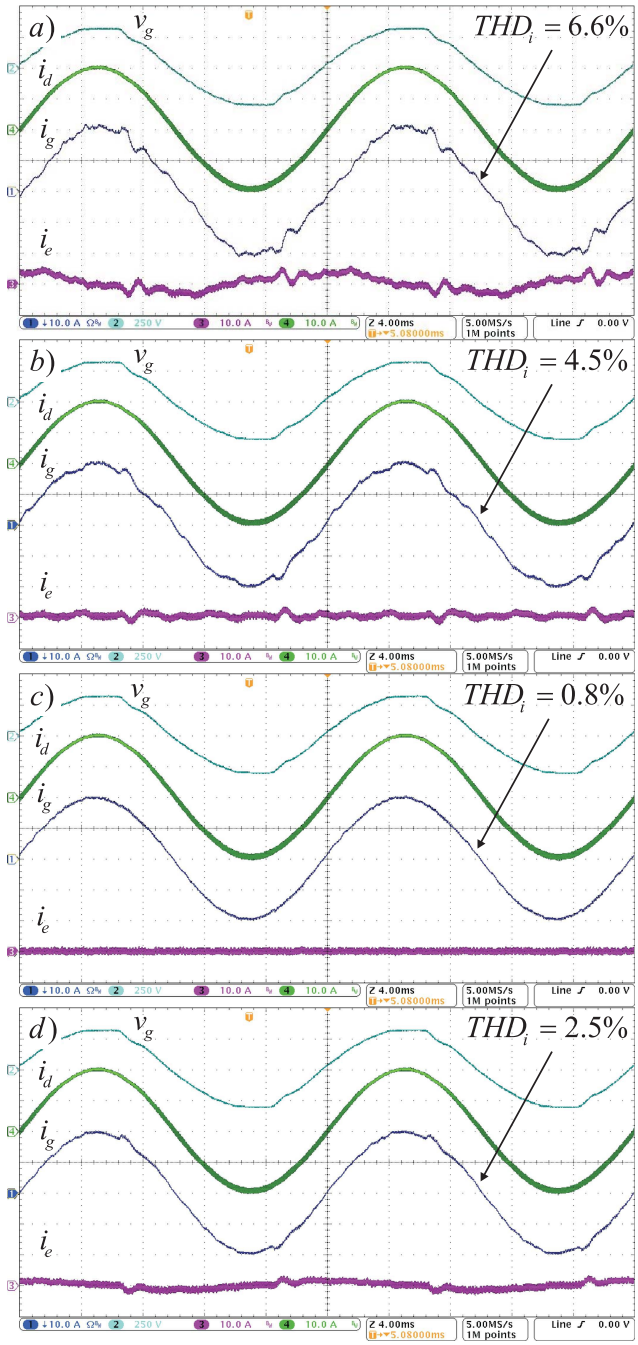

Fig. 9. Steady-state performance injecting 20 A peak per phase. (a) RPCC. (b) PR + HC. (c) Proposed RC. (d) Proposed RC without capacitor current feedforward compensation.

flow ensures extracting maximum power from gusts in small urban wind generators [37], and minimizes the energy storage requirements within the WPGS [3]. Fast tracking of reactive power flow is required to reduce grid voltage variations in the point of common coupling during wind power fluctuations or connection/disconnection of nearby heavy loads [5]. The dynamic response of the new control is evaluated with step changes in both active and reactive power (p^* and q^*) references. The response to a step change in the active power from 9.3 to 4.7-kW is shown in Fig. 10(a). The response to a step change in the phase between reference i_d and the grid positive

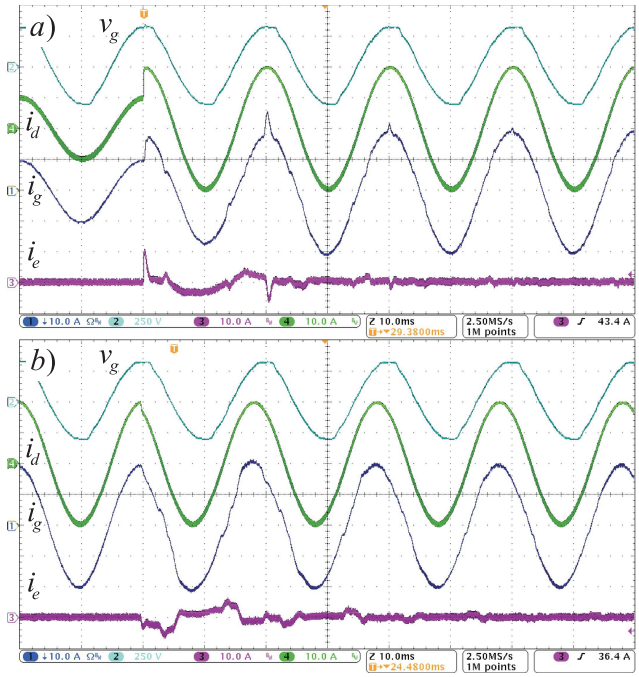

Fig. 10. Power transient performance. (a) p^* goes from 4.7 to 9.3 kW while $q^* = 0$. (b) p^* goes from 9.3 to 8.1 kW while q^* goes from 0 to 1.25 kVA.

sequence from 0° to 30° is shown in Fig. 10(b); this implies that $p^* = 9.3$ kW$\rightarrow$ 8.1 kW, and $q^* = 0 \rightarrow 1.25$ kVA. No significant current overshoots and fast convergence speed (less than three grid cycles) are observed. This ensures seamless transitions when the VSI follows the fast active and reactive power fluctuations required by the wind generator and the grid.

D. Frequency Transient Performance

Grid frequency variations become more important as the amount of grid-connected WPGS increases [37]. Indeed, some of the standards address this issue, and request the WPGS to remain connected even under large frequency changes (±6%) during some minutes (fault ride-through capability) [34]. A series of tests was conducted to assess the performance of the RC under frequency variations. First, the detrimental effect of having $f_s \neq Nf_g$ was considered. Since f_g cannot be changed in the experiments, f_s is changed instead in the same proportion, which yields equivalent results. In addition, using a fixed value for f_s requires the use of a standard SRF-PLL [38] instead of the VSPF-PLL. The results are shown in Fig. 11(a) and (b). A signal proportional to f_s (0.2 kHz/div and centered at 10 kHz) shows the frequency changes. In all the experiments, $f_g = 50$ Hz. In Fig. 11(a), f_s suddenly goes from 10 to 10.2 kHz, while in Fig. 11(b), it goes from 10 to 9.8 kHz. In both cases, the THD increases dramatically after a few cycles since the RC poles no longer lie on the desired harmonic frequencies. Instead, THD is always below 1% when f_s is dynamically adjusted by the VSPF-PLL.

The frequency-adaptive capability of the proposed control system was assessed by disturbing the VSPF-PLL algorithm to induce a transient condition in f_s, which emulates a transient in f_g. The results are shown in Fig. 11(c), where a signal proportional to T_s is shown instead of f_s (10 μs/div and

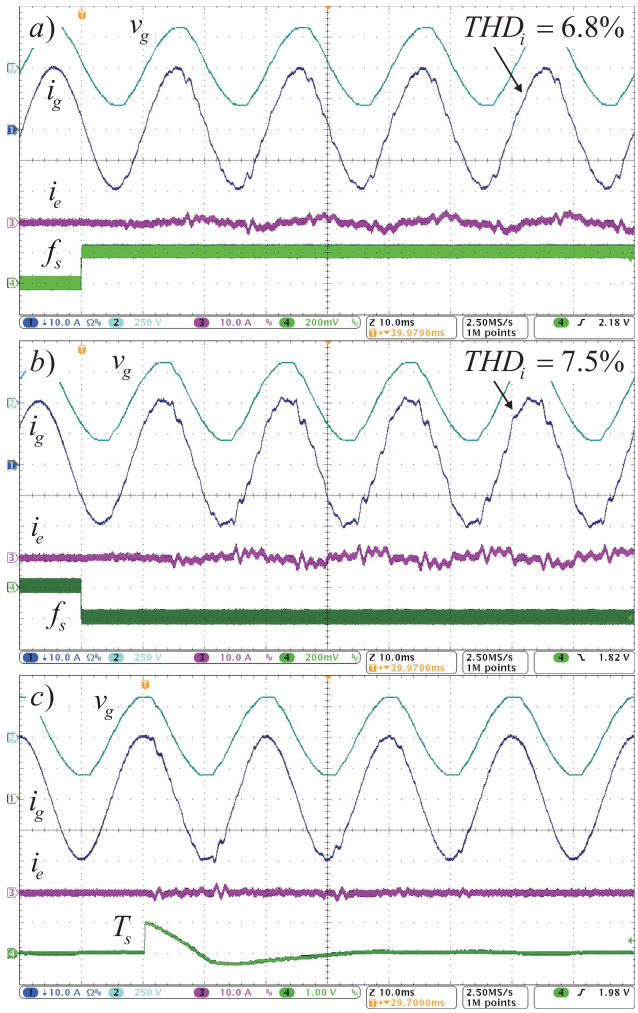

Fig. 11. Frequency transient performance. (a) f_s goes from 10 to 10.2 kHz. (b) f_s goes from 10 to 9.8 kHz. (c) Recovery after a transient in T_s.

centered at 100 μs). A perturbation of 10 μs ($T_s = 110$ μs) was injected into the algorithm, producing a small disruption in the current waveform, and normal operation was restored after two cycles. This test proves that even under a 10% step change in f_g, the dynamic response of the VSPF-PLL accommodates swiftly the output currents, rendering a fast compensation.

E. Performance Under Grid Disturbances and Faults

Simulations were carried out to assess the control system performance under severe grid faults and voltage unbalances. Experimental tests could not be conducted because no means to generate such conditions in a safe manner were available at our research laboratory. Accurate simulation models were employed matching the system parameters of Table I. Comparative tests combining RC with the standard SRF-PLL [38] and VSPF-PLL [30] are shown in Fig. 12. Grid phase voltages (v_{ga}, v_{gb}, and v_{gc}) are balanced and without distortion before t_0. A high distortion is applied to these voltages (THD$_v$ = 11.2%) from t_0 onward, as shown in Fig. 12(a). Then, a grid fault is applied on t_1: phase a is short circuited to ground ($v_{ga} = 0$), while v_{gb} and v_{gc} rise in magnitude and their phases rotate to be 180° from each other.

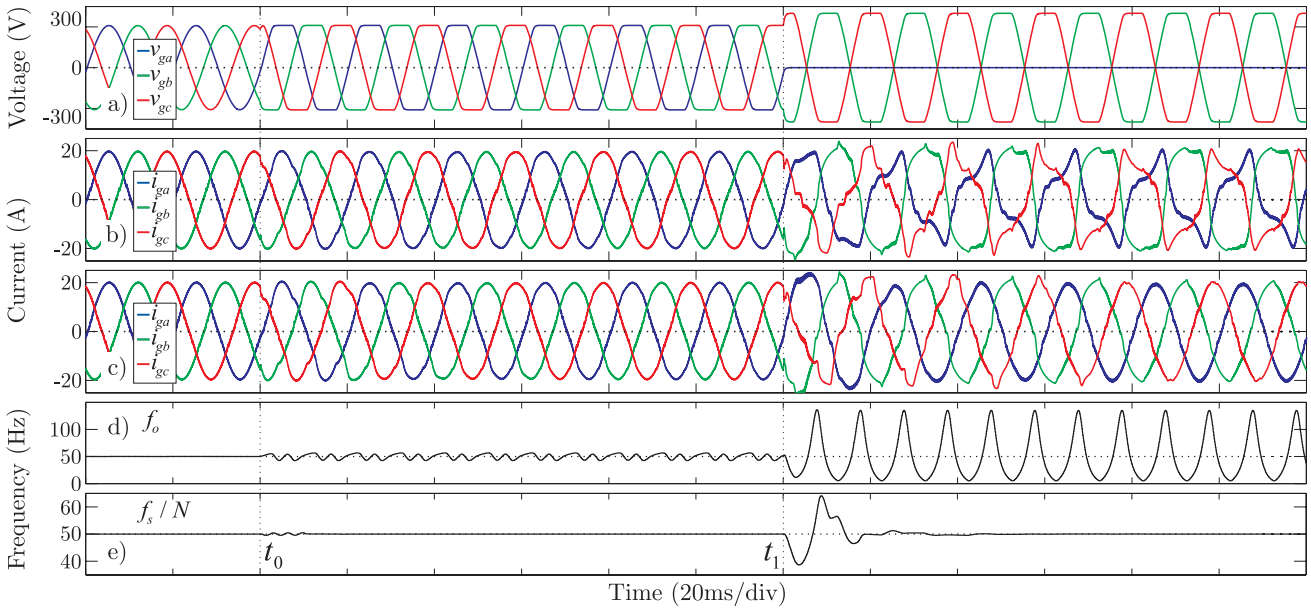

Fig. 12. Comparative results of the transient response employing the proposed control combined with both a standard SRF-PLL and the VSPF-PLL under severe grid disturbances and faults. (a) Grid voltages. (b) Currents with SRF-PLL. (c) Currents with VSPF-PLL. (d) SRF-PLL output. (e) VSPF-PLL output.

Before t_0, the phase currents show a $\text{THD}_i < 0.2\%$. During $t_0 < t < t_1$, THD_i increases to 4.1% with the SRF-PLL in Fig. 12(b), and 1.7% with the VSPF-PLL in Fig. 12(c). The THD_i obtained with the SRF-PLL is higher because voltage distortion also affects the reference signals. This can be noticed in the waveform of f_o in Fig. 12(d), whose integral yields the reference phase φ_u. The current references generated with this φ_u have a $\text{THD}_i = 2.7\%$. Instead, the VSPF-PLL output frequency shown in Fig. 12(e) is very clean, and produces references with $\text{THD}_i < 0.1\%$. When the grid fault is applied on t_1, no significant overshoots are observed in the currents due to a fast response of the inner loop. Current references are very distorted with the SRF-PLL due to an extreme disturbance in f_o of twice the grid frequency. As a consequence, phase currents exhibit high harmonic content ($\text{THD}_i > 30\%$), unacceptable for grid-connected applications. Instead, the VSPF-PLL filters out any component different from the fundamental positive sequence, so after one grid cycle both the output frequency f_s/N and the phase reference stabilize, and the reference signals become clean. In this case, five grid cycles after the fault, the THD_i drops to <1% for i_{ga} and <3% for i_{gb} and i_{gc}. This proves that the proposed control combined with the VSPF-PLL can obtain very low distortion currents even under severe grid faults, and arriving at steady state swiftly. These are very desirable properties for WPGS intended to have fault ride-through capabilities.

VI. Conclusion

An RC for WPGS was presented, which achieves optimal performance in steady-state conditions due to a VSPT. With this new control strategy, the loss of rejection due to grid frequency drift is corrected, as proven by the experimental results. The sampling/switching frequency is slightly adjusted around 10 kHz with a VSPF-PLL, which also adds robustness to the system due to its inherent tolerance to grid voltage distortion and unbalances, and events like frequency steps and grid faults. Since grid frequency drift is usually small during inverter operation, switching losses and LCL filter design remained unaffected by the variable frequency. Experimental results with a 10-kW WPGS also showed that distortion of injected currents remained very low ($\text{THD}_i < 1\%$) even under severe inverter nonlinearities (dead times of 2.5 μS), grid voltages with high harmonic content ($\text{THD}_v \approx 5\%$), grid frequency variations of $\pm 5\%$, and sudden grid faults. Convergence times were within a few grid cycles: three cycles to achieve $\text{THD}_i < 5\%$, and less than 10 cycles to achieve $\text{THD}_i < 1\%$ (steady-state value). This ensures a good tracking of the WPGS active and reactive power flow requirements, e.g., to maximize wind power extraction from gusts in small urban wind turbines and to help the grid to stabilize voltage fluctuations. Computational times in a state-of-the-art DSP were about 15% of a control period of 100 μs, which includes RC and PLL algorithms, proving that the solution is computationally efficient. The implementation of the variable frequency sampling is straightforward as it only requires a few standard hardware modules (configurable ADCs and PWMs), which are already embedded in the selected DSP. The proposed RC was compared through the experimental tests to other control strategies: an RPCC and a PR + HC. The tests showed the superiority of the method: $\text{THD}_i = 6.6\%$ and computational cost of 11 μs for the RPCC, $\text{THD}_i = 4.5\%$ and 18 μs for the PR + HC, and finally $\text{THD}_i = 0.8\%$ and 15 μs for the RC.

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