Methodology and Measurement Setup for Analog-to-Digital Converter Postcompensation

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***Abstract*— We present a methodology for nonlinearity compensation amenable to a wide variety of analog-to-digital converters (ADCs). To that purpose, a postcompensation scheme for a commercial ADC is presented and two compensator models are considered: 1) the memory polynomial (MP) and 2) the modified generalized MP. Since the proposed method does not use any information about the compensated architecture, it can be applied to different ADC designs. Furthermore, we address the measurement and characterization setup of the device under test by making a study of the quality of the signals involved to verify the improvement obtained. The issue of the training sequences required by the proposed compensation method is also addressed in detail. Despite the common use of a single training signal, we propose to use several sinusoids in the bandwidth of interest. With this, it is possible to show that the generalization properties of the estimated postcompensator are greatly enhanced compared with the case of a single sinusoid training sequence. As verified by the measurements, considerable gain in accuracy can be obtained using the proposed methodology. In particular, a 10-dB increment in spurious free dynamic range is obtained using the proposed postcompensators over the complete Nyquist frequency band.**

***Index Terms*— ADC characterization, ADC compensation, measurements.**

I. Introduction

THE TREND toward complete digital signal processing systems, even for applications that were partially restricted to the analog domain because of their high operation frequencies and large bandwidth, has created a demand for analog-to-digital converters (ADCs) of very high speed and low distortion [1], [2]. When considering the high-performance demand, the ADCs designed present static and dynamic nonlinear effects in their characteristic function that cause distortion in the discrete output signal [2], [3]. These nonlinearities originate in different subsystems of the converter, and deteriorate severely the overall performance. The main effect is harmonic distortion that degrades the dynamic range over the frequency band of interest, which leads to a loss in the effective ADC resolution. As a consequence, specific compensation of these nonlinear effects is required.

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An overview of the main compensation strategies found in the literature is presented in [4], which includes: lookup-table-based methods, dithering, model-inversion-based methods, and architecture-based methods. Lookup-table-based methods are well known and have been proved to be effective for static error correction. However, they are memory consuming when dynamics are considered and do not have good generalization properties, i.e., are only capable of correcting for errors that have been previously measured and stored [5]. Dithering methods apply a pseudorandom noise signal at the input of the ADC to decorrelate quantization noise from the input signal. Since nonlinear effects are not addressed, there are errors that dithering methods cannot compensate for [3], [4].

As a result, model inversion and postcompensation strategies have become more attractive alternatives and motivate active research. For example, a track-and-hold (T&H) device at the ADC input is modeled considering its nonlinear behavior in [6]. Mainly focusing on the effects of charge injection and nonlinear input-dependent resistance of the sampling switch, they propose a postcompensation strategy that effectively removes the distortion due to these particular effects. As another example, a postcompensation method is presented in [1], based on an integral nonlinearity (INL) model for pipelined ADCs. They compare their results with a dynamic lookup-table approach and show that similar performance can be obtained with reduced complexity, especially in terms of memory resources. Despite good examples of model inversion and postcompensation, these methods have specific limitations. The first approach does only address the nonlinear effects of charge injection and sampling switch nonideal behavior, and the latter is architecture dependent and does not consider the T&H nonlinear dynamics. In addition, compensation performance is degraded when the frequency of the input signal is different from the frequency of the training signal. Therefore, the issue of training signals must be carefully evaluated as well.

Another approach is an external (black box) compensation, disregarding any specific information about the underlying physics of the ADC nonlinearities. In that case, the ADC behavior is measured and an external circuit is applied to compensate at the required operating point [7]. A disadvantage of this alternative is that the solution obtained is also strongly dependent on the operating point at which the converter is used, i.e., the dynamic range and frequency range of the input signal. A possible alternative to this methodology is the use of model-based digital postcompensation techniques to reduce

the distortion. These techniques are generally based on the application of a compensating distortion of the digital output that cancels out the original distortion [8], [9]. They involve, in general, two steps: first, the postcompensator is trained (offline) using measurement data from converter; then, as a second step, online compensation is applied at the converter output. This methodology involves some extra digital processing.

Following these last ideas, and to obtain an adequate structure for the compensator, it is first necessary to consider the nonideal behavior of the device under test (DUT). In this sense, two alternatives for the postcompensator structure were considered in [10] for a sigma–delta converter (SDC): the memory polynomial (MP) [10], [11] and the modified generalized MP (MGMP) [10], which are particular forms of the more general Volterra model. These models have been proved to achieve good performance in the linearization of complex nonlinear dynamic systems, such as radio-frequency power amplifiers [11] and SDCs [10], with reasonable complexity when compared with the general Volterra series.

Suitable test (training) signals are also a key aspect of the postcompensation scheme proposed in this paper. The use of input–output data obtained by the actual measurements allows for a precise characterization of the acquisition system when proper input signals are used to excite it [12]. To that purpose, we consider the use of high signal-to-noise-plus-distortion (SINAD) ratio signals enhanced using filtering techniques, as suggested in [13]. The input signals usually considered in the literature are single-tone sinusoids [2], [3], [5], [14]. However, we propose the use of input signals composed of several sinusoids. As a result, the generalization properties of the estimated compensator are greatly enhanced.

In the following sections, the performance of the proposed method and compensators is evaluated on a 16-bit analog devices commercial ADC operating up to 130 MS/s. As described, a 10-dB improvement in spurious free dynamic range (SFDR) is obtained at reasonable postprocessing cost, showing the advantage of the proposed strategy.

As a brief summary, the main contributions of this paper are the following.

1) An ADC postcompensation scheme is proposed, where all nonlinear dynamic effects are jointly reduced, achieving great performance improvement in terms of resolution and SFDR enhancement.
2) Two efficient compensator models are evaluated on a high-resolution and high-speed commercial ADC, using input–output data from the actual measurements.
3) A training sequence composed of several sinusoids is proposed. When using this training signal to estimate the compensator parameters, the method is proved to be robust to mismatches between the training and sampled signals, and also leads to significant improvement over the whole Nyquist bandwidth.

The outline of this paper is given as follows. In Section II, a brief description of the compensator structure is discussed. Next, the measurement setup is described in Section III. A characterization by the measurements and some training signal considerations are introduced in Section IV, and the compensation results are presented in Section V. Finally, the conclusion is given in Section VI.

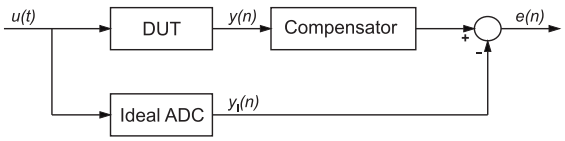

Fig. 1. Postcompensation scheme.

II. ADC Postcompensation

The postcompensation scheme proposed in this paper is shown in Fig. 1, where the ADC block is the DUT and the ideal ADC is the typical staircase characteristic. The test signal $u(t)$ feeds both the DUT and the ideal ADC. The output $y(n)$ of the DUT is applied to the input of the postcompensator. The postcompensator is designed to have an output $\hat{y}_I(n)$ that minimizes the error $e(n) = \hat{y}_I(n) - y_I(n)$, where $y_I(n)$ is the ideal ADC output. This reference value is generated separately using the test input signal $u(t)$. From this point of view, the compensator should include information on the inverse of the DUT and the ideal ADC.

The compensation scheme can be divided into two phases of operation: 1) a training mode in which the parameters of the model are estimated by the minimization of the error between its output and the reference, as shown in Fig. 1 and 2) a run mode, where the chosen parameters are used to predict the desired output of the model.

Two possible structures for the compensator, which consider the static and dynamic ADC nonlnearities, are: 1) the MP [11] and 2) the MGMP [10]. The MP model, shown in Fig. 2, turns out to be a generalization of the Hammerstein system [11], where multiple linear filters follow the static nonlinearity. Assuming an N-order polynomial and an M-order finite impulse response (FIR) filter, the compensator output is given by

$$\hat{y}_I^{MP}(k) = \sum_{n=1}^{N} \left[\sum_{m=0}^{M-1} \alpha_{nm} y^n(k-m) \right] \tag{1}$$

where $y(k)$ is the DUT output and $\hat{y}_I^{MP}(k)$ is the compensator output. The terms α_{nm} are the compensator parameters. This structure has the advantage that the output signal is a linear function of the unknown parameters (i.e., α_{nm}), which renders efficient parameter estimation through least-squares methods [15].

On the other hand, the MGMP model input–output relationship is given by

$$\hat{y}_I^{MGMP}(k) = \sum_{n=1}^{N} \left[\sum_{m=0}^{M-1} \alpha_{nm} y(k-m) \right]^n \tag{2}$$

which corresponds to the transposed form of the block diagram shown in Fig. 2, with the power terms coming after the FIR filter in each parallel branch.

MP and MGMP models are special cases of finite Volterra models [11], [16]. The model described by (2) is a generalization of a Wiener model, different from the GMP derived

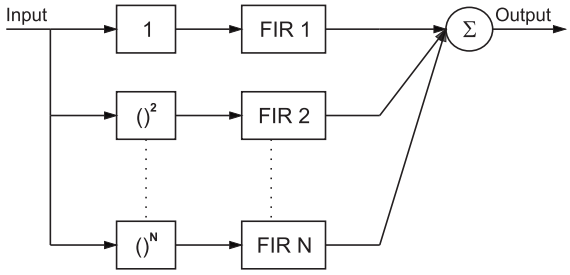

Fig. 2. Nth-order MP.

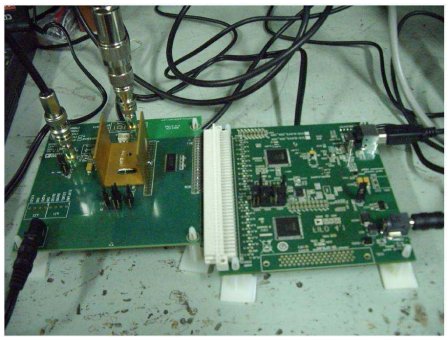

Fig. 3. AD9461 test kit.

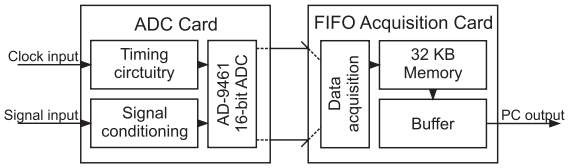

Fig. 4. Functional block diagram of AD9461 test kit.

in [11], where only lead and lag terms are added to the MP case. Note that, different to the MP model, the MGMP model includes cross terms at its output and, as a consequence, it has better modeling capabilities.

In the training mode, the model parameters can be estimated by minimizing the squared error defined as

$$\hat{\phi} = \arg\min_{\phi} \boldsymbol{e}^T \boldsymbol{e} = \arg\min_{\phi} \left(\boldsymbol{y_I} - \boldsymbol{Y}_\phi \hat{\phi}\right)^T \left(\boldsymbol{y_I} - \boldsymbol{Y}_\phi \hat{\phi}\right) \quad (3)$$

where $\boldsymbol{y}_I = [y_I(M+1)\ y_I(M+2)\ \cdots\ y_I(L)]^T$ is the vector formed by the outputs of the ideal converter where L data points are used for training, $\hat{\boldsymbol{y}}_I = \boldsymbol{Y}_\phi \phi$ is the vector of the compensator outputs with $\boldsymbol{Y}_\phi = [\boldsymbol{y}_\phi(M+1)\ \boldsymbol{y}_\phi(M+2)\ \cdots\ \boldsymbol{y}_\phi(L)]^T$ the matrix of observation data composed of the regressor vectors, and $\phi = [\phi_1^T\ \phi_2^T\ \cdots\ \phi_N^T]^T$ is the vector of parameters to be estimated.

The regressor and parameter vectors depend on the model structure. For the MP model

$$\boldsymbol{y}_\phi(k) = \left[y(k)\ y(k-1)\ \cdots\ y(k-M)\ \cdots\ y^N(k-M-1)\right]^T \quad (4)$$

$$\phi_n = \left[\hat{\alpha}_{n0}\ \hat{\alpha}_{n1}\ \cdots\ \hat{\alpha}_{nM}\right]^T \quad (5)$$

and for the MGMP model [considering different parameters for each product of the original parameters (α_{ni}) for $n = 1, 2, \ldots, N$ and $i = 0, 1, \ldots, M$]

$$\begin{aligned}\boldsymbol{y}_\phi(k) = \Big[&y(k) \cdots y(k-M-1)\ \ y^2(k)\ \ y(k)y(k-1)\cdots \\ &y^2(k-M-1)\ y^2(k)y(k-1)\cdots \\ &y^N(k-M-1)\Big]^T\end{aligned} \quad (6)$$

$$\boldsymbol{\phi}_n = \left[\alpha_{n0}^n\ \ \alpha_{n0}^{n-1}\alpha_{n1}\cdots\alpha_{n0}\alpha_{n1}\cdots\alpha_{nn}\cdots\alpha_{nM}^n\right]^T. \quad (7)$$

The training-mode solution is

$$\hat{\phi} = \left(\boldsymbol{Y}_\phi^T \boldsymbol{Y}_\phi\right)^{-1} \boldsymbol{Y}_\phi^T \boldsymbol{y}_I$$

where, to ensure the invertibility of $\boldsymbol{Y}_\phi^T \boldsymbol{Y}_\phi$, the condition of persistent excitation should be satisfied [16].

In the run phase, the predicted output is

$$\hat{\boldsymbol{y}}_I = \boldsymbol{Y}_\phi \hat{\phi}. \quad (8)$$

It is worth mentioning that the parameter estimation process is done only during the training mode. Thus, although the training mode takes more computing time for the MGMP, the complexity of implementation in the run mode remains equal for both approaches (as long as the order of the polynomial and the length of the FIR filters are the same).

III. Experimental Measurement Setup

A. Analyzed Converter

The DUT is the AD9461 ADC [17]. The test kit, shown in Fig. 3, is composed of two cards. The left card includes the converter, the signal conditioning circuits, and the clock circuitry. The right card is a first-in first-out data acquisition card with a memory of 32 kB, synchronism and temporization circuits, and USB interface for a PC link, as shown in Fig. 4. The ADC is excited by a high-quality function generator, which provides both the input and clock signals. The output of the data acquisition card is driven to a PC via USB.

The AD9461 is an ADC with a resolution of 16 bits and a maximum sampling frequency of 130 MS/s. This ADC was chosen due to its high-performance characteristics, which combine high conversion speed and resolution over a wide range of frequencies. The converter data sheet [17] specifies a maximum INL $= \pm 5$ LSB. According to [3], the reduction in effective resolution due to INL can be accurately modeled by

$$n_{\text{red}} = \log(1 + 3\text{INL}^2)/2\log(2) = 3.1240 \quad (9)$$

which implies a typical effective resolution of 12.876 bits.

Moreover, according to the manufacturer, the maximum measured SINAD (equal to 78 dB) occurs for a sinusoidal signal of 14.5 dBm at 10 MHz, which implies an effective number of bits (ENOB) of 13 bits, in the best case. However, many different error effects contribute to overall ENOB, such as INL/differential nonlinearity (DNL), eventual clock impurities, dynamic nonlinearity, and so on. In addition, a lower reference voltage in the ADC core also deteriorate the converter performance [17] and thus an even lower ENOB

should be expected. This information suggests that the performance of this converter can be considerably improved in terms of the effective resolution, enhancing the performance achieved by the circuit design via postcompensation, as shown in the following sections.

B. Instruments

The selection of adequate instruments is a key to obtain reliable measurements and results. In this sense, the spectral purity of the generator used to feed an input signal to the acquisition system should be as high as possible. In this manner, if any additional distortion is introduced by the generator, this should be lower than the actual distortion due to nonideal behavior of the DUT to be able to remove it regardless of the generator used. It is also important to use a generator with low time jitter to generate the clock signals to reduce any possible avoidable errors due to shifts in the sampling instants. Finally, a high-quality spectrum analyzer is required to verify the performance of the generators used and the behavior of the acquisition system itself prior to compensation.

The instruments used to perform the measurements are as follows.

1) A high-quality vectorial function generator (Rhode and Schwarz, Model SMU200A) with harmonics below -30 dBc, nonharmonics <-76 dBc, wideband noise measured at 1-Hz bandwidth <-146 dBc, and a SINAD greater than 45 dBfs for a 0-dBm power output signal, with harmonics of second and third orders. This generator has an extremely low time jitter, which allows the generation of high-quality clock signals and was therefore used for that purpose. The frequency range is 100 kHz–6 GHz.
2) A high-quality function generator (HP, Model 8640B) with nonharmonics <-100 dBc, wideband noise measured at 1-Hz bandwidth <-140 dBc, and harmonics below 54 dBc for a 0-dBm output signal. This generator has a frequency range from 500 kHz to 1 GHz. It was used to generate the input signals because of its lower levels of distortion.
3) A function generator (Agilent, Model 33220A) that generates monotonal signals up to 20 MHz with low distortion.
4) High-resolution spectrum analyzer (Agilent, Model E4407B): this instrument was used to measure the quality of the signals at the generator outputs, and to confirm the spectrum characteristics described in the instrument manual. The level of harmonic distortion was also verified with this instrument on the generated signals for different conditions of power and frequency. The input frequency range is from 9 kHz to 26.5 GHz.

C. Training Sequences

To perform the ADC postcompensation, it is first required to obtain input–output measurements with input signals that allow a complete excitation of the acquisition system dynamics. In this manner, it is possible to analyze the nonlinear effects over several working ranges. It is also important to cover the complete dynamic range of the converter. Multitone input signals are considered to that purpose. Despite considering its use in a different ADC architecture, it was shown in [10] that using this type of training signal, it is obtained a better linearization over a wider frequency range.

However, even though some function generators, such as the R&S described in the previous section, are capable of generating multitone signals, the achievable SINAD levels are below that required for the DUT in this paper (greater than 64 dBfs). In addition, a multitone test signal is problematic in practice, because the intermodulation distortion of the generator cannot be filtered, and therefore the spectral purity of such signal cannot be enhanced. Furthermore, even single-tone sinusoids generated by the available function generators listed above have lower SINAD levels than those required for the present application.

A possible solution to this issue is to enhance the spectral purity of sinusoids using filtering techniques (see next section) and combine them into a novel training signal (a sequence of stepped sinusoids that do not add up in time but are concatenated) with spectral components similar to those of an equivalent multitone signal. To that purpose, we first consider the expression of a time-limited sinusoid input signal

$$\begin{aligned} f(t) &= \cos(2\pi f_0 t)\left[u(t-t_i) - u(t-t_f)\right] \\ &= g_1(t)[g_2(t)] \end{aligned} \tag{10}$$

where $u(t)$ is the heavy-side step function, t_i is the initial time instant, and t_f is the final instant. In (10), the term between brackets defines a time window $g_2(t)$ inside which the signal takes the cosine value $g_1(t)$, such that $f(t)$ is zero for $t < t_i$ and $t > t_f$.

The Fourier transform of the time signal $f(t)$ in (10) is the frequency-domain convolution of the transform functions corresponding to $g_1(t)$ and $g_2(t)$, which are multiplied in the time domain. On the one hand, the transform of $g_1(t) = \cos(2\pi f t)$ is

$$G_1(f) = 1/2[\delta(f - f_0) + \delta(f + f_0)] \tag{11}$$

whereas on the other hand, $g_2(t)$ in (10) can be alternatively expressed as a rectangular function $g_3(t)$ with a time shift $t_0 = (t_f + t_i)/2$ and duration $\Delta t = (t_f - t_i)$, with Fourier transform

$$G_3(f) = \operatorname{sinc}(f) \tag{12}$$

such that the transform of $g_2(t)$ becomes

$$G_2(f) = e^{-j2\pi t_0 f}\frac{\Delta t}{2}\operatorname{sinc}\left(\frac{\Delta t f}{2}\right) \tag{13}$$

where t_0 is a phase shift in the frequency domain and Δt determines the width of the sinc function main lobe, which is narrower for larger Δt. Thus, the Fourier transform of $f(t)$ in (10) is

$$\begin{aligned} F(f) = {} & 1/2[\delta(f - f_0) + \delta(f + f_0)] \\ & \times e^{-j2\pi t_0 f}\frac{\Delta t}{2}\operatorname{sinc}\left(\frac{\Delta t f}{2}\right). \end{aligned} \tag{14}$$

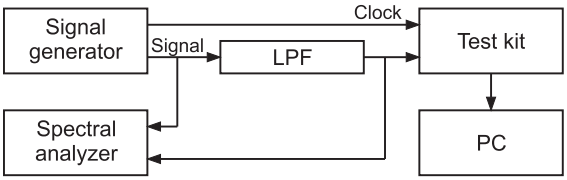

Fig. 5. Measurement setup.

Note that if $t_0 = 0$ and $\Delta t \to \infty$, then the sinc in (14) becomes an impulse and (14) reduces to (11).

Finally, a time-limited multitone signal composed of N tones within the same time window can be posed as

$$f_N(t) = \left[\sum_{n=1}^{N} \cos(2\pi f_n t)\right]\left[u(t-t_i) - u(t-t_f)\right]. \quad (15)$$

With the corresponding Fourier transform

$$F_N(f) = \frac{1}{2}\left[\sum_{n=1}^{N}[\delta(f-f_n) + \delta(f+f_n)]\right] \times e^{-j2\pi t_0 f}\frac{\Delta t}{2}\text{sinc}\left(\frac{\Delta t f}{2}\right). \quad (16)$$

We now consider a signal composed of several time-limited sinusoids that do not overlap over time, i.e., each sinusoid is multiplied by a different rectangular time window like the one described by (10), such that no overlapping in time occurs. In this case, we can express such signal in the time domain as

$$\tilde{f}_N(t) = \sum_{n=1}^{N}\left\{\cos(2\pi f_n t)\left[u(t-t_{in}) - u(t-t_{fn})\right]\right\} \quad (17)$$

with Fourier transform

$$\tilde{F}_N(f) = \frac{1}{2}\sum_{n=1}^{N}\left\{[\delta(f-f_n) + \delta(f+f_n)] \times e^{-j2\pi t_{on} f}\frac{\Delta t_{on}}{2}\text{sinc}\left(\frac{\Delta t_{on} f}{2}\right)\right\} \quad (18)$$

where $t_{on} = (t_{fn} + t_{in})/2$ is the time shift of the window corresponding to tone n and $\Delta t_{on} = (t_{fn} - t_{in})$ is the time duration of the associated window.

From (17) and (18), it can be observed that even though the sinusoid tones do not occur simultaneously in the time domain, the frequency components found in the spectrum of the signal [see (18)] are similar to those obtained using the multitone signal described in (15). While the ADC operates in the time domain and will only see one frequency at a time, the estimation of the compensator parameters is performed offline with the full training sequence including all frequency components, and thus the estimated compensator is able to remove nonlinearities in a wider frequency range.

IV. Characterization of the ADC by Measurement

Fig. 5 shows a block diagram illustrating the complete measurement setup with the function generator connected to the ADC card and the PC connected to the output of the acquisition card. The spectrum analyzer used to measure the output signals from the function generator is also shown.

The procedure for acquiring the measurement data is as follows. First, a clock signal of 130 MHz is generated with the R&S function generator and applied to the corresponding input of the ADC card for a sampling frequency of 130 MS/s. Then, the characteristics of the desired input signal, such as amplitude and frequency, are specified and set in the HP function generator, which is then low-pass filtered and connected to the signal input of the DUT card. The output data from the converter are then acquired and saved in memory.

The input signal is also necessary for the characterization and compensation of the DUT. Therefore, it is generated separately in MATLAB using the information available on the signal characteristics set in the function generator, i.e., frequency and amplitude. Then, the frequency offset and the initial phase of the input signal (at the instant where sampling begins) are estimated by choosing the values that minimize the rms error between input and output.

Before the evaluation of a specific postcompensation model, it is required to have as much knowledge as possible of the ADC performance and behavior in all working ranges.

The ADC allows the maximum input voltage to be varied to obtain the complete range of discrete codes at its output. This is used to eliminate saturation effects and minimize distortion at the output of the ADC due to an incomplete excursion of the input signal. These maximum input voltages depend on the reference voltage applied to the ADC core. The first specification sheet value for the reference voltage is 1.7 V [17], which allows sampling and conversion of an analog input signal of up to 3.4 V peak-to-peak (and 14.6-dBm power) without saturation effects. The second reference voltage value specified in the datasheet is 0.5 V, determining a maximum input signal of 1 V peak-to-peak and 4-dBm power. Finally, a reference voltage between 0.5 and 1.7 V can be externally applied. However, reducing the reference voltage of the converter below 1.7 V deteriorates the DUT linearity, especially in terms of the DNL [17]. Therefore, the ENOB of the DUT will be lower than the typical values specified in the datasheet.

Fig. 6 shows the measurement of SINAD at the generator outputs as a function of the frequency of a single-tone input signal with amplitude of 3.4 V peak-to-peak. In this figure, the solid line corresponds to the SINAD measured using the R&S function generator. The SINAD was also measured in the low-frequency range using the Agilent function generator (dashed line). In this case, a higher SINAD is obtained, and it can be observed that it follows the solid line trend at higher frequencies. The interpretation for this result is that the useful frequency range for the R&S function generator lies above 20 MHz, and below this frequency, the generator introduces high spurious components in the signal spectrum.

Note that the SINAD levels shown in Fig. 6, measured at the output of the R&S and Agilent generators, correspond to an ENOB between six and nine bits. This is lower than the effective resolution of the ADC in the worst case. This is due to the performance of the signal generator, since even though the noise level remains constant, the harmonic distortion of the generated signal increases as a function

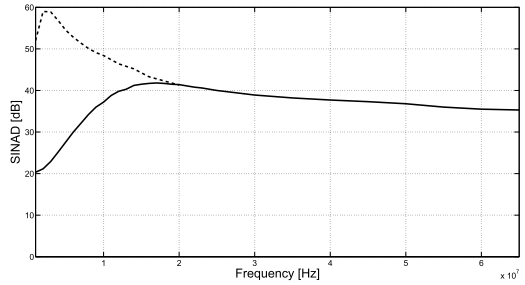

Fig. 6. SINAD as a function of frequency.

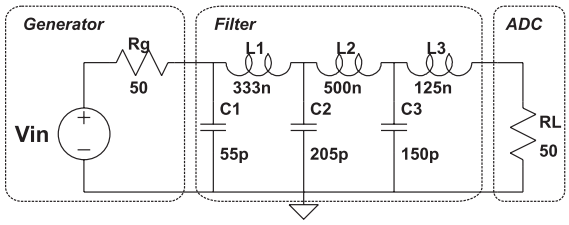

Fig. 7. Circuit diagram of a sixth-order Butterworth filter with cutoff frequency of 28 MHz.

of the required output power. For example, with a sinusoid output signal of 3.4 Vpp (i.e., 14.6 dBm), the R&S function generator provides a signal with a second harmonic only 35–40 dB below the fundamental frequency. This value determines a maximum SINAD of 35–40 dBfs, equivalent to an ENOB of five to six bits, as can be observed in Fig. 6. As a result, since the ADC SINAD lies between 60 and 78 dBfs, the distortion due to the ADC nonlinearity at its output is masked by the harmonic distortion present in the input signal provided by the generator. This means the SINAD of signals at the output of the generator (i.e., input signals for the DUT) has to be enhanced. Otherwise, the signal at the DUT output will be just a quantized version of the generator signal and no information on the ADC will be captured. However, despite the need of high SINAD signals at the input of the ADC, thermal noise may present a limit to the achievable performance.

The harmonic distortion at the output of the signal generator can be reduced by changing the ADC reference voltage to 0.5 V. However, in this case, the output power provided by the R&S function generator is 4 dBm and the second harmonic in the generated signal is 45–50 dB below the fundamental. This SINAD value is still insufficient to measure the nonlinear effects of the DUT at its output. Therefore, a way must be found to further reduce the level of harmonics at the ADC input. A possible solution is to low-pass filter the signal generator output with a high-order passive filter [13]. For example, Fig. 7 shows the schematic of a sixth-order Butterworth low-pass filter with a cutoff frequency of 28 MHz, and its frequency response is shown in Fig. 8. Several filters of this type were used in the measurement process, each of them with cutoff frequency equal to the frequency of the input signal. The amplitude of the input signal was adjusted in every case to obtain 0.5 V at the output of the low-pass filter. The ADC reference voltage was set to 0.5 V and thus the input signal fits within the full scale range of the converter.

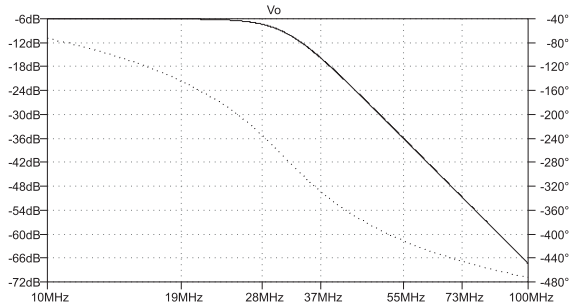

Fig. 8. Frequency response in amplitude (solid line) and phase (dashed line) of the filter in Fig. 7.

V. Compensation Result

The best possible scenario for the compensation of an ADC in terms of resolution enhancement is when sampling a sinusoid signal of known frequency. In this case, either the compensator model fails to capture the dynamics of the system and thus does not linearize the output of the ADC, or it does capture the dynamic behavior of the DUT and achieves an increment in the ENOB. In the latter case, the improvement is most likely to be higher than that obtained for a sampled signal of frequency different than the signal used for training.

Hence, as the first step in the process of postcompensation for the DUT, we propose testing the models presented in Section II for a sampled signal of 36 MHz. This signal was low-pass filtered with a sixth-order passive Butterworth filter, as described in Section IV, and represents the worst case among the measurements taken in terms of SINAD. The SINAD at the output of the filter (measured with the spectrum analyzer) was 72.5 dBfs, and the SINAD at the output of the DUT (measured with the ADSim software from Analog Devices) was 64.5 dBfs. Therefore, an increment of 8 dB is possible, equivalent to 1.4 bits in the ENOB. This increment is close to two bits for the rest of the measurements available at other frequencies. From the 32 000 input–output data points obtained (following the procedure described in Section III), the first 20 000 were used to train both an MP and an MGMP compensator and the remaining 12 000 were used for validation.

For the first test, we trained several compensators of each type for a polynomial of order three, as a function of the length of the FIR filters M. The results are shown in Fig. 9. As can be seen, the MGMP compensator outperforms the MP. This was likely to be expected, as the MGMP model is more general in the sense that cross terms between past samples are considered. Hence, from now on, we will focus our analysis on the MGMP compensator.

Several MGMP models were trained for polynomial order $N = 2, 3$, and 4 as a function of M. The improvement in both ENOB and SINAD is shown in Fig. 10 for validation data obtained by sampling the 36-MHz sinusoid signal. From this figure, it can be observed that the performance for polynomials of order three and four is almost the same, whereas the performance is poorer when using a polynomial of order two.

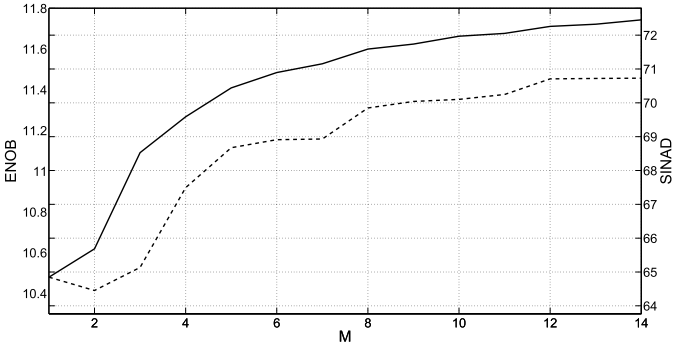

Fig. 9. ENOB and SINAD versus M for MGMP compensator (solid line) and MP (dashed line) using third-order polynomials.

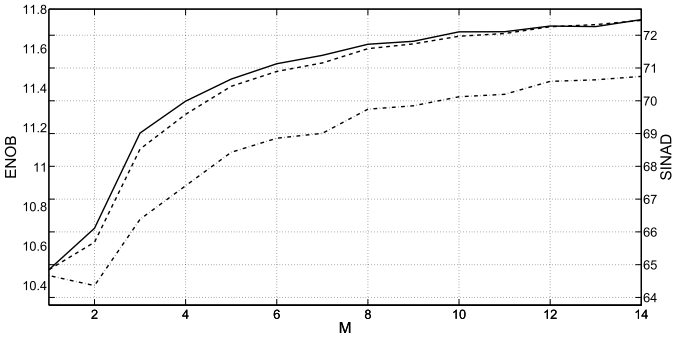

Fig. 10. ENOB and SINAD versus M for polynomials of order two (dot dashed), three (dashed), and four (solid).

It can also be seen that less than 5% of additional improvement occurs for $M > 12$. Thus, $N = 3$ and $M = 12$ are chosen.

The general idea behind the proposed compensation strategy is to train a compensator using as much information as possible about the ADC dynamics in all operating regions (i.e., over a wide range of frequencies). In this manner, the postcompensator should be able to improve the performance in terms of resolution enhancement independently of the frequency of the sampled signal. To do so, we propose the use of a more complete signal for training, obtained by concatenation of input–output data from filtered sinusoid signals of different frequencies.

For that purpose, the ideal input signal should be white noise. However, practical issues prevent the use of this type of signal, not only because it is difficult to generate but also because it is not possible to measure the DUT nonlinear distortion.

Instead, we propose the use of stepped sinusoids of several frequencies as the training sequence. In this case, it is important to select a number of tones greater than the memory of the system. Therefore, we use 17 sinusoids for training the compensator, and we validate the postcompensator technique for eight different frequencies to those used for training.

Fig. 11 shows the SINAD improvement as a function of frequency. It can be seen that the compensator is able to enhance the SINAD for all the measured frequencies.

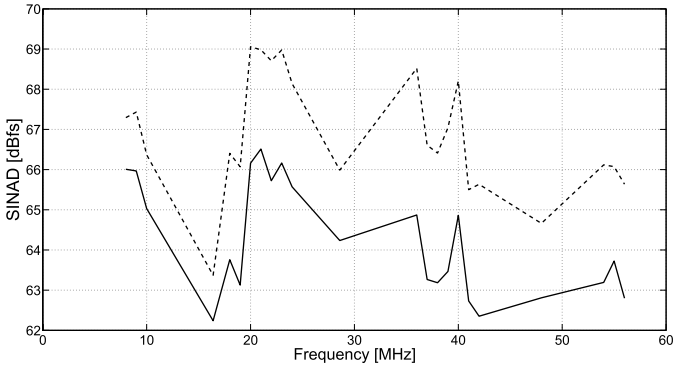

Fig. 11. SINAD versus frequency of the DUT (solid line) and the compensator output (dashed line).

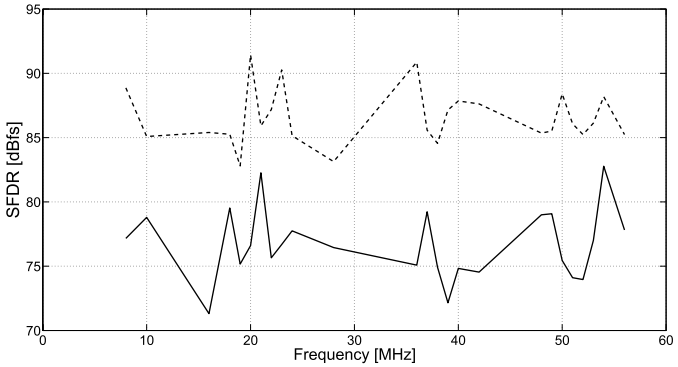

Fig. 12. SFDR versus frequency of the DUT without compensation (solid line) and after compensation (dashed line).

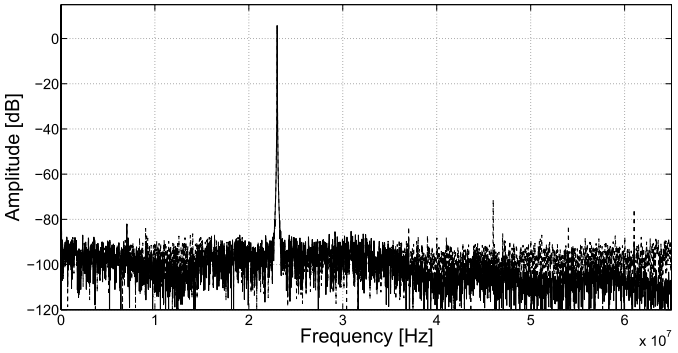

Fig. 13. Output spectrum of the DUT without compensation (dashed line) and after compensation (solid line).

Fig. 12 shows the SFDR of the DUT and that of the compensator output, where an average improvement of 10 dB is obtained for all cases.

Fig. 13 shows the output spectrum of the DUT before and after compensation for an input sinusoid of 23 MHz, not included in the training sequence. It can be observed in this figure that distortion is successfully reduced, particularly in terms of SFDR enhancement.

VI. Conclusion

A complete description of a measurement setup and methodology for postcompensation of ADCs has been presented. Two postcompensators in the form of MP and MGMP models are used to compensate a commercial ADC. Due to its better

modeling capabilities, it is shown that MGMP outperforms MP compensator.

Significative improvement is obtained in terms of resolution enhancement for the case of the MGMP compensator when the frequency of the input signal is known.

It is shown that the use of several frequencies during the training phase greatly enhance the generalization properties of the compensator, at the cost of a lower improvement in terms of SINAD. However, a significant improvement is obtained in SFDR in the whole Nyquist bandwidth. Furthermore, the increment obtained (over the whole Nyquist band) is not frequency dependent when using a set of stepped sinusoids during the training phase.

Finally, the order of the nonlinearity and the memory of the system dynamics are determined, allowing this information to be used for other approaches.

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