Architecture of a Single-Chip 50 Gb/s DP-QPSK/BPSK Transceiver With Electronic Dispersion Compensation for Coherent Optical Channels

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***Abstract*—The architecture of a single-chip dual-polarization QPSK/BPSK 50 Gigabits per second (Gb/s) DSP-based transceiver for coherent optical communications is presented. The receiver compensates the chromatic dispersion (CD) of more than 3,500 km of standard single-mode fiber using a frequency-domain equalizer. A time-domain four-dimensional MIMO transversal equalizer compensates up to 200 ps of differential group delay (DGD) and 8000 ps^2 of second-order polarization-mode dispersion (SOPMD). Other key DSP functions of the receiver include carrier and timing recovery, automatic gain control, channel diagnostics, etc. A novel low-latency parallel-processing carrier recovery implementation which is robust in the presence of laser phase noise and frequency jitter is proposed. The chip integrates the transmitter, receiver, framer and host interface functions and features a 4-channel 25 Gs/s 6-bit ADC with a figure of merit (FOM) of 0.4 pJ/conversion. Each ADC channel is based on an 8-way interleaved flash architecture. The DSP uses a 16-way parallel processing architecture. Extensive measurement results are presented which confirm the design targets. Measured optical signal-to-noise ratio (OSNR) penalty when compensating 200 ps DGD and 8000 ps^2 is 0.1 dB, while OSNR penalty when compensating 55 ns/nm CD (corresponding to 3,500 km of standard single-mode fiber) is 0.5 dB.**

***Index Terms*—Bulk equalization, coherent, DSP, EDC, equalization, framer, interleaved ADC, optical fiber, parallel processing, single-mode, SMF.**

I. Introduction

OPTICAL communication technology in long-haul and metropolitan links is experiencing a transition to coherent techniques and high spectral efficiency modulation formats such as dual-polarization quadrature phase shift keying (DP-QPSK), dual-polarization quadrature amplitude modulation (DP-QAM) and orthogonal frequency-division multiplexing (OFDM). Unlike direct detection, coherent demodulation preserves all amplitude, phase and polarization information present in the received optical signal, thus enabling a penalty-free equalization of fiber optic impairments such as chromatic dispersion (CD) and polarization-mode dispersion (PMD). The combination of coherent demodulation and DSP allows costly optical signal processing hardware traditionally used to compensate fiber impairments to be replaced by DSP-based techniques [1]. Economic large-scale deployment of coherent systems requires the integration of the optical transceiver functions in CMOS technology.

This paper describes a 50 Gb/s single chip 40 nm CMOS DP-QPSK/BPSK transceiver capable of transmission over up to 3,500 km of standard optical fiber. This is the first coherent optical transceiver described in the technical literature incorporating transmit, receive, framer, host interface and analog front end (AFE) functionality in a single CMOS chip. The prior art in high-speed transceivers is presented in two distinct groups of publications. The first group [2]–[5], describes DSP-based transceivers for coherent optical communications of characteristics comparable to the work presented here, although typically with a lower level of integration. For example, transmitter and receiver are implemented in separate chips. This group of publications focuses on system performance measurements in the laboratory or in field tests, but it does not provide details on the architecture and circuit implementation of the transceivers. By contrast, the focus of this paper is architecture and circuit implementation. The second group [6], [7] provides detailed descriptions of the transceiver implementations, but the functionality and the applications presented are significantly different from this work. The applications are backplanes or direct-detection optical channels, the implementation is predominantly analog, the functionality, particularly the signal processing algorithms implemented, is much simpler, and one of the main objectives sought is minimizing the power dissipation.

The transceiver described here builds upon the prior art in the following ways: 1) The transmitter, framer and host interface are integrated with the DSP; 2) The PMD compensation is doubled from the previously published range in [4], [5], [8]; 3) A combination of feedback and feedforward fine carrier recovery (FCR) optimizes performance in the simultaneous presence of laser short-term frequency instabilities and phase noise; 4) It incorporates automatic fiber length estimation (FLE), adaptive

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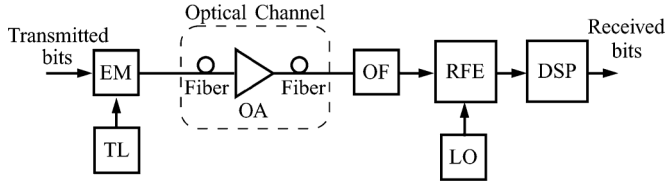

Fig. 1. System model. EM, external modulator; TL, transmitter laser; OA, optical amplifier; OF, optical filter; RFE, receiver front-end; LO, local oscillator; DSP, digital signal processor.

coarse carrier recovery (CCR) with 5 GHz capture range, and channel diagnostics functions.

One of the challenging blocks in the coherent transceiver is the 4-channel 25 Gs/s 6-bit ADC. This block is described in Section V.B, with additional details given in [9]. This paper focuses on the signal processing, framing, and control functionality as well as on the chip architecture.

The maximum symbol rate supported by the transmitter is 12.5 GBaud, which results in 50 Gb/s data rate when using DP-QPSK or DP-DQPSK modulation (with a modulation efficiency of 2 bits per symbol per polarization), and 25 Gb/s when using DP-BPSK (with a modulation efficiency of 1 bit per symbol per polarization). However, the chip supports lower symbol rates as well, in the range 10–11.5 GBaud for one metal mask option, and 11.5–12.5 GBaud for another metal mask option. Although the frequencies of the various clocks discussed throughout the paper, such as ADC sampling clocks and DSP clocks assume a 12.5 GBaud symbol rate, they scale linearly for other symbol rates.

The rest of this paper is organized as follows. Section II describes the channel under consideration. Section III provides a summary discussion of the transceiver block diagram. Sections IV and V provide in-depth descriptions of the egress and the ingress paths, respectively. Section VI summarizes the ADC and DSP architecture. Section VII presents experimental results. Finally, conclusions are drawn in Section VIII.

II. The Coherent Optical Channel

Fig. 1 shows a simplified model of the system under consideration. The transmitted bits externally modulate the intensity and/or phase of the transmitter laser (TL). The optical fiber introduces chromatic and polarization mode dispersion, as well as attenuation. Optical amplifiers (OA) deployed periodically along the fiber compensate the attenuation and introduce amplified spontaneous emission (ASE) noise. The received signal is optically filtered and applied to the receiver front-end (RFE). Then, the optical signal is mixed with a local oscillator (LO) laser and demodulated to baseband. The RFE is similar to the one of an 8-branch double balanced phase and polarization diversity receiver [10], with the exception that the four diversity branches are not immediately combined. Instead, they are treated as a four-dimensional vector to be processed by the digital receiver. The four components of the demodulated signal are sampled at twice the symbol rate, and fed into the digital receiver for subsequent equalization and detection.

Let $P(\omega)$ be the Fourier transform of the total pulse, $p(t)$, which includes the transmit and receive filters. In the presence of CD and PMD, the channel transfer matrix can be expressed as

$$\mathbf{H}(\omega) = H_{\mathrm{CD}}(\omega, L) P(\omega) \mathbf{J}(\omega) \tag{1}$$

where ω is the angular frequency, L is the fiber length, $H_{\mathrm{CD}}(\omega, L)$ models CD, and $\mathbf{J}(\omega)$ is the well-known Jones matrix defined by

$$\mathbf{J}(\omega) = \begin{bmatrix} U(\omega) & V(\omega) \\ -V^*(\omega) & U^*(\omega) \end{bmatrix} \tag{2}$$

where * denotes complex conjugate. Matrix $\mathbf{J}(\omega)$ is unitary (i.e., $\det(\mathbf{J}(\omega)) = 1$) and models the effects of the PMD.

Chromatic dispersion is modeled by the following transfer function:

$$H_{\mathrm{CD}}(\omega, L) = \exp\left(\frac{1}{2} j\beta_2 L\omega^2 + \frac{1}{6} j\beta_3 L\omega^3\right) \tag{3}$$

where β_2 and β_3 are related to the dispersion parameter D and the dispersion slope S by the following equations:

$$D = \frac{2\pi c}{\lambda^2}\beta_2 \tag{4}$$

and

$$S = \left(\frac{2\pi c}{\lambda^2}\beta_2\right)^2 + \left(\frac{4\pi c}{\lambda^3}\beta_3\right). \tag{5}$$

Note that a coherent receiver can compensate for PMD and CD impairments without optical signal to noise ratio (OSNR) penalty. This comes from the fact that (2) is a unitary matrix and (3) generates only phase distortions. Nevertheless, in practice there is some penalty owing to electrical and optical imperfections or departures from the ideal coherent channel model, such as those caused by electrical filters and polarization dependent loss (PDL).

Let $a_n^{(H)}$ and $a_n^{(V)}$ be the QPSK/DQPSK/BPSK symbols to be transmitted in polarizations horizontal (H) and vertical (V), respectively. We also define $s^{(H)}(t)$ and $s^{(V)}(t)$ as the complex signals at the receiver input for polarizations H and V, respectively. The total input signal can be expressed as

$$\overrightarrow{s}(t) = \begin{bmatrix} s^{(H)}(t) \\ s^{(V)}(t) \end{bmatrix} \tag{6}$$

with

$$s^{(H)}(t) = \left[\sum_{k=-\infty}^{\infty} h_{11}(t-kT)a_k^{(H)} + h_{12}(t-kT)a_k^{(V)} + z^H(t)\right] e^{j\phi^{(H)}(t)} \tag{7}$$

$$s^{(V)}(t) = \left[\sum_{k=-\infty}^{\infty} h_{21}(t-kT)a_k^{(H)} + h_{22}(t-kT)a_k^{(V)} + z^V(t)\right] e^{j\phi^{(V)}(t)} \tag{8}$$

where $1/T$ is the symbol rate, $a_n^{(H)}$ and $a_n^{(V)}$ are independent and identically distributed data symbols such $E\{a_k^{(H)}(a_m^{(H)})^*\} = E\{a_k^{(V)}(a_m^{(V)})^*\} = \delta_{m-k}$ with δ_k being the discrete time impulse function; $\phi^{(H)}(t)$ and $\phi^{(V)}(t)$ are the phase noise components on each polarization, while

$$h_{11}(t) = \mathcal{F}^{-1}\{H_{\mathrm{CD}}(\omega, L)P(\omega)U(\omega)\} \quad (9)$$

$$h_{12}(t) = \mathcal{F}^{-1}\{H_{\mathrm{CD}}(\omega, L)P(\omega)V(\omega)\} \quad (10)$$

$$h_{21}(t) = \mathcal{F}^{-1}\{-H_{\mathrm{CD}}(\omega, L)P(\omega)V^*(\omega)\} \quad (11)$$

$$h_{22}(t) = \mathcal{F}^{-1}\{H_{\mathrm{CD}}(\omega, L)P(\omega)U^*(\omega)\} \quad (12)$$

where $\mathcal{F}^{-1}\{\cdot\}$ denotes the inverse Fourier transform. Terms $z^H(t)$ and $z^V(t)$ model the noise component on each polarization. The input signal $\overrightarrow{s}(t)$ can be treated as a four-dimensional *real* vector:

$$\mathbf{s}(t) = [s^0(t)\ s^1(t)\ s^2(t)\ s^3(t)]^T \quad (13)$$

where $s^0(t)$ and $s^1(t)$ ($s^2(t)$ and $s^3(t)$) are the in-phase and quadrature components of $s^{(H)}(t)(s^{(V)}(t))$, respectively, while superscript ^{T} denotes transpose.

III. Transceiver Block Diagram

Fig. 2 shows a simplified block diagram of the chip. The transceiver encompasses two major sections, the egress path and the ingress path, with independent clock generation units (CGUs). The egress path receives data from the host and passes it to the framer and multiplexer, then to the QPSK/DQPSK/DBPSK encoder and finally to the line transmitter. The output of the line transmitter consists of four differential channels, representing the in-phase and quadrature components of the two polarizations, which drive the optical modulator through a modulator driver amplifier (Fig. 3). Serial clock outputs at the symbol rate are provided to facilitate the operation of the optical modulator. Similarly, the line side of the ingress path consists of the in-phase and the quadrature components of the two polarizations, which are generated by the optical demodulator and amplified by four external trans-impedance amplifiers (TIAs). The ingress path encompasses the AFE, the DSP core where most of the receiver signal processing takes place, the ingress path section of the framer and multiplexer, and the ingress path section of the host interface. The transceiver also incorporates a serial peripheral interface (SPI) which provides access to registers used to control the device operation, read or write parameters and coefficients, and read status signals, and a diagnostic unit, which provides a host of observability and controllability features used for testing, characterization, and channel diagnostics. The most important DSP blocks are the bulk chromatic dispersion equalizer (BCD), the feedforward equalizer, the carrier recovery, the timing recovery and the automatic gain control (AGC). These bocks will be described in detail in Section V. As a result of the high symbol rate of this transceiver and the speed limitations of current CMOS technology, parallel processing is required in the DSP and framer blocks. The parallelization factor used in all blocks of the transceiver except the BCD equalizer is 16. This means that 16 symbols are processed in a single clock cycle. Therefore, the DSP clock frequency for all blocks except the BCD is 12.5 GHz/16 = 781.25 MHz. The BCD equalizer, as described in Section V-C2, takes two blocks of 256 input samples. Each one corresponding to one polarization. In order to reduce complexity, the two blocks are processed by the same hardware, in a systolic fashion. Based on this architecture, the clock cycle needed for the BCD is 781.25 MHz/4 = 195.3 MHz. Table II in Section VI summarizes the clock rates and other parameters for the various blocks of the transceiver. It is interesting to mention that clock speeds in highly parallel architectures such as the one described here are limited to frequencies well below 1 GHz by present CMOS technology. This is because highly parallel DSP functions require elaborate logic which results in long critical paths. Use of synthesis and automatic place and route for all the digital blocks of the transceiver also contributes to longer critical paths than would be possible in a full custom design. Notice that applications such as high end CPUs and read channel devices for magnetic recording typically use much faster clocks (in the several gigahertz range), but they use pipelined architectures with extremely short critical paths instead of parallel processing. However pipelined architectures are not sufficient to reach the speed required in coherent optical communications, at least not in current CMOS technology. This situation may change in the future.

It is important to understand how the transceiver interfaces with the optical channel. Fig. 3 shows typical transmit and receive optical front ends and their relationship with the transceiver. On the transmit side, the signal is generated by a continuous wave (CW) laser, and split into two components representing the horizontal and vertical components of the polarization vector. These are independently modulated in phase and quadrature by Mach-Zehnder modulators, and then recombined to generate the DP-QPSK transmitted signal. On the receive side, the two polarization components are separated by a polarization beam splitter, mixed with the signal generated by the local oscillator (LO) by 90° hybrids and demodulated to baseband. The results of the demodulation are four signals representing the in-phase and quadrature components of the two polarizations. These components preserve all amplitude, phase, and polarization information present in the input optical signal. This property of coherent demodulation, together with the fact that (i) CD is a purely phase distortion (it does not affect the magnitude of the optical signal, as can be seen from (3)), and (ii) PMD is described by a frequency-dependent unitary transformation, is instrumental to make perfect equalization of the CD and PMD of the optical fiber possible. Unlike linear equalization of most other channels, linear equalization of CD and PMD in coherent optical channels does not result in noise enhancement.

It is important to realize that the LO is not phase-locked to the transmitter, therefore the demodulated signal may have a residual carrier whose frequency depends on the accuracy of the LO. The architecture where the LO is not phase locked to the transmitter is called *intradyne* [1]. Compared to the more traditional heterodyne or homodyne architectures, the intradyne architecture has the important advantage of not requiring an optical phase-locked loop. Typical values for the residual carrier frequency are in the range 0–5 GHz. This carrier is tracked by the carrier recovery subsystem in the receiver.

IV. Egress Path

A. Overview

The egress path includes the 16 bit wide SFI 5.1 host interface. Each data input operates at the nominal rate of 3.125 Gb/s for an aggregate nominal data rate of 50 Gb/s. Inputs are CML and include clock and deskew pins. The SFI 5.1 Interface includes a 3.125 GHz clock output synchronous to the reference clock. This clock output allows the host to use a forward clocking scheme where the transceiver generates the clocking

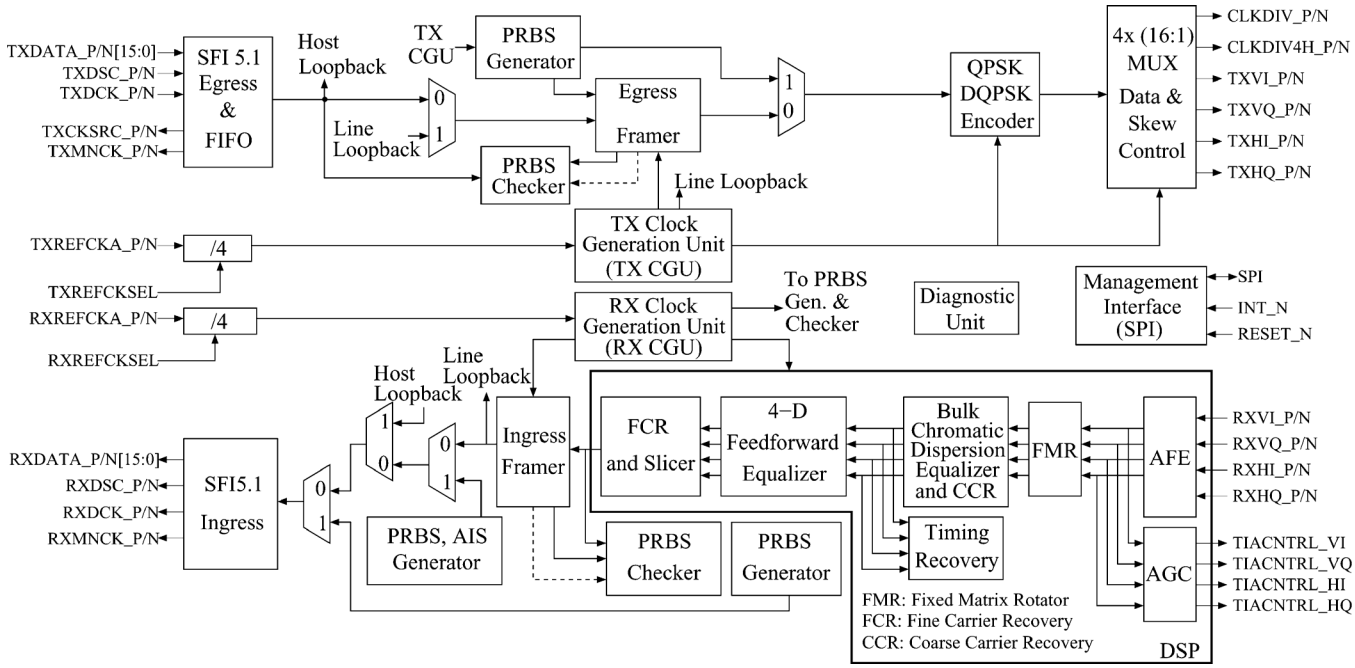

Fig. 2. Transceiver block diagram.

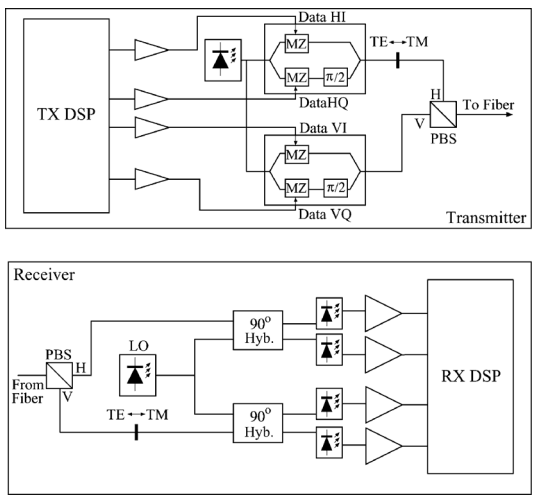

Fig. 3. Receiver and transmitter front ends.

used by an external downstream framer/forward error correction (FEC) code or network processor. The egress path includes an optional framer and PRBS generator. The framer finds frame boundaries if the data received from the host interface is formatted in OTU3 frames. Optionally it can insert the frame alignment sequence (FAS) and the multiframe alignment sequence (MFAS) specified by the ITU G.709 Recommendation [11]. In such case, the framer has the possibility to replace the input FAS and MFAS by locally generated ones. The purpose of this is to correct possible errors introduced by the channel in these sequences. This function is optional. The framer also introduces the FAS and MFAS in test modes where the transceiver transmits framed PRBS. Finally, the framer sorts the data into the four lanes transmitted on the optical fiber; corresponding to the horizontal (H) and vertical (V) polarizations, and for each polarization, the in-phase (I) and quadrature (Q) components. At this point, each of the four lanes is still represented by a 16-bit wide parallel stream, since the clock rate in this part of the egress path is 781.25 MHz. When the PRBS generator is enabled, the data from the host interface is ignored and the egress path data source is the OTU3 framer and PRBS generator.

The egress path also features a PRBS checker that can check sequences generated by the same polynomials of the PRBS generator in the data coming from the host interface.

The line side transmitter includes the ability to adjust the phase relationship of each data output relative to the clock. The delay is controlled through an internal register. The phase is adjustable in steps of 1/128 of a unit interval (UI). Most of the digital logic in the egress path, including the alignment logic in the host interface, the framer, the PRBS generator, the PRBS checker, and the encoder, operates at a 781.25 MHz nominal clock rate using parallel processing.

B. Encoder

QPSK encoding requires only combinatorial logic, and therefore its parallel processing implementation is straightforward. DQPSK encoding can be viewed as a first-order recursive filtering operation, which can be implemented in parallel processing hardware by using the lookahead transformation [12]. The parallelization is more efficiently implemented in the phase domain. The logic equations for the phase are the following:

$$\begin{aligned}\alpha_n &= \alpha_{n-16} + \sum_{k=0}^{15} \Delta\alpha_{n-k} \\ \alpha_{n-1} &= \alpha_{n-16} + \sum_{k=1}^{15} \Delta\alpha_{n-k}, \\ &\cdots \\ \alpha_{n-15} &= \alpha_{n-16} + \Delta\alpha_{n-15}\end{aligned} \tag{14}$$

where α_n is the phase of the transmitted symbol at time n and $\Delta\alpha_n$ is the phase change, which represents the differentially encoded symbol.

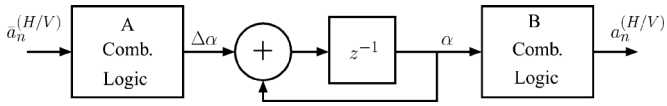

Fig. 4. Differential encoder.

A simplified block diagram (not showing the parallel processing) is shown in Fig. 4. The DBPSK encoding operation is a subset of the DQPSK encoding and it is implemented using the same techniques. The outputs of the QPSK/DQPSK/DBPSK encoder are serialized for transmission at 12.5 Gbaud nominal symbol rate. Serialization is done using four 16:1 analog multiplexers (one per lane). The serial output, after being buffered, drives the external circuitry shown in the top panel of Fig. 3. Please notice that the transceiver output is not filtered in the chip, therefore it is binary in both QPSK and BPSK. As a result, a DAC is not needed in the transmitter (or, equivalently, the line driver can be considered as a 1-bit DAC). The line driver output level can be programmed to 800 $\mathrm{mV_{ppd}}$ or 400 $\mathrm{mV_{ppd}}$.

V. Ingress Path

A. Overview

The analog signal input to the transceiver consists of four channels, corresponding to the in-phase and quadrature components of the two polarizations. These four components are generated by an external optical demodulator, and their amplitudes are adjusted by external variable gain amplifiers (VGA), which are typically part of a TIA chip. The transceiver provides four analog gain control signals which can be used to control the gain of the variable gain amplifiers. The gain control signals are generated by the AGC, which is part of the DSP, and they are converted to analog by four on-chip digital to analog converters (DAC). The four input signal channels are sampled at 25 GHz rate by the track and hold (T/H) circuits and then quantized by the 25 GHz ADCs. The sampling phase of the T/Hs is controlled by four 12.5 GHz phase interpolators, whose input clock is generated by the 12.5 GHz RX CGU and whose digital control is generated by the timing recovery block in the DSP. The timing recovery provides a common digital control word for the four phase channels, but the phase control word can be offset independently for each channel based on a user-provided calibration value whose purpose is to compensate demodulator skews. The digital outputs of the ADCs are retimed and demultiplexed to reduce their rate to 781.25 MHz, and passed to the DSP, where the main receiver functions, such as compensation of chromatic and polarization mode dispersion, timing, and carrier recovery, etc. are carried out. The output of the DSP is the recovered data from the four input channels. However, the DSP does not have information to sort out the data corresponding to each of the four channels. When the data comes formatted in OTU3 frames, the transceiver uses the framing information to identify the four channels and pass them properly sorted to the ingress host interface. This operation is executed by the framer block, described in Section V-D. If framing information is not available, the user must provide control signals to instruct the transceiver on how to do this sorting. Besides the functionality associated to the normal data detection, the ingress path incorporates some auxiliary functions such as pattern generation and checking. The pattern checker is used to check sequences received from the line side, and the generator is used to send test sequences to the host through the host interface.

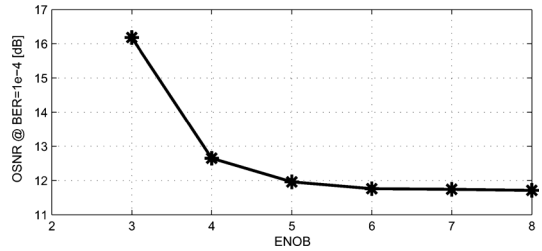

Fig. 5. Simulation of OSNR penalty versus ENOB, for QPSK modulation.

TABLE I
Analog Requirements

T&H and ADC Requirements	
Structure	8-way interleaved/flash
Number of bits (Nominal)	6
Effective number of bits (ENOB)	5.5 bits (min)
Track bandwidth	12GHz (min)
Sampling rate (per interleave)	3.125GHz
Sampling phase error (worst-case difference between latest and earliest sampling instant in the interleaved array)	2ps max
Random jitter of 3.125GHz sampling clocks	1ps rms max
Input Voltage	360 $\mathrm{mV_{ppd}}$

B. ADC

Table I provides a summary of the requirements for the ADC. Fig. 5 shows the OSNR penalty versus ENOB, which justifies the ENOB requirement of Table I. Each channel of the 4-channel ADC consists of 8 interleaved 6-bit flash ADCs. The ADC outputs are retimed, demultiplexed to 781.25 MHz and passed to the DSP. Each ADC is calibrated at startup by its own on-chip $\Sigma\Delta$ DAC (the CalDAC), with the input squelched. Each comparator threshold is set by its dedicated DAC (RefDAC). The CalDAC generates each of 63 desired references in turn, and an on-chip state machine adjusts each RefDAC to match the desired reference. In this way, buffer nonlinearity, gain and offset are calibrated out, as are comparator offsets. The 8 sampling phases for each ADC are generated from a common 12.5 GHz LC VCO which drives 4 phase interpolators (PI), one for each ADC. Their digital control is generated by the timing recovery block in the DSP. The divider generates eight 3.125 GHz 25% duty cycle clocks that drive the sampling switches. A feedback loop between PI output and 8-phase input ensures a 50% duty cycle. Short clock delays allow interleave timing errors of <2 ps with no other correction or calibration. Additional details about the ADC and other analog blocks can be found in [9].

C. DSP

The DSP implements the main receiver functions, such as compensation of chromatic and polarization mode dispersion, timing, and carrier recovery, etc. It uses parallel processing with a parallelization factor of 16, which results in a clock frequency of 781.25 MHz.

TABLE II
IMPLEMENTATION SUMMARY

Block	Paral. Factor	Clock Frequency	Resolution bits (In/Out)	Gates [M]	Power [W]
ADC	8	3.125 GHz	NA / 6	NA	3
Host	16	781.25 MHz	NA	0.224	0.063
Framer	16	781.25 MHz	NA	1.252	0.213
Encoder	16	781.25 MHz	NA	0.010	0.001
FMR	16	781.25 MHz	6 / 6	0.468	0.176
CCR	16	781.25 MHz	6 / 6	0.348	0.096
BCD	128	195.3 MHz	6 / 8	15.92	11.063
FFE	16	781.25 MHz	8 / 9	12.56	6.950
FCR	16	781.25 MHz	9 / 9	1.296	0.717
TR	16	781.25 MHz	8 / 7	0.220	0.088
AGC	16	781.25 MHz	8 / 10	0.080	0.023

1) Fixed Matrix Rotator: This block applies a linear transformation to the input signal vector, which can be described by the following equation:

$$\tilde{\mathbf{r}}_{n,k} = \mathbf{F}\mathbf{s}_{n,k} \tag{15}$$

where

$$\tilde{\mathbf{r}}_{n,k} = \left[\tilde{r}^0_{n,k}\ \tilde{r}^1_{n,k}\ \tilde{r}^2_{n,k}\ \tilde{r}^3_{n,k}\right]^T \tag{16}$$

$$\mathbf{F} = \begin{bmatrix} f^{00} & f^{01} & f^{02} & f^{03} \\ f^{10} & f^{11} & f^{12} & f^{13} \\ f^{20} & f^{21} & f^{22} & f^{23} \\ f^{30} & f^{31} & f^{32} & f^{33} \end{bmatrix} \tag{17}$$

$$\mathbf{s}_{n,k} = \left[s^0_{n,k}\ s^1_{n,k}\ s^2_{n,k}\ s^3_{n,k}\right]^T \tag{18}$$

with f^{mn} being real numbers, while $s^i_{n,k}$ are the samples of the real input signals (13), that is,

$$s^i_{n,k} = s^i(t)\big|_{t=nT+kT/2}, \quad k = 0, 1, \quad i = 0, \ldots, 3. \tag{19}$$

Notice that $s^0(t), \ldots, s^3(t)$ are sampled at twice the symbol rate, or 25 GHz. The transformation (15) is memoryless, in other words, it is applied to the signal on a sample by sample basis, and it does not involve past signal samples. The default value of the transformation matrix is the identity matrix. By overriding the default values of the matrix elements, the user can calibrate errors of the demodulator such as a departure of 90° of the hybrid or other errors caused by imperfect optical components.

2) Bulk Chromatic Dispersion (BCD) Equalizer: The bulk chromatic dispersion (BCD) equalizer can compensate the chromatic dispersion of over 3,500 km of optical fiber. The BCD filter computes the inverse of transfer function (3) using frequency domain filtering. A simplified block diagram is shown in Fig. 6. For each polarization, the input buffer collects blocks of 512 complex samples representing the I and Q components of the input signal, sampled at twice the symbol rate. The overlap and save block filtering method [13] is used. A block of 256 samples is taken every filtering cycle, and it is concatenated with the block of equal size taken in the previous cycle to create the input block of size 512. The filtering cycle consists of 128 symbol periods, corresponding to 8 DSP clock cycles. The startup machine loads the coefficients of the filters during startup phase. Fig. 7 depicts the architecture of the FFT core (the IFFT core is similar). It consists of 9 columns of

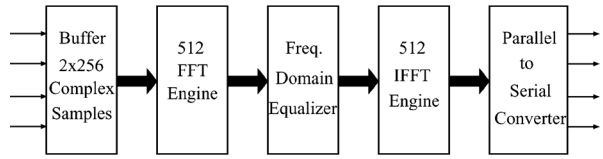

Fig. 6. Block diagram of the BCD equalizer.

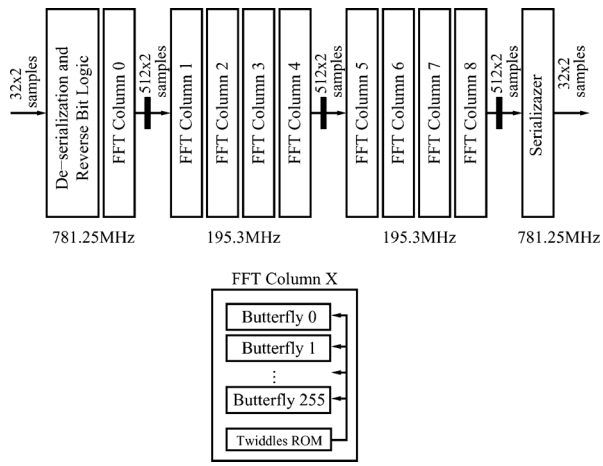

Fig. 7. FFT core architecture.

256 radix-2 butterflies. The main core of the FFT operates at a clock rate four times lower than the rest of the DSP. This reduces power dissipation and eases timing closure. In order to save resources both polarizations are processed using the same hardware, in a systolic fashion. Note the first FFT column (FFT Column 0) is processed by the first stage. This is done in order to improve timing closure in the next stage. While this processing element does not require a full rate clock, the processing is still done fully parallel as the complexity of this column is small enough in comparison with the overhead needed to implement hardware reutilization[1].

The default values of the constants used by the BCD filter to compute its transfer function are based on the assumptions of $\lambda = 1550$ nm, $D = 17$ ps/(nm·km) and $S = 0.09$ ps/(nm^2·km). During the fiber length estimation search, the frequency response of the BCD equalizer is successively computed for all fiber lengths (represented by integer multiples of length quantization step l_{step}) within a certain range, typically between -3500 km and 3500 km (negative fiber lengths are used to represent negative dispersion, such as in dispersion compensation fibers). Once the fiber length has been estimated, the response corresponding to that particular length is saved and the BCD filter is ready for normal operation. The fiber length estimation is controlled automatically by the startup state machine, so the process is transparent to the user.

It is important to observe that LO phase noise is converted to amplitude noise by the BCD equalizer, resulting in a penalty in the presence of CD. The phase noise of the transmit laser does not cause a similar effect because the CD introduced by the fiber is compensated by the BCD equalizer. As a result the phase noise of the transmit laser sees an equivalent channel with no CD.

[1]The reduction in complexity for FFT Column 0 comes from the fact that all its twiddle factors are trivial. For example, there is a ten fold reduction in complexity of FFT Column 0 versus FFT Column 8.

3) Feedforward Equalizer (FFE): The 16-tap $T/2$ multiple-input and multiple-output (MIMO) feedforward equalizer (FFE) performs the polarization demultiplexing and the compensation of PMD and polarization-dependent loss (PDL). The number of taps has been chosen taking into account mainly the possible residual CD at the FFE input. This residual CD can be experienced in applications where the BCD is bypassed[2], as well as caused by inaccuracies of the chromatic dispersion estimation algorithm (e.g., see [14] for more details related to the accuracy of CD estimation techniques). Fast adaptation is essential in optical channels since the receiver must track nonstationary effects (PMD, PDL, changes in the state of polarization of the TX or LO lasers, etc.). A decision-directed least mean squares (LMS) algorithm with no downsampling of the updates is used.

The FFE is a MIMO adaptive transversal filter (see Fig. 8). Let N be the number of the MIMO-FFE taps (in our work, $N = 16$). The input of the MIMO-FFE can be written as a column vector $\mathbf{R}_n$ defined by

$$\mathbf{R}_n = \left[\mathbf{r}_{n,0}\ \mathbf{r}_{n,1}\ \mathbf{r}_{n-1,0}\ \mathbf{r}_{n-1,1}\ \cdots\ \mathbf{r}_{n-\frac{N}{2}+1,1}\right]^T \tag{20}$$

where

$$\mathbf{r}_{n-m,k} = \left[r^0_{n-m,k}\ r^1_{n-m,k}\ r^2_{n-m,k}\ r^3_{n-m,k}\right]^T \tag{21}$$

with $k = 0, 1$ and $m = 0, \cdots, (N/2) - 1$, is the output of the BCD equalizer at instant $(n - m)T + k(T/2)$. Then, the FFE vector output can be expressed as

$$\mathbf{q}_n = \boldsymbol{\mathcal{C}} \times \mathbf{R}_n \tag{22}$$

where

$$\mathbf{q}_n = [\, q^0_n\ q^1_n\ q^2_n\ q^3_n\,]^T \tag{23}$$

$$\boldsymbol{\mathcal{C}} = [\, \mathbf{C}^0\ \mathbf{C}^1\ \cdots \mathbf{C}^{N-1}\,] \tag{24}$$

with

$$\mathbf{C}^l = \begin{bmatrix} c^{00,l} & c^{01,l} & c^{02,l} & c^{03,l} \\ c^{10,l} & c^{11,l} & c^{12,l} & c^{13,l} \\ c^{20,l} & c^{21,l} & c^{22,l} & c^{23,l} \\ c^{30,l} & c^{31,l} & c^{32,l} & c^{33,l} \end{bmatrix}, \quad l = 0, \ldots, N-1. \tag{25}$$

Notice that $\boldsymbol{\mathcal{C}}$ is a $4 \times 4N$ matrix while $\mathbf{R}_n$ is a $4N$-dimensional column vector. Note also that the LMS adaptation scheme adapts each real coefficient $c^{ij,l}$ independently. A common constraint imposed on this type of equalizers consists in treating the 4×4 real coefficient matrix as a 2×2 complex matrix. Not adding constraints such as this or others on the coefficient matrix greatly improves the back to back performance of the receiver. This is owing to the fact that the equalizer performs a more accurate compensation of the optical and analog front end misalignments affecting the in-phase and quadrature components of the signal.

Fig. 9 shows the actual implementation of the parallel MIMO-FFE. The parallelization factor (denoted as P) used in the MIMO-FFE is $P = 16$. Notice that the parallelization factor is defined as the number of symbol periods processed per clock period. In the case of the FFE, the number of input samples processed per clock period is 32, or twice the parallelization factor. Convergence monitoring functions, as well as initialization programmability and override functions are provided. The FFE works at a clock rate of 781.25 MHz.

[2]This mode is used in some applications to minimize power dissipation.

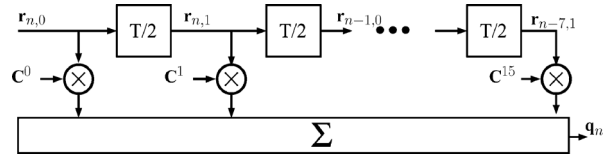

Fig. 8. Feed forward equalizer.

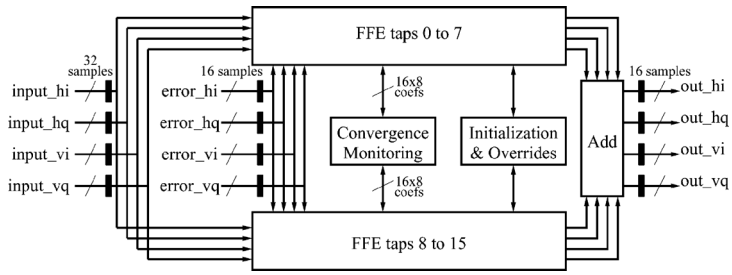

Fig. 9. Feed forward equalizer architecture.

Figs. 10 through 13 show the micro architecture of the FFE. Fig. 10 shows the dot product engine using distributed arithmetic [15], which computes

$$q^{i,l}_n = [c^{i0,l}\ c^{i1,l}\ c^{i2,l}\ c^{i3,l}] \times \left[r^0_{n-m,k}\ r^1_{n-m,k}\ r^2_{n-m,k}\ r^3_{n-m,k}\right]^T, \tag{26}$$

where $i = 0, 1, 2, 3$, $k = 0, 1$, $m = 0, 1, \ldots, (N/2) - 1$, and $l = 2m + k$. Input samples are represented by 6 bits. Fig. 11 depicts a multiplication engine that provides the vector

$$\mathbf{q}^l_n = \left[q^{0,l}_n\ q^{1,l}_n\ q^{2,l}_n\ q^{3,l}_n\right]^T \quad l = 0, \ldots, N-1. \tag{27}$$

Fig. 12 shows a 16-tap processing element of the FFE that provides the equalizer output (22) as follows:

$$\mathbf{q}_n = \sum_{l=0}^{N-1} \mathbf{q}^l_n. \tag{28}$$

Finally, Fig. 13 displays the complete 16-tap, 16-way parallel FFE.

4) Equalizer Adaptation: Initial adaptation of the FFE is done using the blind equalization algorithm known as the constant modulus algorithm (CMA) [16]. Subsequent adaptation is done using a traditional decision directed LMS algorithm [1]. The only change between blind and decision directed adaptation is the way the error is computed.

The four-dimensional column error vector is defined by

$$\mathbf{e}_n = \tilde{\mathbf{a}}_n - \mathbf{q}_n \tag{29}$$

where $\tilde{\mathbf{a}}_n$ is the vector with the components of the rotated decisions provided by the carrier recovery stage. Notice that the carrier recovery is inside the FFE adaptation loop. Therefore phase noise and the phase rotation resulting from the LO offset are compensated and have no detrimental effect on the adaptation.

The LMS adaptation algorithm for the parallel MIMO-FFE is

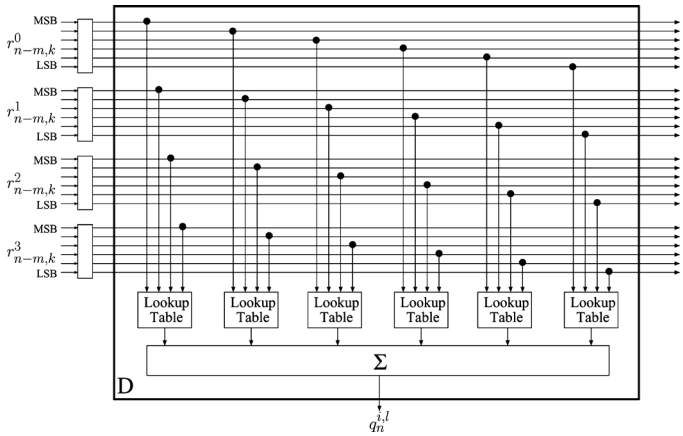

Fig. 10. FFE dot product for a 6 bits resolution input (block "$\mathbf{D}$").

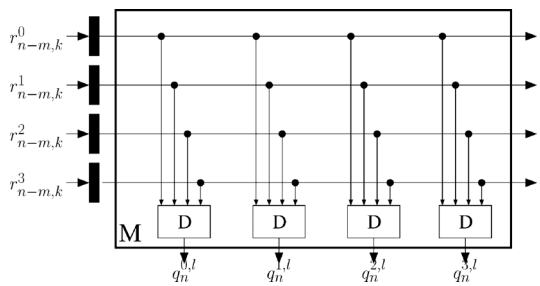

Fig. 11. FFE matrix coefficient multiplication (block "$\mathbf{M}$").

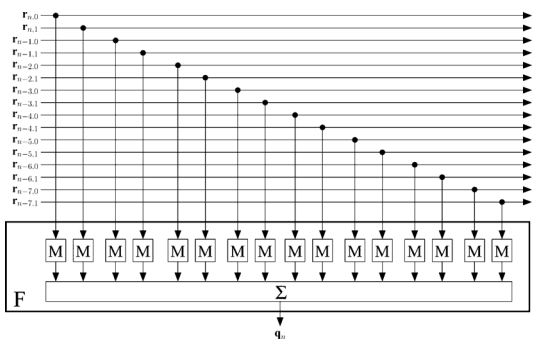

Fig. 12. MIMO FFE architecture with $N = 16$ (block "$\mathbf{F}$").

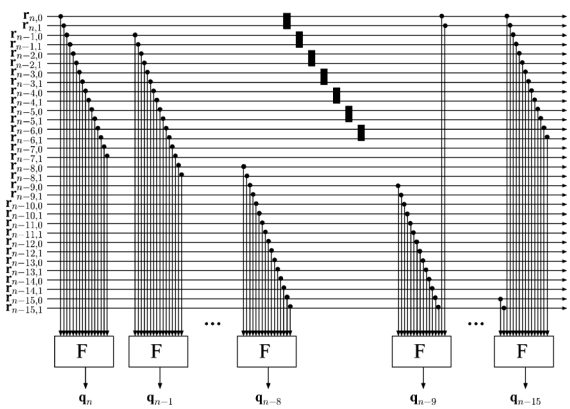

Fig. 13. Parallel implementation of the MIMO FFE with $P = 16$ and $N = 16$.

$$\mathbf{C}_u^l = \mathbf{C}_{u-1}^l + \delta \sum_{p=0}^{P-1} \mathbf{e}_{n-p} \times \mathbf{r}_{n-m-p,k}^T \tag{30}$$

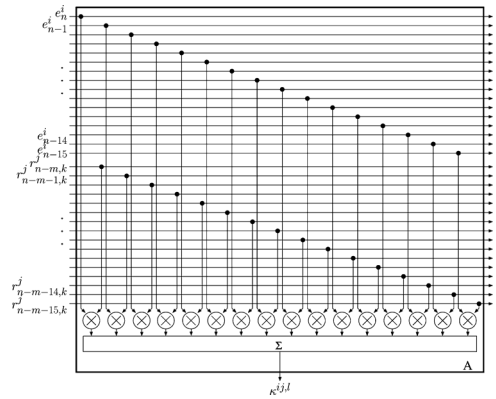

Fig. 14. FFE adaptation initial stage with $P = 16$ (block "$\mathbf{A}$").

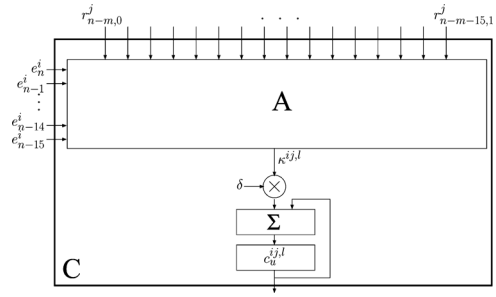

Fig. 15. FFE adaptation engine module (block "$\mathbf{C}$").

where $k = 0, 1$, $m = 0, 1, \ldots, (N/2) - 1$; matrix $\mathbf{C}_u^l$ with $l = 2m + k$ is the lth *matrix-coefficient* of $\boldsymbol{\mathcal{C}}$ (see (24)) at the uth iteration with $u = \lfloor n/P \rfloor$, and δ is the step size [1]. From (30), it is possible to show that each *real* element of the coefficient matrix $\mathbf{C}_u^l$, $l = 0, \cdots, N-1$, is updated by

$$c_u^{ij,l} = c_{u-1}^{ij,l} + \delta \sum_{p=0}^{P-1} e_{n-p}^i r_{n-m-p,k}^j, \quad i, j = 0, \ldots, 3, \tag{31}$$

$m = 0, 1, \ldots, (N/2) - 1$, $k = 0, 1$, and $l = 2m + k$.

Figs. 14 through 17 show the micro architecture of the FFE coefficient update engine. Fig. 14 displays the adaptation dot product engine that implements the summation of P products in (31), that is,

$$\kappa^{ij,l} = \sum_{p=0}^{P-1} e_{n-p}^i r_{n-m-p,k}^j. \tag{32}$$

Fig. 15 shows the adaptation logic for a single coefficient as given in (31) (i.e., $c_u^{ij,l} = c_{u-1}^{ij,l} + \delta\kappa^{ij,l}$), and Fig. 16 depicts the adaptation logic for the complete FFE. Fig. 17 shows the lookup table refresh logic. This logic precomputes the entries of the lookup tables used in the distributed arithmetic [15] implementation of the FIR filter computation, whose main building block is the dot product engine of Fig. 10.

The most important innovations of the equalizer described here are the following:

- Use of four-dimensional real instead of the two-dimensional complex MIMO architecture traditionally used in coherent optical transceivers. The former has the advantage of a substantially better compensation of the optical demodulator impairments.

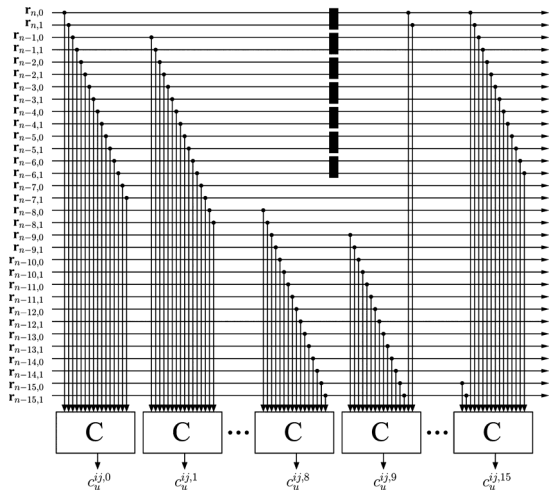

Fig. 16. 16-tap FFE adaptation engine.

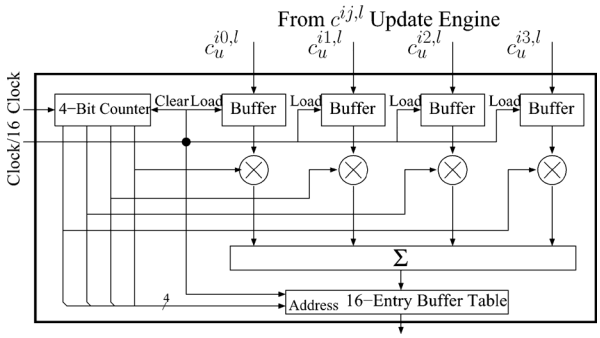

Fig. 17. Lookup table refresh logic for FFE adaptation engine (see [15] for more details on the distributed arithmetic technique).

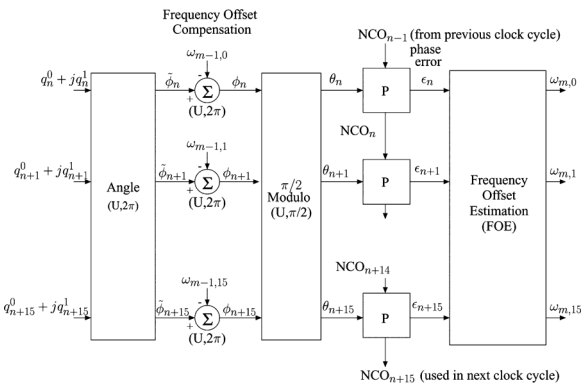

Fig. 18. PLL stage of the FCR. (U,2π) corresponds to unsigned modulus 2π operation (block "**P**" is depicted in Fig. 19).

- Extremely fast adaptation resulting from the use of the entire block of slicer error samples in each cycle of the LMS update and refresh of the coefficients at the full DSP clock rate. This results in optimal tracking of nonstationary effects such as dynamic PMD and rotations of the state of polarization of the lasers.
- In order to achieve high throughput, optimal partioning of the layout is required. Optimal partioning results in a greatly simplified routing, which minimizes critical path delays. Fig. 9 shows the partioning used in this design.

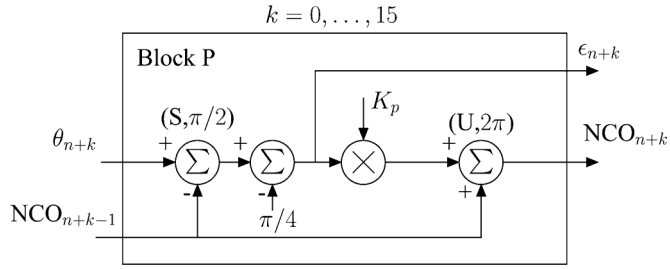

Fig. 19. Serial implementation of a first-order PLL. (S,π/2) corresponds to signed modulus π/2 operation (block "**P**").

- In a highly parallel design as the one described here, very large fanout nodes result in complex routing and difficult timing closure. *Cloning*[3] is used to mitigate this problem.

5) Fine Carrier Recovery (FCR): The FCR is key to the receiver performance. It must be able to track high-frequency laser phase noise, nonlinear phase noise and short-term frequency instabilities of the lasers [17]. Traditional decision-directed phase locked loops outperform Viterbi and Viterbi (V&V) feedforward carrier recovery in some aspects of the operation, such as tracking large amplitude, high frequency sinusoidal carrier jitter. On the other hand, feedforward carrier recovery outperforms the decision directed phase-locked loop (PLL) in random phase noise tracking performance. It has been found that the best solution consists of a first stage of decision-directed carrier recovery, followed by a second stage based on the V&V algorithm. However, a parallel processing implementation of the decision-directed PLL has large latency, which results in limited bandwidth and poor performance.

The latency resulting from parallel-processing would severely limit the bandwidth of the PLL, degrading its phase noise tracking performance and its capture range. Therefore, it is necessary to identify low-latency implementations of decision-directed carrier recovery PLLs.

A first-order PLL is often modeled as a linear filter. This is useful to compute the small-signal transfer function. However, the PLL is actually a nonlinear filter. This precludes the use of traditional unfolding techniques [12], which are applicable only to strictly linear filters, to parallelize the PLL. The approach used in this work to implement a low-latency parallel processing PLL is based on the following: *(i)* implement the PLL in the phase domain, rather than in the complex signal domain; *(ii)* take out of the low-latency loop as much hardware as possible; and *(iii)* use an approximation of the PLL computation to be presented later. A simulation-based comparison between the conventional V&V algorithm and the two stage carrier recovery architecture adopted in current paper (i.e., PLL plus VV) has been investigated by the authors in [18].

Fig. 18 shows a block diagram of the PLL. The frequency offset estimator (FOE) block is used to implement the integral part of the loop filter as usual in a type II second order-PLL. This is based on the fact that the latency in the integral path of a (P+I) loop filter is not as critical as in the proportional loop, therefore its effect on the PLL performance will be negligible. Notice that the techniques *(i)* and *(ii)* above are used in this implementation of the proportional loop. However, a serial implementation

[3]Cloning consists in replicating registers with the same content with the sole propose of reducing fanout. Notice that cloning does not change the logic function implemented.

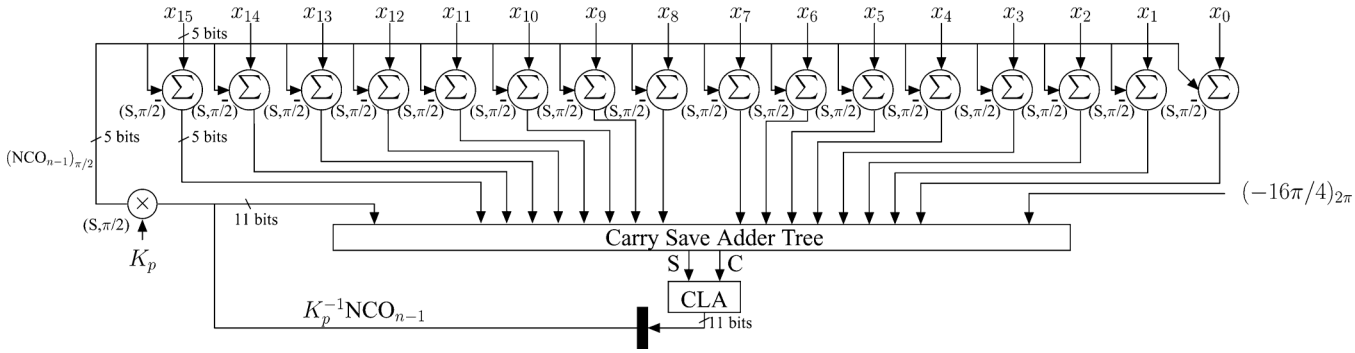

Fig. 21. Instantiation W_{15} of the parallel implementation of the PLL. CLA: carry look-ahead adder.

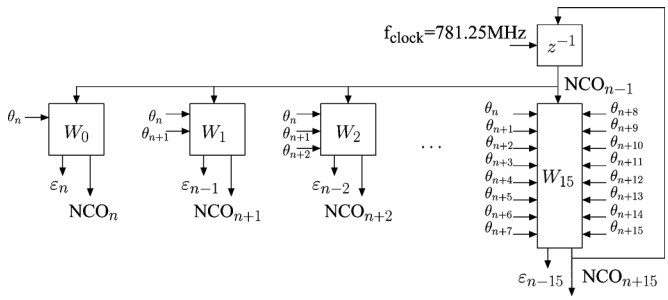

Fig. 20. Parallel implementation of the PLL.

of the PLL is still shown in this diagram for conceptual simplicity. The serial PLL implementation is shown in more detail in Fig. 19. This implementation is not feasible at the required frequency of operation in current technology. The parallel implementation of the PLL, which will be discussed, is based on the following approximation. Let ϕ_n be the phase of sample n at the output of the FFE after the frequency offset compensator, NCO_n the nth output of the numerically controlled oscillator (NCO), and K_p the proportional gain of the PLL. Then the phase error for a QPSK constellation is:

$$\varepsilon_n = (\phi_n - \mathrm{NCO}_{n-1})_{\frac{\pi}{2}} - \frac{\pi}{4} \tag{33}$$

where the notation $(x)_{\pi/2}$ means "x modulo $\pi/2$". Taking into account that $(a-b)_M = ((a)_M - (b)_M)_M$, from (33) we get

$$\begin{aligned}\varepsilon_n &= \left((\phi_n)_{\frac{\pi}{2}} - (\mathrm{NCO}_{n-1})_{\frac{\pi}{2}}\right)_{\frac{\pi}{2}} - \frac{\pi}{4} \\ &= \left(\theta_n - (\mathrm{NCO}_{n-1})_{\frac{\pi}{2}}\right)_{\frac{\pi}{2}} - \frac{\pi}{4}.\end{aligned} \tag{34}$$

The PLL recursion equation is:

$$\mathrm{NCO}_n = \mathrm{NCO}_{n-1} + K_p\left[(\theta_n - (\mathrm{NCO}_{n-1})_{\frac{\pi}{2}})_{\frac{\pi}{2}} - \frac{\pi}{4}\right]. \tag{35}$$

Iterating the recursion, we get:

$$\begin{aligned}\mathrm{NCO}_{n+1} &= \mathrm{NCO}_n + K_p\left[(\theta_{n+1} - (\mathrm{NCO}_n)_{\frac{\pi}{2}})_{\frac{\pi}{2}} - \frac{\pi}{4}\right] \\ &= \mathrm{NCO}_{n-1} + K_p\left[(\theta_n - (\mathrm{NCO}_{n-1})_{\frac{\pi}{2}})_{\frac{\pi}{2}} - \frac{\pi}{4}\right] \\ &\quad + K_p(\theta_{n+1} - (\mathrm{NCO}_{n-1})_{\frac{\pi}{2}} \\ &\quad - K_p\left[(\theta_n - (\mathrm{NCO}_{n-1})_{\frac{\pi}{2}})_{\frac{\pi}{2}} - \frac{\pi}{4}\right])_{\frac{\pi}{2}} - K_p\frac{\pi}{4}.\end{aligned} \tag{36}$$

If K_p is sufficiently small, as happens in most practical situations, the following approximation is valid:

$$\begin{aligned}&K_p\Big(\theta_{n+1} - (\mathrm{NCO}_{n-1})_{\frac{\pi}{2}} \\ &\quad - K_p\left[(\theta_n - (\mathrm{NCO}_{n-1})_{\frac{\pi}{2}})_{\frac{\pi}{2}} - \frac{\pi}{4}\right]\Big)_{\frac{\pi}{2}} \\ &\quad \approx K_p(\theta_{n+1} - (\mathrm{NCO}_{n-1})_{\frac{\pi}{2}})_{\frac{\pi}{2}}\end{aligned} \tag{37}$$

Therefore:

$$\begin{aligned}\mathrm{NCO}_{n+1} \approx \mathrm{NCO}_{n-1} &+ K_p[(\theta_{n+1} - (\mathrm{NCO}_{n-1})_{\frac{\pi}{2}})_{\frac{\pi}{2}} \\ &+ (\theta_n - (\mathrm{NCO}_{n-1})_{\frac{\pi}{2}})_{\frac{\pi}{2}}] - 2K_p\frac{\pi}{4}\end{aligned} \tag{38}$$

and,

$$\begin{aligned}\mathrm{NCO}_{n+k} \approx \mathrm{NCO}_{n-1} &+ K_p\sum_{m=0}^{k}(\theta_{n+m} - (\mathrm{NCO}_{n-1})_{\frac{\pi}{2}})_{\frac{\pi}{2}} \\ &- (k+1)K_p\frac{\pi}{4}.\end{aligned} \tag{39}$$

Fig. 20 shows a fully parallel implementation of the PLL based on approximation (39), and Fig. 21 presents the detail of block W_{15} (blocks W_1 through W_{14} are similar, although simpler). Based on the architecture just described, the low latency parallel implementation of the PLL can be implemented at the DSP clock speed of 781.25 MHz.

A coarse carrier recovery (CCR) preprocessing block expands the capture range to ± 5 GHz. The output of the DSP is the recovered data from the four input channels.

The most important features of the FCR architecture implemented here are the following:

- A novel parallel carrier recovery algorithm is used. This combines a low-latency parallel digital PLL (DPLL) with a traditional feedforward carrier phase recovery algorithm (i.e., VV).
- A new approximation to the DPLL computation is used to enable a parallel-processing implementation.
- The implemented architecture reduces the latency within the feedback loop of the DPLL introduced by parallel processing, while providing a bandwidth and capture range close to those achieved by a serial DPLL.
- The DPLL stage is used to compensate not only frequency offset, but also laser frequency fluctuations, which cannot be efficiently compensated by the VV algorithm.

6) Timing Recovery: Timing recovery (TR) is based on the method described in [19]. In this method the phase error is computed as the difference between the square magnitudes of the (complex) samples of the signal taken at $T/4$ before and after

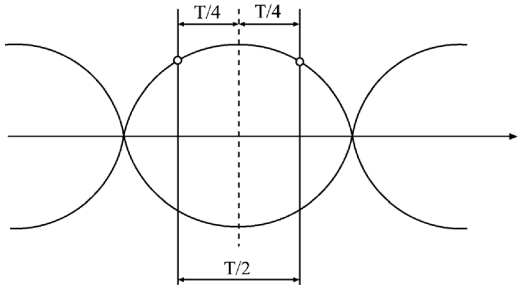

Fig. 22. Phase detector concept [19].

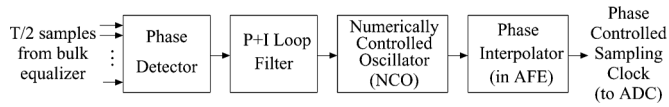

Fig. 23. Timing recovery loop filter.

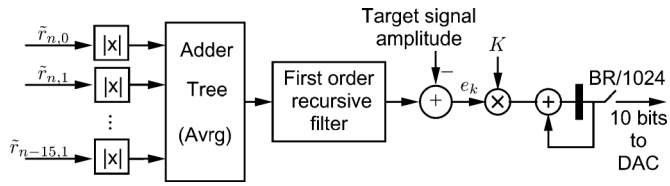

Fig. 24. Block diagram of the AGC.

the center of the eye (Fig. 22). It can be shown that the above computation generates a nearly sinusoidal tone at the difference frequency between the local sampling clock and the clock used in the remote transmitter to transmit symbols. The TR seeks the zero crossings of this sinusoidal tone. The $T/2$ feed forward equalizer that follows interpolates the sample at the center of the eye from the samples at $T/4$ before and after the midpoint of the eye. This method works well in the presence of intersymbol interference. TR is based on a traditional second order loop (Fig. 23). The phase error is processed by a proportional plus integral filter and the output of the filter feeds an NCO. The excellent behavior of the implemented TR algorithm has been recently reported in [20].

7) Automatic Gain Control (AGC): Fig. 24 shows a simplified block diagram of the AGC. The transceiver provides the control signal for an external gain control such as a transimpedance amplifier (TIA) with gain control. The AGC estimates the RMS value of the input signal as a low-pass filtered version of the sum of the absolute values of the samples in the block of 32 $T/2$ samples entering the receiver every cycle of the DSP clock. A first-order low-pass filter is used, with a programmable time constant. The estimate of the RMS value of the signal is compared versus a target, and the difference constitutes the gain error. The gain error is scaled by a gain parameter K and integrated in an accumulator. The output of the integrator is converted to analog using a 10-bit DAC with a 10 MHz sampling rate. The gain values are also available through a serial output port for their use in applications where the gain applied to the input signal is controlled digitally.

D. Framer and Host Interface

The transceiver supports the lane multiplexing and demultiplexing method described by Annex C of the ITU-T G.709 Recommendation [11]. In addition, it supports five custom modes. The framer supports nominal data rates of 50 Gb/s, 25 Gb/s, and 12.5 Gb/s. The lower speed modes result from the use of DBPSK modulation in combination with transmission over either two polarizations or a single polarization. The 25 Gb/s mode may also arise from QPSK or DQPSK transmission over a single polarization. The framer supports these reduced data rate modes. It is assumed that in 50 Gb/s modes, the data coming from or going to the host interface can have one of the following formats: a) According to the OTU3 frame structure, or b) According to a custom defined frame structure, in which case framing at the ingress framer is externally controlled, and a custom mode is used at the egress framer. Frame detection in the egress path is based on the OTU3 framing algorithm (see [11] and [21] for a complete specification of this algorithm). Frame detection is necessary to identify the frame boundaries in the data entering the egress path through the host interface and to apply the Annex C demultiplexing algorithm. The ingress framer must correct for interchange of the two polarization components, skews among the polarizations, phase rotation and phase conjugation. All these effects may occur in the optical channel.

The host interface is a 16-bit wide SFI5.1 interface. Each channel operates at a nominal data rate of 3.125 Gb/s for an aggregate data rate of 50 Gb/s. The data rate of each SFI5.1 channel scales appropriately for other transceiver data rates. There is a 17th channel called the deskew channel, which is used to implement the deskew compensation algorithm. This channel carries out of band data samples organized in a frame structure. Both the egress and the ingress host can be considered as composed of two major blocks, the AFE (not to be confused with the line side AFE) and the digital processing block. To enable the implementation of elaborate logic functions in CMOS technology, in the egress path the data and the deskew channel are demultiplexed by a factor of 4 before being passed to the digital processing block. Therefore processing of the framing and deskew functions in the egress digital processing block takes place at a nominal clock rate of 781.25 MHz. Similarly, in the ingress path the data and deskew channels are processed by the ingress digital processing block at 781.25 MHz and then they are passed to the AFE where they are multiplexed by a factor of 4 and transmitted to the host at 3.125 Gb/s per channel.

E. Startup State Machine

A startup state machine (SSM) controls the operation of the receiver blocks and ensures a proper sequencing of the convergence of the various adaptive blocks. The SSM senses status signals provided by the different blocks and transitions from state to state in response to internal timers or the values of the status signals. The ADC is calibrated upon power up. Inmediately after that, the convergence of the DSP starts. The AGC is converged first followed by the CCR, the FLE, and the BCD equalizer. Since the chromatic dispersion reduces the energy of the timing tone provided by the WDM-TR [19], it must be compensated before timing recovery. Thus, once the chromatic dispersion is compensated by the BCD, the convergence of the TR follows. The rest of the receiver operates synchronously with the symbol rate of the receive signal, therefore it must be converged after timing synchronization. The FFE is trained first in the blind mode and then in decision directed mode. FCR is enabled during final phase of the FFE adaptation. Finally, the framer acquires synchronization.

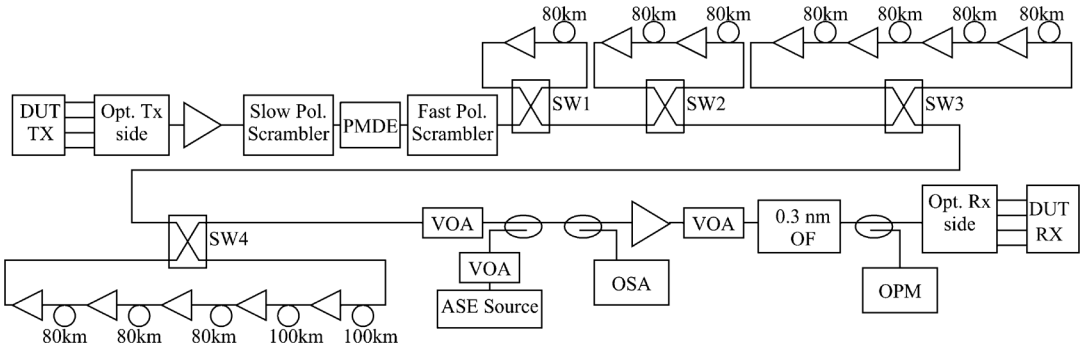

Fig. 25. Device under test (DUT) testbed setup. VOA: variable optical attenuator; OSA: optical spectrum analyzer; PMDE: polarization mode dispersion emulator; OPM: optical power meter; SW: switch.

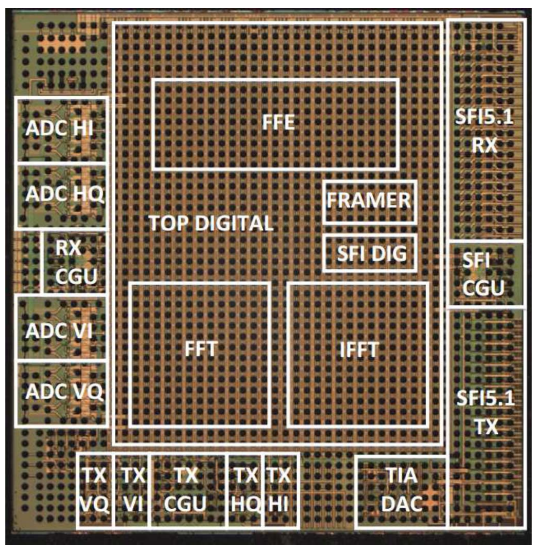

Fig. 26. Chip micrograph.

To enhance testability and facilitate the laboratory characterization of the device, the state machine incorporates functions such as single step, breakpoints, and a stack where up to the 256 most recent SSM states, control, and status signals are stored.

VI. Summary of ADC and DSP Architecture

Table II summarizes parameters of the ADC and DSP architecture discussed throughout this paper. The total gate count is 40 millions, and the power dissipation is 25 W of which the AFE share is 5 W (including transmitter, receiver and host interface analog blocks). The chip is encapsulated in a 27×27 mm, 676 pin BGA package.

Fig. 26 shows a micrograph of the 40 nm CMOS, 75 mm^2 chip.

VII. Experimental Results

Fig. 25 shows the optical setup used in performance measurements. Fig. 27 depicts the OSNR required to achieve a bit error rate (BER) of 10^{-3} versus fiber length for QPSK, DQPSK and DBPSK modulation formats[4]. Chromatic dispersion performance was also tested to the full specification of 55,000 ps/nm (3,500 km of standard fiber) using fiber Bragg gratings. Measured OSNR penalty for this case was 0.5 dB.

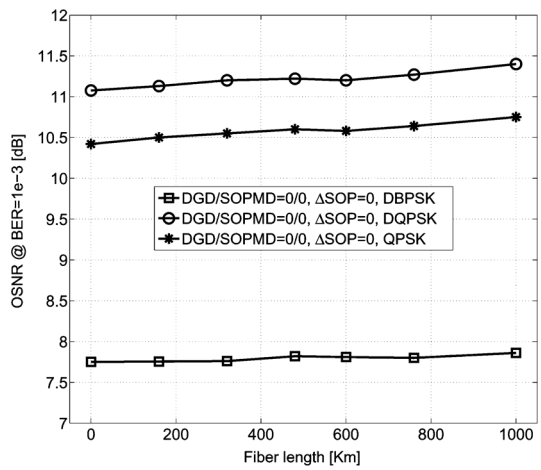

Fig. 27. CD compensation performance measurement results.

Fig. 28 shows the receiver performance in the presence of differential group delay (DGD) for 1000 km of fiber. Performance was tested up to 200 ps of DGD, with no observable degradation. Fig. 29 shows the receiver performance as a function of PMD (SOPMD), where the channel includes 1000 km of fiber and 100 ps of DGD. SOPMD was tested up to 8000 ps^2 with almost no degradation. The range of DGD and SOPMD is twice the previously reported [8], and the OSNR penalty at maximum DGD/SOPMD is negligible (compared to $\sim$1 dB in [8]). Fig. 30 shows the OSNR penalty at $\mathrm{BER} = 10^{-3}$ versus PDL.

Fig. 31 depicts the receiver performance versus the rotational speed of the state of polarization (SOP), for 1000 km of fiber, 100 ps of DGD and 6000 ps^2 of SOPMD. Fig. 32 displays the results for convergence time of the entire receiver. The setup consists of an optically amplified link of 850 km length with an optical switch which cuts the received signal in and out to emulate a protection switching event. The top signal shows the optical switch control, whereas the bottom signal depicts the OTU3

[4]In performance measurements it is customary to specify the required OSNR for certain specific values of BER. Usually these values correspond to the so called *BER threshold* of the various forward error correction codes used in optical communications applications. The BER threshold is defined as the BER at the input of the FEC decoder that results in an output $\mathrm{BER} \leq 10^{-15}$. For example, the *super-FEC* recommended by ITU-975.1 subclause I8 [22] is a non-concatenated RS(2720,2550) code. The BER threshold of this code is 10^{-3}.

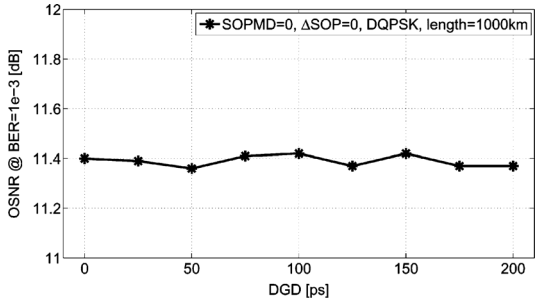

Fig. 28. DGD compensation performance measurement results.

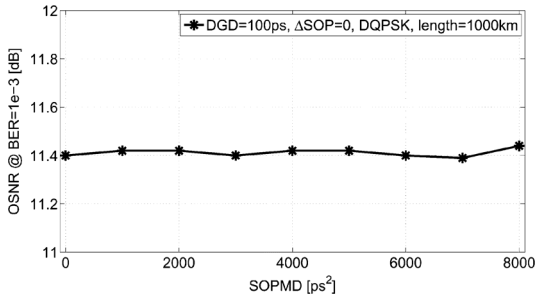

Fig. 29. SOPMD compensation performance measurement results.

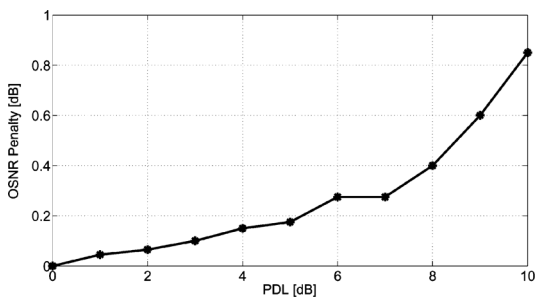

Fig. 30. OSNR penalty at $\mathrm{BER} = 10^{-3}$ versus PDL.

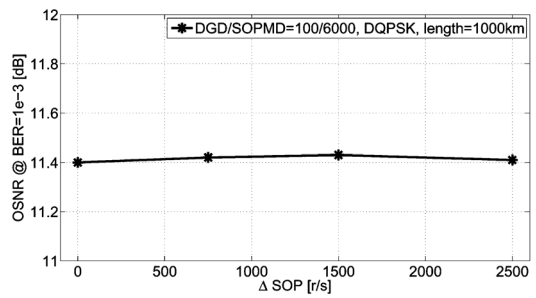

Fig. 31. SOP variation performance measurement results.

alignment status of the receiver. The procedure is repeated 1000 times. As shown in the graph, the total convergence time for the receiver was about 12.6 ms. The block by block breakdown of the convergence time is shown in Table III.

Table IV shows a summary of performance parameters for this work and comparative values from the prior art for the cases where these values were available in the technical literature. The values of Table IV come from [3] and [8].

VIII. Conclusion

The world wide optical communications network is in the middle of a major transition from direct detection and relatively simple modulation schemes such as OOK to coherent detection and high spectral efficiency modulation formats. Coherent demodulation preserves all amplitude, phase and polarization information available in the input optical signal. This information is used by the DSP-based transceiver described in this paper to compensate impairments of the optical channel. In particular, CD and PMD can be completely compensated by the receiver without introducing any penalty. Fast adaptation of the DSP-based equalizer is particularly suited to track the time variations of PMD and other non-stationary effects of the optical channel. It is interesting to observe that direct detection systems can also be equalized by DSP based receivers, but equalization causes noise enhancement and results in a non-zero penalty. This severely limits the reach of these systems, even if they use electronic dispersion compensation.

Other impairments that can be at least partially compensated by the DSP-based coherent receiver are the carrier phase noise introduced by lasers and by cross-phase modulation and self-

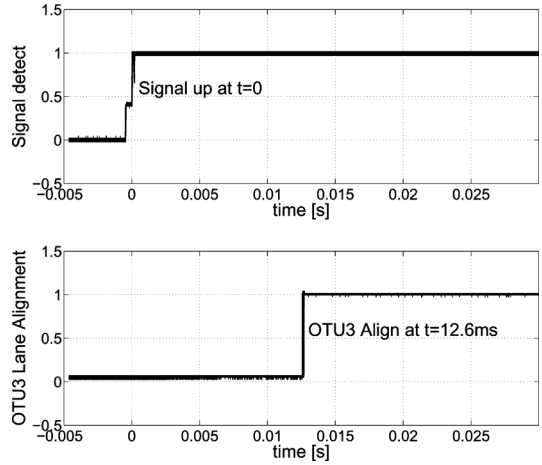

Fig. 32. Optical protection switching performance.

TABLE III
Approximate Convergence Times for Different Blocks During Signal Acquisition

Block	Time to convergence [ms]
AGC	2.5
CCR	0.05
BCD	4
FFE	6

TABLE IV
Performance Comparison With Prior Art

Condition	Prior Art (46Gb/s) Penalty in dB	This Work (50Gb/s) Penalty in dB
CD=55,000ps/nm	0.5 [3]	0.5
DGD=100ps	0.4 [8]	<0.1
DGD=200ps	N/A	<0.1
SOPMD=4000ps2	0.5 [8]	<0.1
SOPMD=8000ps2	N/A	<0.1
PDL=4dB	N/A	<0.2
PDL=8dB	N/A	0.5
SOP Rotation=50kHz	N/A	0.3
Combination (*)	N/A	0.6

(*) The *Combination* case corresponds to CD=56,862 ps/nm, DGD=70ps, SOPMD=3000ps2 and rotational speed of the SOP of 300rad/sec.

phase modulation, random rotations of the state of polarization of the transmit or LO lasers, timing jitter, etc.

Coherent technology will continue to experience fast progress in the future. Major improvements in speed, spectral efficiency, level of integration and power efficiency of CMOS DSP-based transceivers are expected.

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Hugo S. Carrer, photograph and biography not available at the time of publication.

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