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Non-linearities modelling and post-compensation in continuous-time ΣΔ modulators

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Abstract: The authors present a post-compensation technique for continuous-time (CT) ΣΔ modulators based on efficient finite-order Volterra models. At first, the authors develop a behavioural model for a CT sigma–delta modulator (SDM). This model includes non-linear and non-ideal behaviour and leads to a finite Volterra representation of the SDM. Then, they derive and discuss two novel compensation blocks that are special cases of Volterra models. These models, a memory polynomial (MP) and a modified generalised memory polynomial (MGMP), can be interpreted as generalisations of classical block-based non-linear models, like Hammerstein and Wiener systems, respectively. The authors show that the MGMP compensator offers a better distortion cancellation because of the inclusion of cross-terms at the output of the model, at the price of increasing complexity. Simulation results, based on a transistor level circuit model for the SDM, show a good agreement between the SDM and the developed models. In addition, the authors also verify good performance of the proposed compensators.

1 Introduction

Recently, the need for high-resolution analogue-to-digital converters (ADCs) with low power consumption, especially for mobile applications, has drawn much attention towards sigma–delta architectures for signal conversion. Such devices combine low-resolution quantisation with oversampling and noise shaping in order to reduce the in-band noise and thus increase the dynamic range. In particular, continuous-time (CT) sigma–delta modulators (SDMs) seem to be an attractive choice because of their inherent anti-aliasing properties and low circuit complexity, among other advantages [1]. Sigma–delta structures have been proposed for many applications, including DVB-T (digital video broadcasting-terrestrial) [2–4] and bluetooth [5]. In addition, they provide a flexible choice between resolution and bandwith, which makes them suitable for multi-standard transceiver architectures combining for example global system for mobile communications (GSM)/wireless local area network (WLAN)/bluetooth [6, 7].

Despite of the attractive properties, circuit non-ideal behaviour degrades the overall performance resulting in harmonic distortion and increased in-band noise, which reduces the effective number of bits in the converter. A possible solution to reduce this distortion is the use of model-based digital post-compensation techniques. These techniques are generally based on application of another distortion to the digital output of the converter that would cancel out the original distortions present in the device output [8, 9], and they involve two steps. First, the post-compensator is trained (off-line) using measurement data from the CT SDM; then, it is on-line implemented at the output of the converter. This methodology involves some extra digital processing, that is a few multiplications and additions in the digital domain to obtain the corrected output sample.

In order to obtain an adequate structure for the compensator it is first necessary to understand the non-ideal behaviour of CT SDMs. Several partial studies have been performed in the literature. For example, the issue of the non-linearity in the integrator is considered in [10–12] modelling the quantiser effects as an additive noise source. In [11, 12] a Volterra model is developed following the additive noise assumption for SDMs with multibit quantisation. In other line, in [13] the non-ideal effects on the digital-to-analogue converter (DAC) are addressed and in [14] a new interpretation on the quantiser effects is discussed. However, none of the mentioned works offer a complete description of the SDM including all these effects jointly.

In this work, we propose efficient finite Volterra-based post-compensation schemes for this type of converters in order to maintain a low complexity for the necessary on-line processing. In order to achieve this, we first develop a behavioural model for such devices by studying the different elements composing the modulator and considering all their effects on the system. Since the behavioural model represents in general weak non-linearities, it is possible to consider a finite Volterra model to capture all the mentioned characteristics. This Volterra model allows to design and use a post-compensation model and the corresponding parameter estimation techniques.

The present work is organised as follows. In Section 2, a novel behavioural model for an SDM is introduced. Then, efficient finite Volterra models for the system and the novel post-compensator schemes are described in Sections 3 and 4, respectively. Simulation results are presented in Section 5. Finally, conclusions are discussed in Section 6.

2 Behavioural SDM model

The general hypothesis behind a post-compensation strategy using a finite Volterra model considers that the SDM behaviour is well described by a weak non-linear system. In this section we study the non-linear effects present in an SDM in order to test the validity of this hypothesis. We start from the ideal SDM shown in Fig. 1 consisting of three blocks (integrator, quantiser and digital-to-analogue converter) connected in a feedback loop. In the following subsections we consider a model for each block introducing the real effects that preclude SDM ideal behaviour, with the aim of finding an equivalent block oriented model, illustrated in Fig. 2, that represents the non-ideal SDM. In the diagram $P(\cdot)$ and $N(\cdot)$ represent weak static non-linearities and $I(s)$ and $H(s)$ represent linear [finite impulse response (FIR)] dynamic blocks.

2.1 Integrator non-linearities

One of the main factors that limit the maximum achievable signal to noise ratio (SNR) in a sigma–delta analogue-to-digital converter (SDC) is the non-linearity in the integrator [10]. This performance degradation is most significant in the case of CT SDCs, as switched capacitor circuits suffer from effects such as capacitor mismatch and switch non-ideal behaviour.

The linearity of the integrator is limited by the effect of the non-linear trans-conductance of the operational amplifier which appears in the output integrator current [11]. From this point of view, CT integrators can be approximated as a cascade of a static non-linear operator and an ideal integrator device [10]. In the case of fully differential architectures, which is usually used for amplifiers to implement the integrator, the even terms can be neglected because of the common mode rejection ratio. Assuming this structure here, the non-linear operator will contain only odd terms [11, 12].

In general, it can be assumed that a third-order non-linearity is sufficient to capture the main non-linear effects

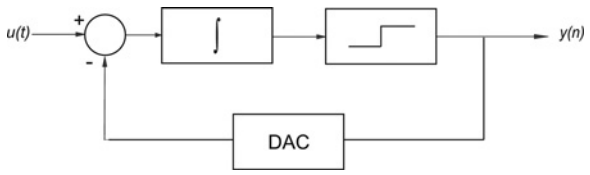

Fig. 1 *Block diagram of an ideal CT SDM*

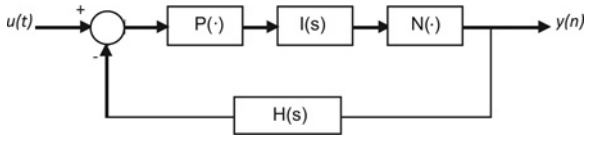

Fig. 2 *Equivalent block diagram of a CT SDM replacing all elements with their corresponding models*

in the integrator [11, 12]. Thus, we can assume that the static non-linear operator is given by

$$f(x) = ax - bx^3 \tag{1}$$

where x is the input signal to the integator, and a and b are constants depending on the trans-conductance of the transistors used in the integrator. A block diagram of the CT SDM, including the non-ideal integrator, could be obtained replacing $P(\cdot)$ by $f(x)$ in Fig. 2. The derivation of (1), for different integrator architectures, can be found in [12].

2.2 Model for non-ideal behaviour of the feedback DAC

Any first-order binary SDC architecture includes a single bit DAC in the feedback loop. This device introduces non-ideal effects that have to be taken into account when a precise model is required. In order to analyse these effects, we present a model based on the results presented in [13].

Given a differential binary signal $y(n)$ at the input of a single-bit DAC, we can define its output as

$$y(t) = \sum_{n=-\infty}^{\infty} y_0(n)h(t - nT) \tag{2}$$

where T is the clock period, $y_0(n)$ is defined as

$$y_0(n) = \begin{cases} +V_{\text{ref}} & \text{if } y(n) \geq 0 \\ -V_{\text{ref}} & \text{if } y(n) < 0 \end{cases} \tag{3}$$

with V_{ref} as the reference voltage for the DAC, and

$$h(t) = \begin{cases} 1 & \text{if } 0 < t < T \\ 0 & \text{otherwise} \end{cases} \tag{4}$$

is an ideal sample and holds device for the DAC.

This model can be modified to include the additional effects that exist in real circuits, such as propagation delays and non-instantaneous swing between positive and negative reference voltages. To that purpose, the function $h(t)$ in (4) can be replaced by a first-order filter response, generating an exponential voltage settling at the output of the DAC, that is

$$h(t) = 1 - \mathrm{e}^{-t/\tau} \tag{5}$$

which has the following Laplace transform

$$H(s) = \frac{1}{1 + s\tau} \tag{6}$$

where τ is the time constant of the circuit, determined by the slew rate of the transistors that limits the time response of the DAC. Note that the actual response of the DAC is still linear.

2.3 Linearisation of the quantiser

In a single-bit first-order CT SDM, the one-bit quantiser (usually a comparator) can be modelled using the sign function, which is strongly non-linear. However, as will be discussed in this section, the noise shaping of the quantisation noise and the feedback nature of the SDM linearise the quantiser in the signal bandwidth [14]. In fact,

little quantisation noise occurs in the signal band, and out-of-band quantisation noise is filtered out by the decimation filter.

The non-linearity of a static transfer function can be drastically reduced using an additive dither signal (in the field of signal processing, a dither signal is a pseudo-random noise added at the input of an ADC in order to de-correlate the quantisation noise from the analogue input signal to it [1]. On the other side, the same technique is used in control of non-linear systems but the objective is different. In this case, a high-frequency sinusoidal signal is used to change the behaviour of a non-linearity in such a way that an averaging effect takes place. This is due to the convolution between the non-linearity and the amplitude distribution of the sinusoidal signal [15]. It can be shown that the non-linear element, usually a strong or discontinuous non-linearity, behaves as a smoother non-linear element in the lower frequency range. In this section, we use the second interpretation of dithering) at the input of the non-linear element [14]. For this purpose, the dithering signal must satisfy the condition of having a fundamental frequency much higher than the input signal bandwidth. However, in the case of discrete time non-linear systems, the output contains sub-harmonics of the dither signal that can overlap in the signal band. This effect is called noise injection of the dither signal [14].

In open loop, the dither signal effect is such that the quantiser is less non-linear in the input signal bandwidth. If the dither signal is a sinusoid of amplitude A_{d}, and its frequency is much higher than the input signal bandwidth, then the output signal (after a low-pass filter) can be written as [14]

$$y_{\mathrm{lp}} = \frac{2}{\pi}\sin^{-1}\left(\frac{x}{A_{\mathrm{d}}}\right) \simeq \frac{2}{\pi A_{\mathrm{d}}}x, \quad x \ll A_{\mathrm{d}} \tag{7}$$

Therefore the dither signal linearises the quantiser in the signal bandwidth. If the noise injection of the dither signal is negligible, then this model is an open-loop equivalent to a single-bit SDM. Owing to the feedback structure, the noise injection can be further reduced by means of a high gain loop filter at the signal bandwidth. The integrator in the direct signal path of an SDM fits such description.

In order to generate a dither signal, an oscillator consisting of a high dynamic gain followed by a static non-linear element is needed. That is the case of the integrator followed by a comparator in a single-bit CT SDM. Hence, in an SDM, the quantiser input contains a dithering signal. As a general conclusion, the quantiser model can be well described by a weakly static non-linear system. Hence, if $x(t)$ is the input to the comparator, we can model its output with an pth-order polynomial

$$b[x(t)] = x(t) + k_1 x^2(t) + \cdots + k_{p-1}x^p(t) \tag{8}$$

where the k_i $(i = 1, \ldots, p-1)$ are the polynomial coefficients. As suggested by (7), the output of the comparator is almost linear, and then $p \leq 3$ should suffice.

In the case of a SDM with a multibit quantiser, the usual assumption is that the multibit ADC in the forward path can be replaced by an additive noise source [1, 11, 12]. This noise source is assumed to be white with uniform distribution on the interval $-$LSB/2 to $+$LSB/2, where LSB is the quantisation step. However, this is still an approximation for high-resolution ADCs. If we consider a low-resolution multibit quantiser, that is up to 4 bits (which is usually the case in SDMs), then another approach should be considered.

Let us consider an SDM with a multibit quantiser. Hence, assuming a flash (for example, a flash ADC is a natural choice because of the high sampling rate of the system and the low-resolution required [16]) B-bit quantiser with thermometric coding, the output of the multibit DAC at the feedback branch can be written as

$$y(t) = b_0(t) + b_1(t) + \cdots + b_B(t) \tag{9}$$

where b_i is the ith bit corresponding to the output of comparator i, with different reference voltages for each $i = 1, 2, \ldots, B$. Since a single-bit quantiser in an SDM is linearised in the band of interest (and therefore it can be modelled with a weakly static non-linearity), each bit b_i in (9) can be represented arbitrarily well with a polynomial such as the one represented in (8). Then, $y(t)$ can be represented as a sum of polynomials, which in turn is a polynomial as well. Therefore the multibit quantiser can also be modelled as a weakly static non-linear system.

2.4 Complete behavioural model

The integrator in the SDM, as discussed in Section 2.1, can be replaced by a third-order polynomial $P(\cdot)$ followed by an ideal integrator [i.e. a linear filter $I(s)$]. Also, the DAC in the feedback loop (Section 2.2) can be represented by a filtered version of the output signal $y(t)$ through a linear filter $H(s)$. In addition, the quantiser can be considered almost linear in the signal bandwidth, and so we can model it with a weak static non-linearity $N(\cdot)$ (Section 2.3).

Hence, the inclusion of non-ideal effects in the block diagram of Fig. 1 leads to the complete behavioural model depicted in Fig. 2. Note that aging and temperature dependencies are not considered at the moment such that the parameters of the SDC remain constant. Based on the behavioural model we consider the design of efficient non-linearities post-compensation techniques in next sections.

3 Volterra model of a CT SDC

It is well-known that systems presenting weak non-linearities, as the one described in Fig. 2, allow for a Volterra representation. Moreover, discrete-time systems with fading memory can be approximated arbitrarily well by a discrete-time Volterra model (DTVM), if adequate orders are chosen [17–19]. In general, the output of a DTVM, at instant k, can be expressed as [18]

$$y(k) = \Phi(y(k-1), \ldots, y(k-p), u(k-1), \ldots, u(k-q)) \tag{10}$$

where the choice of the function $\Phi(\cdot)$ and the parameters p and q define the model.

In the case of the system depicted in Fig. 2, an equivalent Volterra representation can be formulated as follows. First, we consider that the CT SDC can be approximated arbitrarily well by a discrete-time system with a sufficiently high sampling rate. In fact, this is the case of interest since the signals are sampled at the comparator with a relatively high over-sampling ratio (OSR). Then, we assume, without loss of generality, that $I(s)$ and $H(s)$ are linear systems with finite memory. This is justified, because the output of physical systems does not depend on the infinitely remote

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past. Thus, we consider a length M_I for $I(s)$ and a memory of M_H for $H(s)$.

Also, it is possible to assume that signal components that have already passed through the feedback path will not re-enter the loop (a similar approach was used in [14] to model the dynamic nonlinearities in a radio frequency power amplifier). This assumption is based on two facts. On the one hand, the non-linearity $P(\cdot)$ will mix up some of these components to higher frequencies out of the band of interest. On the other hand, the remaining components would be so far away in the past that their effect can be considered negligible on the present output $y(n)$. Therefore the system will also have a finite memory M such that $M \cong M_I + M_H$. This is confirmed by the fact that the output of real physical systems do not depend on the infinitely remote past and so fading memory can be assumed. On the other hand, the non-linear effects of the system are frequency dependent and vanish when the excitation is removed.

Since that this system present finite memory, we choose $p = 0$ in (10), that is, non-linear FIR systems and focusing on the family of analytic continuous functions $\Phi(\cdot)$ (which can be expanded into Taylor series), it is possible to define DTVMs analogous to the CT Volterra models. In such a case, the integrals are replaced by discrete convolution sums and the system response becomes

$$y(k) = y_1(k) + y_2(k) + y_3(k) + \cdots \tag{11}$$

where the first term, given by

$$y_1(k) = \sum_{i=0}^{\infty} \alpha_1(i)u(k-i) \tag{12}$$

corresponds to the linear convolution model, and the higher-order terms can be written as

$$y_2(k) = \sum_{i=0}^{\infty}\sum_{j=0}^{\infty} \alpha_2(i,j)u(k-i)u(k-j) \tag{13}$$

$$y_3(k) = \sum_{i=0}^{\infty}\sum_{j=0}^{\infty}\sum_{l=0}^{\infty} \alpha_3(i,j,l)u(k-i)u(k-j)u(k-l) \tag{14}$$

and so on.

Furthermore, any non-linear function can be approximated by a polynomial of sufficiently high-order giving rise finite DTVMs, which are the simplest among all Volterra models. Finite DTVMs are composed of a moving average linear model of order M and a polynomial non-linearity of degree N. For the SISO case, the input–output relationship of such systems is given by

$$y(k) = y_0 + \sum_{n=1}^{N} v_M^n(k) \tag{15}$$

where

$$v_M^n(k) = \sum_{i_1=0}^{M} \cdots \sum_{i_n=0}^{M} \alpha_n(i_1, \ldots, i_n)u(k-i_1)\cdots u(k-i_n) \tag{16}$$

At this point, we can extract further information about the Volterra representation of the SDM structure in Fig. 2. As previously mentioned, the linear filter in the feedback path generates cross-terms of the input signal to the output. Also, the feedback system with Hammerstein–Wiener model in the forward path suggests that a more general model than Hammerstein–Wiener is needed to represent the SDM. Finally, there are two different linear filters, that is $I(s)$ and $H(s)$, so a model with at least two linear dynamics is be required.

4 Post-compensation of SDM

The post-compensation scheme proposed in this work is illustrated in Fig. 3, where the SDM block represents the real device under test (DUT) and the ideal SDM is the one represented by Fig. 1. The signal $u(t)$ feeds both, the ideal SDM and the DUT, and the output $y(n)$ of the real device is applied to the input of the post-compensator. Then, the post-compensator is a system such that its output $\hat{y}_I(n)$ minimises the error $e(n)$ for a certain criterion when compared to the output of the ideal SDM. From this point of view, the compensator should include information of the inverse of the SDM and of the ideal SDM.

The signal $y_I(n)$ from Fig. 3 must be known a priori in order to train the post-compensator. This information could be obtained by simulation of an ideal SDM. Nevertheless, it is also possible to generate it directly with a digital signal generator, and apply it to the DUT input after a high-quality DAC as shown in Fig. 4. This procedure can be easily carried out in a practical implementation, and allows for periodical training if needed. Both approaches are equivalent and have been widely used for ADC error correction [20, 21].

Since the DUT can be approximated by the real SDM of Fig. 2, it can be represented by a Volterra model (as discussed in Section 3). Now, it is known that it can also be p-linearised with a Volterra system of similar complexity [17]. From the analysis of Section 3, we know that the Volterra representation for the SDM is more general than a Hammerstein or a Wiener model. We also know that more than one linear dynamic is needed to represent it. Thus, the choice of a model for the compensator should be more complex than Hammerstein or Wiener models.

Our first approach is to examine the performance of a memory polynomial (MP) model for the compensator, as the illustrated in Fig. 5. This model is a generalisation of a Hammerstein system [22], where multiple linear filters are allowed after the static non-linearity. Assuming an Nth-order polynomial and an FIR filter of length M, the

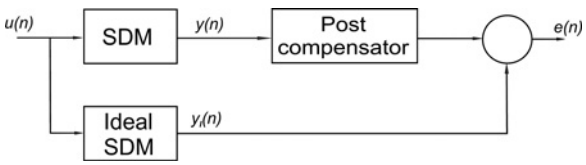

Fig. 3 *Post-compensation scheme*

Fig. 4 *Ideal signal generation*

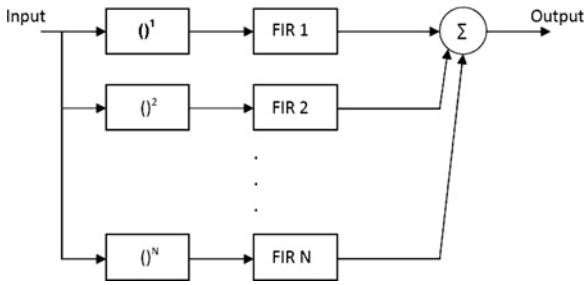

Fig. 5 *Nth-order MP*

compensator output is given by

$$\hat{y}_I^{\mathrm{MP}}(k) = \sum_{n=1}^{N}\left(\sum_{m=0}^{M-1}\alpha_{nm}y^n(k-m)\right) \tag{17}$$

where $y(k)$ is the output of the SDC, $\hat{y}_I^{\mathrm{MP}}$ is the output of the compesator and α_{nm} are the parameters of the compensator. This structure has the advantage that the output signal is linear in the unknown parameters (i.e. the terms α_{nm}), which renders efficient parameter estimation possible through least-squares methods [23].

As an alternative to the MP model, we introduce a modified generalised memory polynomial (MGMP). It can be shown that in this case, the input–output relationship of the model is

$$\hat{y}_I^{\mathrm{MGMP}}(k) = \sum_{n=1}^{N}\left(\sum_{m=0}^{M-1}\alpha_{nm}y(k-m)\right)^n \tag{18}$$

This model is the transposed of the block diagram shown in Fig. 5, with the power terms after the FIR filter in each parallel branch. Note that this model includes cross-terms among the samples $y(k-m)$. This is clear from the fact that for a given n, the power terms in brackets at the left-hand side of (18) can be posed as

$$\left(\sum_{m=0}^{M-1}\alpha_{nm}y(k-m)\right)^n \propto \sum_{m_1=0}^{M-1}\sum_{m_2=m_1}^{M-1}\cdots \sum_{m_n=m_{n-1}}^{M-1}\alpha_{nm_1}\cdots\alpha_{nm_n}y(k-m_1)\cdots y(k-m_n) \tag{19}$$

Both MP and MGMP models are special cases of finite Volterra models [18, 22]. The model described by (18) is a generalisation of a Wiener model different to the GMP derived in [22]. Note that the MGMP model includes cross-terms at the output in the same way as the Volterra model for the real SDM. Thus, MGMP model is expected to outperform the MP as compensator. Expression (18) can also be represented in matrix form and the parameters can be jointly estimated by least squares (LS) in a similar way to that of [24] for a Wiener model. However, an over-parametrisation is needed to force linearity in the unknown parameters and solve equations in matrix form.

4.1 Parameter estimation of the compensators

Once the model structure has been chosen, the issue of parameter estimation arises. The values of the model parameters must be estimated in such a way that a given error criterion is minimised.

We can distinguish two phases of operation for each kind of compensator block. The first one is the 'training mode', in which the parameters of the model are estimated by minimisation of the error between its output and a reference value (as shown in Fig. 4). The second is the "running mode", where the chosen parameters are used to predict the desired output of the model.

Let us define the reference value $y_I(k)$, which is the desired output of the compesator. This reference value is generated separately by simulation of an ideal SDM, using the test input signal $u(t)$ (Fig. 3) and written in vectorial form as

$$\boldsymbol{y}_I = [y_I(M+1)\,y_I(M+2)\,\cdots\,y_I(L)]^{\mathrm{T}} \tag{20}$$

where L data points will be used for the training.

In general, the output of the compensator can be written as

$$\hat{\boldsymbol{y}}_I = \boldsymbol{Y}_\phi\boldsymbol{\phi} \tag{21}$$

where $\boldsymbol{Y}_\phi$ is the matrix of observation data for a sequence of L data points

$$\boldsymbol{Y}_\phi = [\boldsymbol{y}_\phi(M+1)\,\boldsymbol{y}_\phi(M+2)\cdots\boldsymbol{y}_\phi(L)]^{\mathrm{T}} \tag{22}$$

composed by the regressor vectors, and

$$\boldsymbol{\phi} = [\boldsymbol{\phi}_1^{\mathrm{T}}\,\boldsymbol{\phi}_2^{\mathrm{T}}\cdots\boldsymbol{\phi}_N^{\mathrm{T}}]^{\mathrm{T}} \tag{23}$$

are the vector of parameters to be estimated.

The regressor and the parameter vectors are a function of the output of the DUT ($y(k)$) when it is excited by the input $u(t)$ and depend on the structure of the model. For the MP model

$$\boldsymbol{y}_\phi(k) = [y(k)\,y(k-1)\cdots y(k-M)\cdots y^N(k-M-1)]^{\mathrm{T}} \tag{24}$$

and

$$\boldsymbol{\phi}_n = [\hat{\alpha}_{n0}\,\hat{\alpha}_{n1}\cdots\hat{\alpha}_{nM}]^{\mathrm{T}} \tag{25}$$

For the MGMP model, considering different parameters for each product of original parameters (α_{ni}) for $n = 1, 2, \ldots, N$ and $i = 0, 1, \ldots, M$, the over-parameterised vectors can be defined as

$$\boldsymbol{y}_\phi(k) = [y(k)\cdots y(k-M-1)\,y^2(k)\,y(k)y(k-1)\,\cdots\,y^2(k-M-1)\,y^2(k)y(k-1)\cdots y^N(k-M-1)]^{\mathrm{T}} \tag{26}$$

and

$$\boldsymbol{\phi}_n = [\alpha_{n0}^n\,\alpha_{n0}^{n-1}\alpha_{n1}\cdots\alpha_{n0}\alpha_{n1}\cdots\alpha_{nn}\cdots\alpha_{nM}^n]^{\mathrm{T}} \tag{27}$$

Then, in the training phase the parameters can be estimated through LS, that is, minimising the squared error defined as

$$\hat{\phi} = \arg\min_{\phi}\,\boldsymbol{e}^{\mathrm{T}}\boldsymbol{e} = \arg\min_{\phi}(\boldsymbol{y_I} - \boldsymbol{Y}_{\phi\hat{\phi}})^{\mathrm{T}}(\boldsymbol{y}_I - \boldsymbol{Y}_\phi\hat{\phi}) \tag{28}$$

where the solution is given as

$$\hat{\boldsymbol{\phi}} = (\boldsymbol{Y}_\phi^{\mathrm{T}}\boldsymbol{Y}_\phi)^{-1}\boldsymbol{Y}_\phi^{\mathrm{T}}\boldsymbol{y}_I \tag{29}$$

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In order to ensure the invertibility of the term $\boldsymbol{Y}_{\phi}^{\mathrm{T}}\boldsymbol{Y}_{\phi}$ the condition of persistent excitation should be satisfied.

In the running phase, the predicted output is

$$\hat{\boldsymbol{y}}_{\boldsymbol{I}} = \boldsymbol{Y}_{\boldsymbol{\phi}}\hat{\boldsymbol{\phi}} \tag{30}$$

In the case of MGMP, the vector of parameters involves $\sum_{n=1}^{N} M^n$ terms. However, note that the permutations of the cross-terms products have the same values. Thus, they can be grouped without loss of generality as suggested in (19) by the sums indexes. This reduces the amount of parameters to $\sum_{n=1}^{N}(M+n)!/(M!n!)$, although it is still higher than the amount required for the MP (which is MN).

From (27), we see that there are elements in each ϕ_n such that $\phi_n(j) = (\alpha_{ni})^n$. Thus, the parameters α_{ni} can be extracted from $\hat{\phi}$ as follows. ϕ_1 are the coefficients for the first filter. In general, for $n = 2, \ldots, N$ and $i = 0, \ldots, M-1$, we can obtain α_{ni} as the nth root of those elements in $\hat{\phi}$ such that $\phi_n(j) = (\alpha_{ni})^n$. Note that this approach will give the exact MGMP coefficients if the system behaviour is well described by the model and is not corrupted by noise. Then, ϕ can be constructed from the obtained α_{ni} and compared to $\hat{\phi}$ in order to verify this statement. Other methods for coefficient extraction in over-parameterised systems can be found in [24] and the references therein.

Its worth mentioning that the parameter estimation process is done only during the training mode. Thus, although the training mode takes more computing time for the MGMP, the complexity of implementation in the running mode remains equal for both approaches (as long as the order of the polynomial and the length of the FIR filters are the same). Note that if no parameter separation is performed, then ϕ from (27) are simply the coefficients for the more general finite DTVM described by (15). In that case, the complexity during both operation modes is similar to that of the MGMP in the training phase.

5 Validation and discussion

In order to validate the behavioural model presented in Section 2, a circuit model of a CT SDM is simulated in Spice. This circuit model is also used to generate input–output data for the design of two different post-compensators and for the estimation of the parameters involved.

5.1 Circuit model of a SDM

The proposed post-compensation method is calibrated using signals obtained from a transistor level circuit model by transient simulations in Spice. This provides realistic simulation data, leading to general and reliable results when evaluating compensation performance. It also allows to verify which compensation model fits better the physical phenomena that cause the non-ideal behaviour.

The circuit model of a first-order CT SDM is shown in Fig. 6. Higher order architectures can be obtained by combining several first-order SDMs into a MASH structure, with the advantage that the inherent stability of a first-order modulator is preserved [1].

Our DUT has a sampling frequency of 100 MS/s, over a bandwidth from DC to 1 MHz, determining an over-sampling ratio OSR > 50 and a resolution of over 7 bits. Return-to-zero coding is used in the feedback loop, which is known to reduce errors in the modulation [1]. A latch outside the loop codes the signal in non-return-to-zero format. The architecture is fully differential and the design uses 180 nm complementary metal-oxide-semiconductor (CMOS) technology with the transistor model provided by manufacturer MOSIS.

In our simulation studies, different sinusoidal single-tone (ST) and multi-tone (MT) input signals are used to excite the circuit, as usually found in the literature [20, 21, 25].

5.2 Behavioural model simulation

The simulation of the behavioural model of a CT SDM presented in Section 2 is based on the modification of an ideal SDM. First, we introduce the third-order polynomial of (1) preceding the ideal integrator. Then, an FIR filter is used to model the feedback DAC. For that case, a first-order discrete-time filter impulse response can be written as

$$v(k) = \sum_{l=0}^{\infty} p^l u(k-l) \tag{31}$$

which is clearly an IIR filter. However, since $|p| < 1$, the

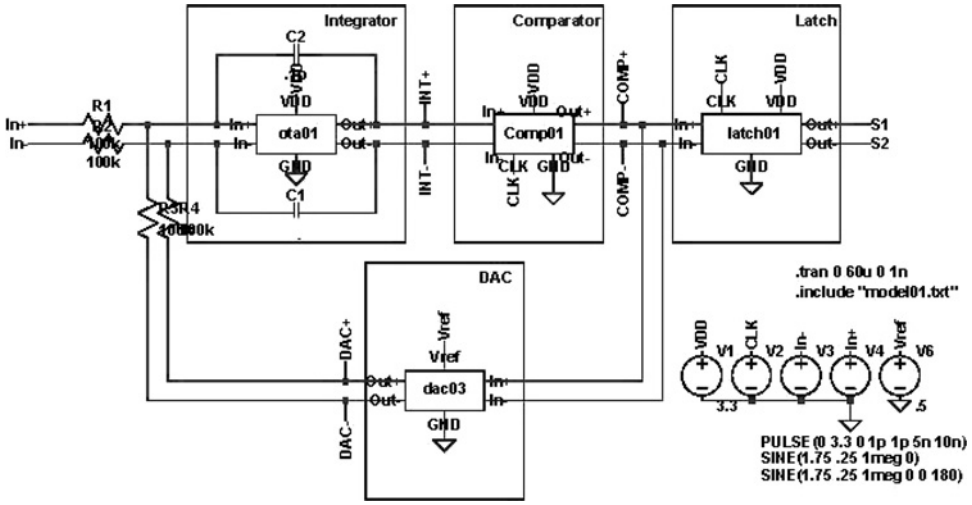

Fig. 6 *Circuit model of a SDM simulated in Spice*
Architecture is fully differential and uses 180 nm CMOS technology

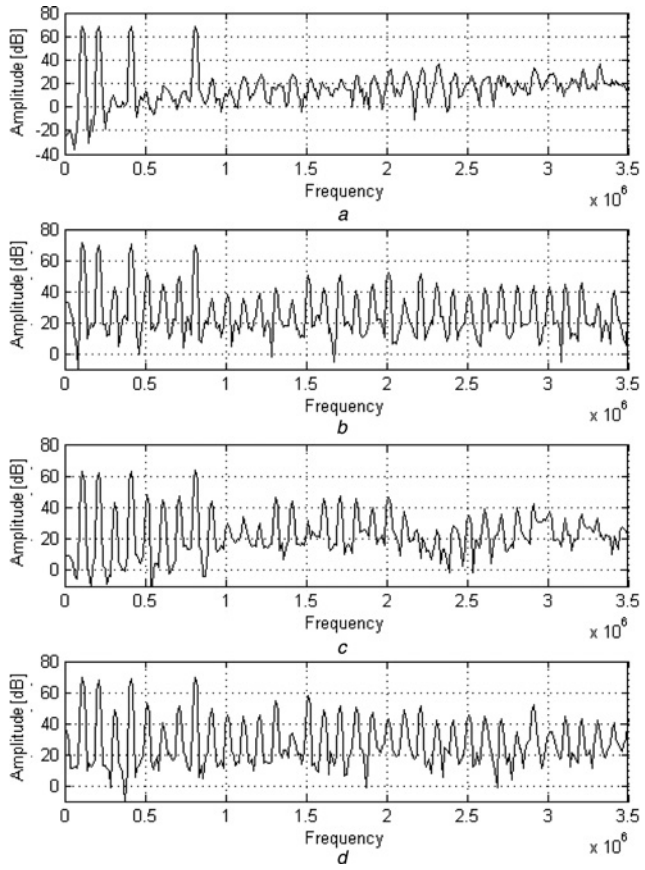

Fig. 7 *Output spectrum*

a Ideal SDM
b Circuit model
c Behavioural model with DAC represented by a delay
d Behavioural model with DAC represented by a two tap FIR filters

response can be truncated and a good approximation is obtained by a FIR filter with just a few taps.

Fig. 7 shows the simulated output spectrum of an ideal SDM (top), the circuit model (below), and the behavioural model using just a delay to represent the feedback DAC and a two tap FIR filters (bottom). The addition of the FIR filter clearly models the raise in the noise floor and some high-frequency peaks that are not present when using a single delay to model the DAC, when compared to the circuit model output spectrum.

5.3 Simulation results

The performance of the compensation method was simulated in MATLAB for different sets of input–output signals provided by the circuit model of the SDM. An ideal SDM was simulated in MATLAB both to estimate the parameters of the compensators and to measure their performance through the generation of the signal y_I. The input signal used to excite this ideal modulator is imported to MATLAB from the circuit simulator software, so the output of both models can be compared.

Fig. 8 shows the reduction in mean squared error (MSE) as a function of FIR order M for the case of a ST input signal, a 200 kHz sinusoid. The identification of the compensation block was first performed for different polynomial order N keeping a fixed filter order M, and the MSE in prediction $\sum (y_I - \hat{y}_I)^2$ was analysed [17].

When using an MP model as compensator, see (17), we see that the MSE reduction for $N = 2$ is more than an order of

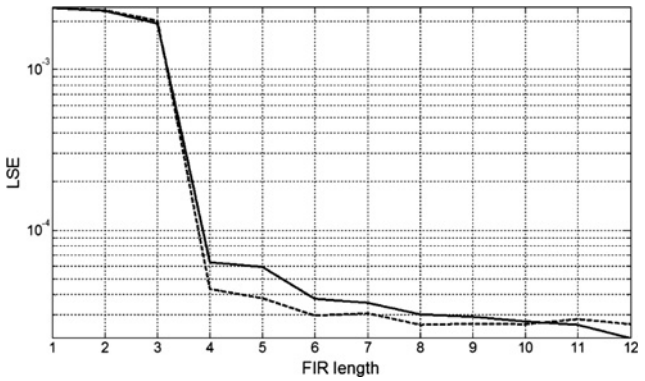

Fig. 8 *LSE in training (full line) and running (dashed line) phases as a function of M for a polynomial order of 2*

magnitude. Then, for a fixed value of N the MSE was computed as a function of M. Again, a large reduction in the measured error is observed for $M \geq 5$. The same procedure was carried out to evaluate the performance of the MGMP model described in (18) and (19). In the case of the MGMP, the compensation performance was evaluated using the parameter vector $\hat{\boldsymbol{\phi}}$ from (29) before coefficient extraction. A comparison with the MP model is done in Table 1.

Fig. 9 shows the spectrum of the input ST signal and the output of the DUT before and after compensation using both an MP and an MGMP as compensators. It is clear that after compensation all harmonics are significantly reduced. Furthermore, the signal to noise and distorsion (SINAD) ratio was computed for the DUT before and after compensation, and compared to the theoretical result for SNR of an ideal distorsionless SDM, showing a close to ideal behaviour for the compensated SDC (Table 1).

In all cases the parameters chosen for comparing the performance were $N = 2$ and $M = 9$. We consider a longer length for the FIR filters because higher frequency signal components (above the 200 kHz tone of the previous example) introduce longer memory effects. This results in the estimation of $P_1 = 18$ parameters for the MP and $P_2 = 54$ joint parameters for the MGMP. Thus, the training requires $P_1^2 + P_1(L - P_1)$ and $P_2^2 + P_2(L - P_2)$ multiplications for the MP and for the MGMP, respectively, when computing the post-compensation block. Here, L is the length of the training sequence, which has to be larger than P_i for the estimate to be unbiased. However, this processing is done by LS off-line.

In the running mode, the extra digital processing required is NM multiplications and $NM - 1$ additions in order to compute the corrected output sample, where M is the length of the FIR filters and N is the order of the polynomial. However, this requires low aditional computational power

Table 1 LSE and improvement in SINAD and SFDR for ST and MT analysis ($N = 2$, $M = 9$)

	ST(MP)	ST(MGMP)	MT(MP)	MT(MGMP)
LSE	2.2×10^{-5}	2×10^{-5}	4.5×10^{-4}	3.1×10^{-5}
SNR, dB	69	69	–	–
$SINAD_{bc}$, dB	34.2	34.2	–	–
$SINAD_{ac}$, dB	68.5	68.3	–	–
$SFDR_{imp}$, dB	26	26	17	22
parameters	18	54	18	54

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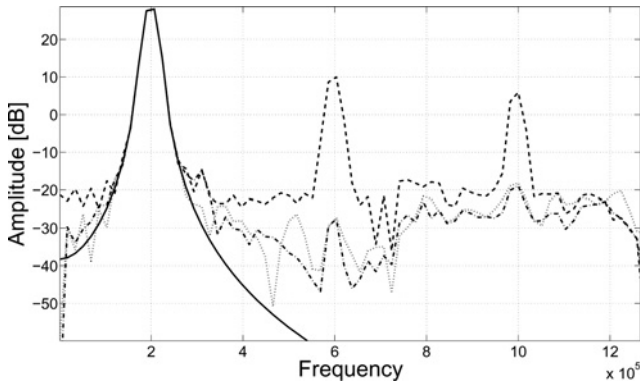

Fig. 9 *Spectrum of the input signal (full line) and the output of the DUT before (dashed line) and after compensation (MP: dot–dash; GMP: dots)*

since most DSP processors today have very efficient vector multipliers and are optimised for FIR filter calulations (e.g. see [26]).

The tests using ST signals show that a large improvement can be obtained by compensation using both models, but it is not clear which one offers a better representation for the dynamics of the system. For this purpose, a more general signal has to be used as excitation for the circuit model of the SDM. Therefore we chose a MT signal with four tones at 100, 200, 400 and 800 kHz. This signal does not only cover most of the signal bandwidth but frequencies are chosen in such a way that harmonics because of different frequency components do not overlap.

Fig. 10 shows the spectrum of the input signal and the output of the DUT before and after compensation using both models. We see that both models achieve a good cancellation of harmonic distortion. However, the MSE is an order of magnitude lower for the MGMP (see Table 1). The spurius free dynamic range (SFDR) improvement obtained with the MGMP is about 7 dB higher than that of the MP. This can be explained by the presence of cross-terms in the MGMP, which allows to model the dynamics of the system in more detail. These cross-terms arise from the linearisation of (18). Thus, the number of estimated parameters increases dramatically because of the over-parametrisation (19). Therefore there is a trade-off between accuracy and complexity.

Finally, some additional tests have been performed to evaluate the robustness of the post-compensators when

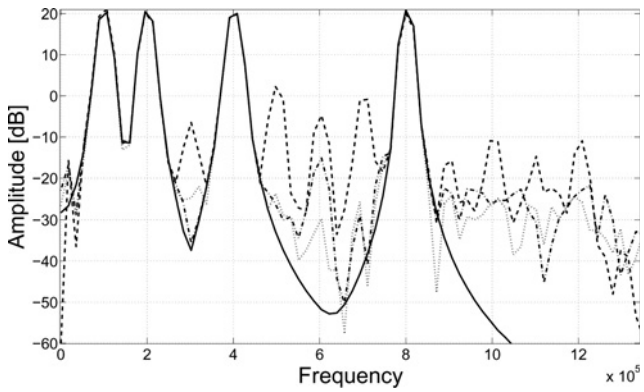

Fig. 10 *Spectrum of the input signal (full line) and the output of the DUT before (dashed line) and after compensation (MP: dot–dash; GMP: dots)*

Table 2 SFDR improvement when sampled and training signals differ

Frequency shift	SFDR improvement (MP), dB	SFDR improvement (MGMP), dB
0%	17	22
5%	11	10
10%	7	5
DMS	5	0

sampling signals somewhat different to those used in the training phase are applied. For this purpose, we test the compensator performance in terms of SFDR when the sampling signal has a frequency shift of 5 and 10% in each frequency component compared with the MT signal used for training. In adition, we also test the compensator performance when sampling a different multi-tone signal (DMS) composed of four tones in 200, 300, 500 and 700 kHz (while the tones used in the training mode were 100, 200, 400 and 800 kHz). The results are shown in Table 2.

From these results we see that there is still an improvement in all cases when using an MP as compensator, even if it is lower when sampled and training signals differ. In the case of the MGMP, the improvement in SFDR is more sensitive to mismatch between the sampled and training signals. This is not surprising, since the MGMP has more parameters that the MP compensation, allowing some degree of overtraining. However, no deterioration in the performance occur even in the worst case.

6 Conclusions

A complete behavioural model of a CT first-order SDM is presented in this work. This model includes the main non-linear and non-ideal effects that degrade the performance of the system. The validity of this model is evaluated comparing its behaviour with a circuit model simulated in Spice, showing good agreement between the mathematical expressions and the circuit output. The resulting dynamic model is weakly non-linear, which allows for a Volterra representation of it. This also means that the system can be p-linearised with a Volterra model of similar complexity, which leads to the development of post-compensators belonging to this family. The insight provided by the behavioural model excludes the use of simple Hammerstein and Wiener box models for the compensation block. Thus, two post-compensators that are generalisations of them are developed and tested. The performance of such compensators is then evaluated and compared by simulations in MATLAB, using the usual metrics for ADCs as SFDR, SINAD and MSE. As expected, the MGMP results in better cancellation of distortion when a more general input signal is used to excite the circuit at the cost of higher complexity and more sensitivity to missmatches between training and sampled signals. Although a training is needed to obtain the model parameters, it can be performed previously off-line. This result in a low complexity implementation composed of a few FIR filters and a low-order polynomial that can be coded in a small sized table.

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