

Comparison of the degradation characteristics of AlON/InGaAs and Al₂O₃/InGaAs stacks

F. Palumbo, I. Krylov, and M. Eizenberg

Citation: *Journal of Applied Physics* **117**, 104103 (2015); doi: 10.1063/1.4914492

View online: <http://dx.doi.org/10.1063/1.4914492>

View Table of Contents: <http://scitation.aip.org/content/aip/journal/jap/117/10?ver=pdfcov>

Published by the [AIP Publishing](#)

Articles you may be interested in

[X ray photoelectron analysis of oxide-semiconductor interface after breakdown in Al₂O₃/InGaAs stacks](#)

Appl. Phys. Lett. **105**, 102908 (2014); 10.1063/1.4895627

[Indium out-diffusion in Al₂O₃/InGaAs stacks during anneal at different ambient conditions](#)

Appl. Phys. Lett. **104**, 243504 (2014); 10.1063/1.4882645

[The effect of post oxide deposition annealing on the effective work function in metal/Al₂O₃/InGaAs gate stack](#)

Appl. Phys. Lett. **104**, 202103 (2014); 10.1063/1.4879246

[Arsenic decapping and pre-atomic layer deposition trimethylaluminum passivation of Al₂O₃/InGaAs\(100\) interfaces](#)

Appl. Phys. Lett. **103**, 071602 (2013); 10.1063/1.4818330




[Minority-carrier characteristics of InGaAs metal-oxide-semiconductor structures using atomic-layer-deposited Al₂O₃ gate dielectric](#)

Appl. Phys. Lett. **89**, 132103 (2006); 10.1063/1.2357566



AIP | Journal of Applied Physics

Meet The New Deputy Editors

| | | | | | |
|---|---------------------------|---|----------------------|---|-----------------------|
|  | Christian Brosseau |  | Laurie McNeil |  | Simon Phillpot |
|---|---------------------------|---|----------------------|---|-----------------------|

Comparison of the degradation characteristics of AlON/InGaAs and Al₂O₃/InGaAs stacks

F. Palumbo,^{a)} I. Krylov, and M. Eizenberg

Department of Materials Science and Engineering, Technion – Israel Institute of Technology,
32000 Haifa, Israel

(Received 2 December 2014; accepted 28 February 2015; published online 13 March 2015)

In this paper, the degradation characteristics of MOS (Metal-Oxide-Semiconductor) stacks with Al₂O₃/AlON or Al₂O₃ only as dielectric layers on InGaAs were studied. The dielectric nitrides are proposed as possible passivation layers to prevent InGaAs oxidation. At negative bias, it has been found out that the main contribution to the overall degradation of the gate oxide is dominated by the generation of positive charge in the gate oxide. This effect is pronounced in MOS stacks with Al₂O₃/AlON as dielectric, where we think the positive charge is mainly generated in the AlON interlayer. At positive bias, the degradation is dominated by buildup of negative charge due to electron trapping in pre-existing or stress-induced traps. For stress biases where the leakage currents are low, the changes in the electrical characteristics are dominated by electron-trapping into traps located in energy levels in the upper part of the semiconductor gap. For stress biases with higher leakage current levels, the electron trapping occurs in stress-induced traps increasing the shift of V_{FB} towards positive bias. The overall results clearly show that the improvement of the high-k dielectric/InGaAs interface by introducing N into the Al-oxide does not necessarily mean an increase in the reliability of the MOS stack. © 2015 AIP Publishing LLC.

[<http://dx.doi.org/10.1063/1.4914492>]

I. INTRODUCTION

InGaAs is an attractive candidate to be used as a channel material for the extension of CMOS (Complementary Metal-Oxide-Semiconductor) technology beyond Si due to its high electron mobility.^{1–3} Lacking a good native oxide interface, a major challenge is the reduction of the density of interface states (D_{it}) at the semiconductor interface.^{3,4} High D_{it} values lead to inefficient Fermi level response, degrade the control of charge concentration in the channel, decrease the sub-threshold slopes, and reduce the drive current of metal-oxide-semiconductor field effect transistors (MOSFETs).⁵ High D_{it} values are manifested in the capacitance-voltage (C-V) measurements as a hump at the weak inversion regime, a phenomenon that is almost always observed in InGaAs-based gate stacks at room temperature.^{6–9} Krylov *et al.* have shown that an ammonia (NH₄OH) pretreatment of the InGaAs surface improved the C-V characteristics of alumina-based MOS capacitors, and reduced the mid-gap D_{it} . An X-ray photoelectron spectroscopy (XPS) study revealed that the treatment with NH₄OH suppressed Ga-O bonds development only after annealing in N₂ for 30 min at 400 °C.¹⁰ It should be noted that the improvements in D_{it} have been achieved to such levels that the multi-frequency C-V response associated with genuine surface inversion has been achieved.^{11–13}

Despite the wide literature available about the good interface passivation and excellent device performance obtained with this approach, very few reliability studies of this MOS stack have been reported.^{1,2} We have shown in

Ref. 14 that the degradation of such capacitors is strongly affected by the oxide-semiconductor surface treatment. Surface treatment with NH₄OH shows a better quality of the interface in terms of interface states;¹⁰ however, it contributes to generation of charge on the dielectric layer. The charge generation is mainly due to the interface contribution, since the accumulation of trapped charge is accompanied by the generation of interface states.¹⁴ The physical origin of the interface contribution can be understood in terms of the dissociation of the bonds at the interface (i.e., depassivation of the interface).^{14,15} Therefore, since the suppression of the Ga-O bonds by the treatment with NH₄OH only occurs after the annealing in N₂, it opens the question about the role of N in the generation of defects/charge in the gate oxide.

Although it is well known that in standard Si/SiO₂ stacks the addition of N to the SiO₂ gate oxide has an adverse effect on reliability,^{16–18} there is no information about the role of N in the degradation of high-k dielectric/InGaAs stacks. It is clear that more information is needed to describe and model the mechanisms responsible for the degradation of high-k dielectric/InGaAs stacks.

In this work, the analysis of the degradation characteristics of metal gate (MG)/high-k dielectric/InGaAs stacks with Al₂O₃/AlON in comparison to Al₂O₃ only gate dielectrics is performed under constant voltage stresses (CVS). The addition of N is not applied to the InGaAs interface by NH₃ treatment as in Ref. 10, but rather by creating with ALD (atomic layer deposition) an N-enriched AlO_x inner layer; NH₄OH was used as a chemical passivation step for both samples prior to the ALD. In the first part of the manuscript, the influence of the AlON interlayer on the electrical characteristics is analyzed, while the second part is focused on the study of

^{a)}Author to whom correspondence should be addressed. Electronic mail: felix.palumbo@conicet.gov.ar. Tel.: +54-11-6772-7128.

the dynamics of degradation of the flat band voltage (V_{FB}) and the generation of defects at interfaces of the stack.

II. EXPERIMENTAL

An n-type Sn-doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layer ($7 \times 10^{16} \text{cm}^{-3}$) 500 nm thick was grown by metal-organic molecular beam epitaxy (MOMBE) on an n-type InP substrate. Before ALD of the dielectric stacks, the samples were cleaned in acetone, methanol, and propanol, rinsed in de-ionized water (DI), dipped into a diluted H_2SO_4 solution for 30 s, dipped into DI water, and treated with NH_4OH 36% solution for 1 min. The samples were introduced into the ALD chamber within less than 3 min after the pre-deposition treatment. This procedure results in a relatively low density of interface states.¹⁰ Two different gate dielectric stack were deposited by ALD at 270°C — Al_2O_3 (20 nm) and Al_2O_3 (10 nm)/ AlO_xN_y (10 nm). The deposition precursors of Al_2O_3 were trimethylaluminium (TMA) and H_2O , while tetrakis-dimethylaminoaluminium and NH_3 served for the deposition of AlO_xN_x . The thickness of the samples was confirmed by ellipsometry. We note that both gate stacks have a similar physical thickness of the dielectric layer. The gate electrode, Au (200 nm)/Ti(≈ 2 nm) was deposited by electron beam deposition and patterned by the lift-off technique. The area of all devices is $4 \times 10^{-4} \text{cm}^2$. The samples were annealed in N_2 at 400°C for 5 min. We note that both kinds of gate stacks have the same metal/dielectric interface while the dielectric/InGaAs interface differs by the nitrogen content in the dielectric.

C-V measurements were carried out at different frequencies using an Agilent 4285A LCR meter. Current-Voltage (I-V) and CVS measurements were performed using an Agilent 4155C parameter analyzer. During CVS, the stress was periodically interrupted for C-V measurements to track the degradation of the device parameters such as V_{FB} . For each stress condition, a dozen of devices were measured. To avoid recovery-related artifacts, we kept constant values of the delay time between the C-V measurements and the CVS pulses. The calculation of V_{FB} was performed by the recently introduced inflection point technique.¹⁹

III. RESULTS

A. Influence of the AION interlayer

Figure 1 shows typical C-V hysteresis curves at 500 KHz of the two sets: set A ($\text{Al}_2\text{O}_3/\text{AION}$) and set B (Al_2O_3). The C-V hysteresis measurement was done in a retrace mode, where the voltage was swept from inversion to accumulation and back to inversion (see arrow 1 in Figure 1). It should be noted that both C-V curves reach the same level at inversion if the voltage limit is large enough. While in strong accumulation if the voltage limit is large enough set A ($\text{Al}_2\text{O}_3/\text{AION}$) reaches a higher value of capacitance that might be explained by an increase of the k value for the AION interlayer.²⁰

By comparing the C-V curves in Figure 1, we observe similarity in the C-V hysteresis measured at flat band ($\Delta V_{FB}^{\text{Hysteresis}} \approx 0.055 \text{V}$ for both sets), but differences in the C-V stretch out showing that the main difference between

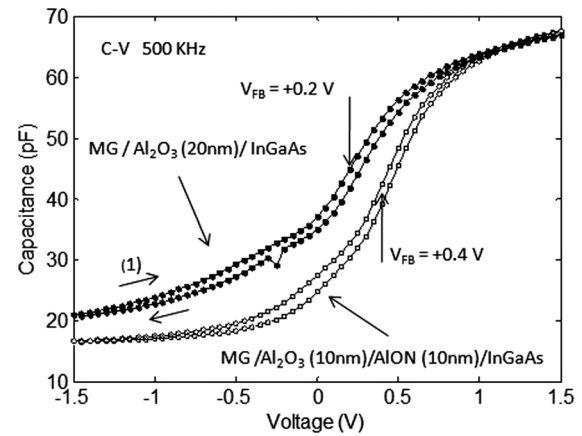


FIG. 1. Typical C-V hysteresis curves measured in retrace mode. Open symbols correspond to set A [$\text{MG}/\text{Al}_2\text{O}_3$ (10 nm)/ AION (10 nm)/InGaAs]; close symbols correspond to set B [$\text{MG}/\text{Al}_2\text{O}_3$ (20 nm)/InGaAs].

both sets of samples is related to the density of interface states, and not to the charged defects close to the oxide/InGaAs interface, namely, border traps.^{21,22} The MOS stack with the AION/InGaAs interface (set A) shows a reduction in the C-V stretch out, which is a clear indication of a lower density of interface states. This is also consistent with the reduction of the frequency dispersion of the C-V at negative bias (Figure 2), defined in the literature as “weak inversion

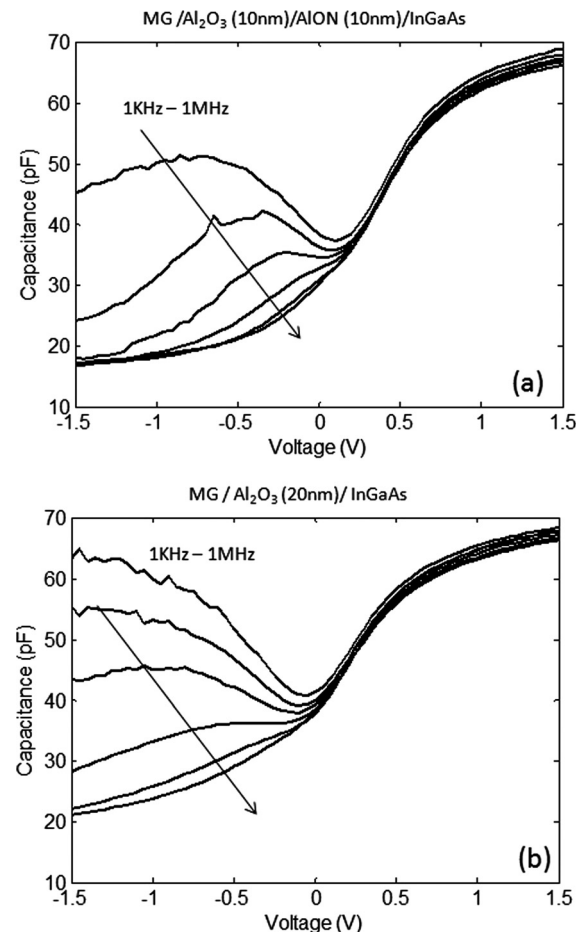


FIG. 2. Typical multi-frequency capacitance-voltage curves from 1 KHz to 1 MHz (a) for set A corresponding to $\text{MG}/\text{Al}_2\text{O}_3$ (10 nm)/ AION (10 nm)/InGaAs; (b) set B corresponding to $\text{MG}/\text{Al}_2\text{O}_3$ (20 nm)/InGaAs.

hump,” which is attributed to oxide/InGaAs interface states.¹⁰ These results suggest, in agreement with recent papers,^{20,23} that the dielectric nitrides are possible passivation layers to prevent InGaAs oxidation. It might be attributed to a smaller extent of out-diffusion of Ga and As atoms from the substrate into the high-k dielectric layer associated with the blocking role of AION.²⁰

Another relevant feature of Figure 1 is the difference between both sets in the flat band voltage (V_{FB}). The larger positive value of V_{FB} for set A ($\text{Al}_2\text{O}_3/\text{AION}$) can be explained by the characteristics of the AION interlayer. Choi *et al.* have shown that the incorporation of nitrogen in high-k dielectrics during ALD deposition on semiconductors such as GaN, Si, and III-As acts as a source of negative fixed charge.²⁴ On the other hand, regarding the density of interface states, it was reported that the incorporation of nitrogen may be also effective in alleviating the problem of native interface defects.²⁴ Therefore, the incorporation of N into Al_2O_3 to form AION explains both the increase of V_{FB} and the decrease of interface states as observed in Figure 1.

Finally, it is worth to note that the frequency dispersion in strong accumulation is similar in sets A and B (Figure 2). Although it is reported that AION oxide layers show less dispersion in frequency at strong accumulation,²⁰ it may occur that the variations are not significant to be measured since the oxide thicknesses of the samples in our study are relatively thick (20 nm).

Figure 3 shows the current-voltage (I-V) characteristics of both sets, where we observe large differences at positive and negative polarities. Since the physical thickness of the dielectrics is the same for both sets of samples, and the metal/dielectric barrier is the same, the main reason of such differences must be related to the high-k/InGaAs barrier.²⁵ Based on the characteristics found in literature, it is reasonable to assume that the AION/InGaAs barrier is smaller compared to the $\text{Al}_2\text{O}_3/\text{InGaAs}$ barrier due to a reduction of the oxide band gap of AION.^{23,26}

Figure 4 shows the general trend of the absolute values of V_{FB} after CVS on both polarities for sets A and B. The samples were stressed at similar $V_G - V_{FB}$ values ranging

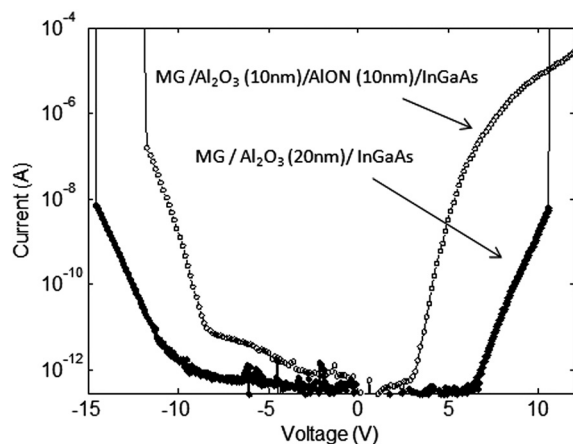


FIG. 3. Typical current-voltages (I-V) curves measured at room temperature. Open symbols correspond to set A [MG/ Al_2O_3 (10 nm)/AION(10 nm)/InGaAs]; close symbols correspond to set B [MG/ Al_2O_3 (20 nm)/InGaAs].

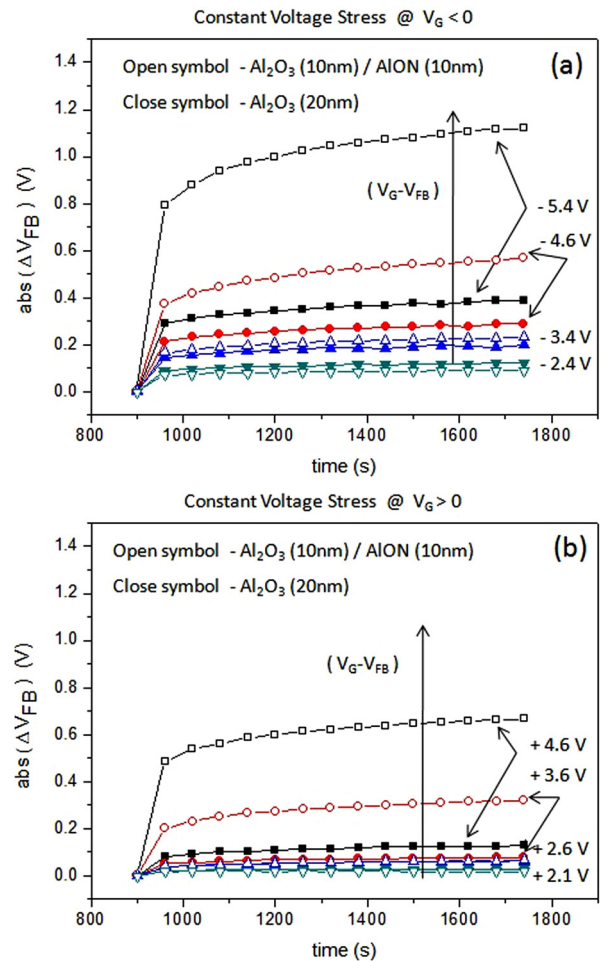


FIG. 4. Typical trend of the absolute values of V_{FB} after constant-voltage-stress (CVS) as function of the stress time on both polarities for sets A and B. Open symbols correspond to set A [MG/ Al_2O_3 (10 nm)/AION(10 nm)/InGaAs]; close symbols correspond to set B [MG/ Al_2O_3 (20 nm)/InGaAs]. The samples were stressed at similar $V_G - V_{FB}$ values ranging from -2.4 V to -5.4 V (Fig. 4(a)), and from $+2.1$ V to $+4.6$ V (Fig. 4(b)).

from -2.4 V to -5.4 V (Fig. 4(a)), and from $+2.1$ V to $+4.6$ V (Fig. 4 (b)). It is observed that the shift of $\text{abs}(V_{FB})$ for set A ($\text{Al}_2\text{O}_3/\text{AION}$) dominates at high stress values. Hence, even though the MOS stack with AION/InGaAs interface (set A) shows lower density of interface states (i.e., smaller C-V stretch out), it contributes with much more charge than the $\text{Al}_2\text{O}_3/\text{InGaAs}$ stack (set B) after CVS pulses at high voltages.

At this point it is particularly relevant to understand the origin of such observations. Although the larger shifts of the electrical characterizations of the set A ($\text{Al}_2\text{O}_3/\text{AION}$) could be associated with higher leakage currents levels,^{27,28} there is evidence in the literature that trapping²⁹ and/or depassivation of the high-k/InGaAs interface^{14,15} may also contribute to the degradation of the MOS stack.

B. Electrical stress at negative polarity

To clarify the physical origin of the changes generated due to stress at negative polarity, V_{FB} was studied as function of the stress voltage. Figure 5 shows the shift in V_{FB} as function of the stress voltage for CVS pulses of short

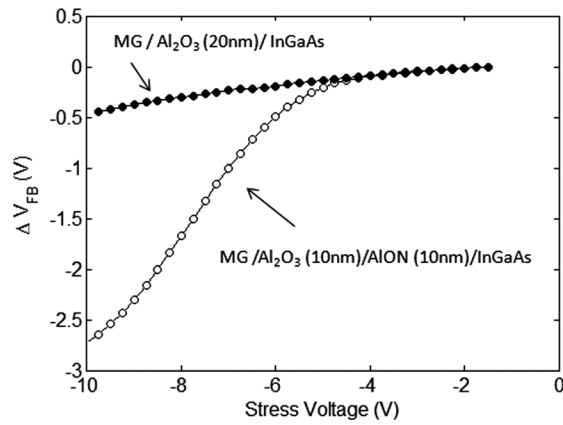


FIG. 5. Shift of the flat band voltage (ΔV_{FB}) as function of the stress voltage from C-V curves measured at 500 KHz. Open symbols correspond to set A [MG/Al₂O₃ (10 nm)/AlON(10 nm)/InGaAs]; close symbols correspond to set B [MG/Al₂O₃ (20 nm)/InGaAs]. On both cases CVS pulses of 1 s were used.

duration (≈ 1 s). V_{FB} was measured from consecutive C-V curves at 500 KHz while decreasing the minimal DC bias point in inversion (namely, the stress voltage in Figure 5), and with the same maximal DC bias point in accumulation. Since the recovery of trapped charge for the InGaAs/Al₂O₃ MOS system can be fast,²⁹ special attention was taken to keep constant and small (100 ms) the values of the delay time between measurements. This methodology extensively used to stress MOS stacks^{29–31} allows CVS pulses of short duration, reducing the percentage of trapped charge removed during the delay time, and avoiding recovery-related artifacts.³⁰

Figure 5 illustrates the effect of the minimal DC bias in inversion (marked as stress voltage in Fig. 5) on the shift of V_{FB} for sets A (Al₂O₃/AlON) and B (Al₂O₃). Similar shifts of V_{FB} for stress voltages up to -5 V are observed for both sets. For more negative stress voltages, set A (Al₂O₃/AlON) shows a significant decrease in V_{FB} . By comparing the results of Figure 5 with the I-V curves of Figure 3, it is clear that charge build-up due to higher injection current during the stress is not the reason for the decrease in V_{FB} of set A (Al₂O₃/AlON). The increase in current in the I-V curve (which occurs around -9 V) is not related to the onset point (≈ -5 V) of the decrease of V_{FB} of set A (Al₂O₃/AlON). It should be emphasized that these results are independent of the duration of the CVS pulse. As observed in Figure 4, a similar behavior is observed in longer CVS pulses.

Figure 6 shows the V_{FB} values calculated from the C-V hysteresis curves in the retrace mode (where the voltage was swept from inversion to accumulation and then back to inversion as exhibited in Fig. 1) after consecutive CVS pulses. The V_{FB} values marked by close symbols were measured with the voltage swept from inversion to accumulation, while the V_{FB} values marked by open symbols were measured from the C-V curve when the voltage was swept back to inversion. Therefore, the difference between both curves is the hysteresis at flat band (ΔV_{FB}^{hys}). Figures 6(a) and 6(b) show the V_{FB} values using this methodology for set A (Al₂O₃/AlON) and B (Al₂O₃), respectively, as function of the time during CVS pulses followed by an annealing at

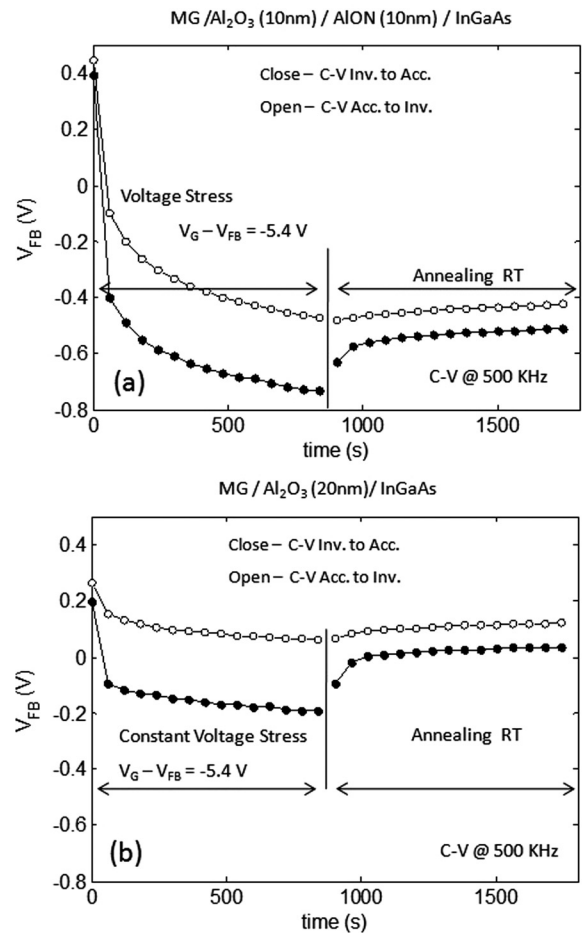


FIG. 6. The flat band voltage (V_{FB}) calculated from the C-V hysteresis curves in retrace mode. The V_{FB} points corresponding to close symbols were measured with the voltage swept from inversion to accumulation; while the V_{FB} corresponding to open symbols were measured from the C-V curve back to inversion. (a) Set A corresponding to MG/Al₂O₃(10 nm)/AlON(10 nm)/InGaAs; (b) set B corresponding to MG/Al₂O₃(20 nm)/InGaAs.

room temperature (27°C) without bias on the gate contact. As result of the stress pulses, the C-V curves shift towards negative bias indicating accumulation of positive charge in the gate oxide. It should be noted that the current level for the bias condition used in this figure ($V_G - V_{FB} = -5.4$ V) is of the order of pA for both sets of samples (see Figure 3) to avoid charge build-up due to higher leakage currents.

We observe that even though the shift in V_{FB} is much larger for set A (Al₂O₃/AlON), the magnitude of the hysteresis after the stress is similar for both samples. This observation suggests that the stress-induced charge (responsible for the shift in V_{FB}) is mainly related to the volume of the AlON layer, since the defects that contribute to the C-V hysteresis are close to the oxide/InGaAs interface.^{14,21,22,31}

It should be pointed out that for both sets of samples the shift in V_{FB} includes an additional component of degradation. This is observed in Figure 6 by the fact that the C-V hysteresis and the conductance peak (results not shown here) increases significantly after the stress in both sets of samples. It should be noted that the charge trapping responsible for the C-V hysteresis is taking place primarily in the interfacial oxide transition layer between InGaAs and the ALD

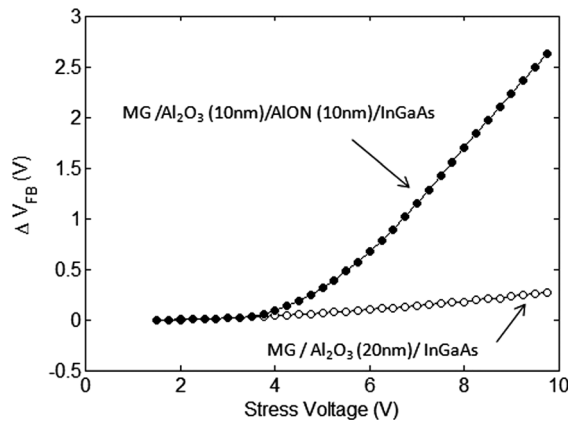


FIG. 7. Shift of the flat band voltage (ΔV_{FB}) as function of the stress voltage from C-V curves measured at 500 KHz. Close symbols correspond to set A [MG/Al₂O₃ (10 nm)/AlON(10 nm)/InGaAs]; open symbols correspond to set B [MG/Al₂O₃ (20 nm)/InGaAs].

deposited oxide.³¹ On the other hand, the measurements by the conductance method correspond to fast D_{it} states around mid-gap.⁵ Finally, we also observe recovery of the flat band voltage during the annealing at RT without bias on the gate contact. Although the recovery of the V_{FB} after CVS is not the scope of this work, the magnitude of this effect is consistent with earlier reports.^{29,30}

The comparison of the degradation characteristics at negative bias between set A (Al₂O₃/AlON) and set B (Al₂O₃) shows that the degradation is significantly enhanced when nitrogen (N) is added into the gate dielectric. We find that the main mechanism of degradation is not related to the high levels of leakage current through the gate oxide, but rather the volume of the AlON interlayer plays a major role in the overall degradation. At stress with a negative bias, we observe two components of positive charge build-up. One

component, which is present in both sets of samples, is associated with the generation of defects near the oxide/InGaAs interface due to the increase of the C-V hysteresis. The other component occurs only when the AlON interlayer is present. In this case, the generation of positive charge is independent of the C-V hysteresis indicating that the incorporation of nitrogen into the dielectric is the main reason of the charge build-up.

These results clearly show that the improvement of the dielectric/InGaAs interface by an AlON interlayer increases at the same time the buildup of oxide charges under CVS with negative bias. Therefore, further studies about the degradation characteristics in terms of the nitrogen content are needed to find the proper concentration that can improve the oxide/InGaAs performance without affecting the reliability of the stack.

C. Electrical stress at positive polarity

At positive bias the CVS experiments show a different behavior. Figure 7 shows the shift of V_{FB} as function of the stress voltage of CVS pulses of short duration using the same methodology of Figure 5. In this case, the V_{FB} values were measured from consecutive C-V curves where the same starting DC bias point in inversion was used, with an increasing maximal DC bias point in accumulation, marked as the stress voltage in Figure 7. We observe two regions as function of the stress voltage. At low voltages ($<+4.5$ V) both MOS stacks show a similar dynamics with no differences in the V_{FB} values, while at higher voltages ($>+4.5$ V), set A (Al₂O₃/AlON) shows a significant increase of V_{FB} . Contrary to the previous case of Figure 5, the onset of this variation is related to the increase of the current in the I-V characteristics

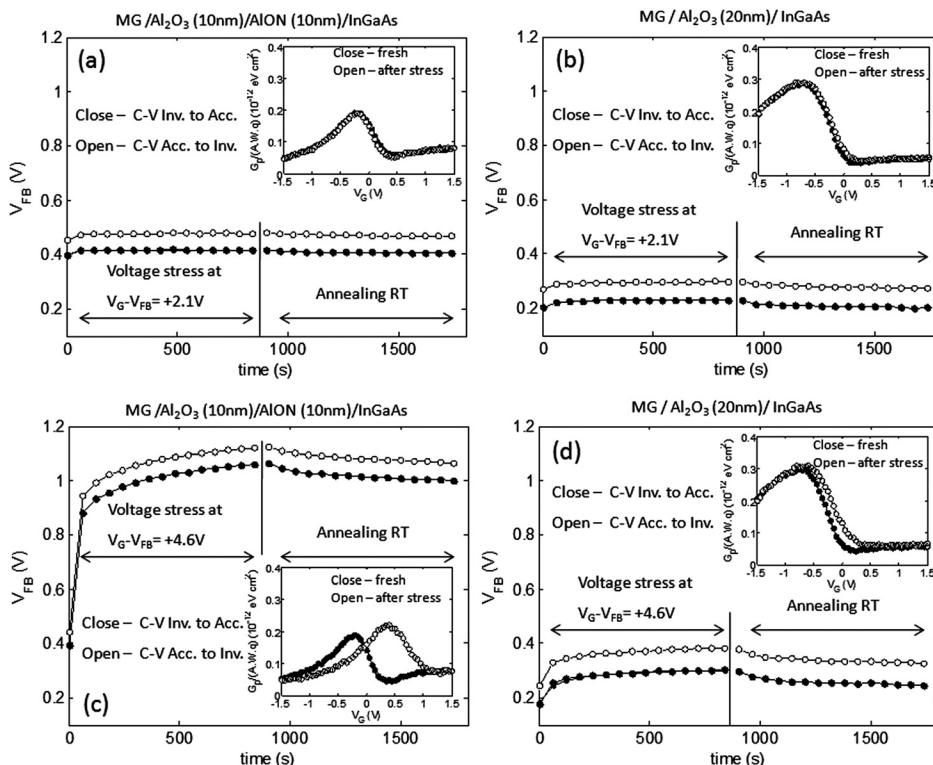


FIG. 8. The flat band voltage (V_{FB}) calculated from the C-V hysteresis curves in retrace mode. The V_{FB} points corresponding to close symbols were measured with the voltage swept from inversion to accumulation; while the V_{FB} corresponding to open symbols were measured from the C-V curve back to inversion.

in Figure 3, suggesting that it is a consequence of higher injection currents during the CVS experiment.^{27,28}

Figure 8 shows the V_{FB} values measured from the C-V hysteresis curves with the same methodology of Figure 6. The V_{FB} values marked by close symbols were measured with the voltage swept from inversion to accumulation, while the V_{FB} values marked by open symbols were measured from the C-V curve when the voltage was swept back to inversion. Figures 8(a) and 8(b) show typical results for both sets of samples after CVS pulses at $V_G - V_{FB} = +2.1$ V, where the leakage current is of the order of pA. Figures 8(c) and 8(d) show similar results after CVS pulses but for $V_G - V_{FB}$ values in the high voltage range ($>+4.5$ V), where the leakage current level is not equal for both sets. The current level for the set A ($Al_2O_3/AlON$) is two orders of magnitude higher than the current level of set B (Al_2O_3). It can be observed that in the regime of low voltages (Figures 8(a) and 8(b)) the dynamic of the V_{FB} shift is similar for both sets, showing no change in the magnitude of the shift (≈ 0.05 V), in the hysteresis (≈ 0.05 V), and in the conductance peak (see insets of Figures 8(a) and 8(b)). It is worth to note that the C-V hysteresis and the conductance peak are related to the generation of

defects near the oxide/InGaAs interface and fast interface traps around the mid-gap, respectively. On the other hand, in the regime of higher voltages (Figures 8(c) and 8(d)), we observe large differences in the dynamics of the V_{FB} shift as function of time, which are associated with the increase of the leakage current. Note that the set A ($Al_2O_3/AlON$) shows a significant increase of V_{FB} , and of the conductance peak (see inset of Figure 8(c)) indicating generation of defects during the CVS. The overall analysis of the dynamics of the V_{FB} shows that the buildup of negative charge (i.e., V_{FB} shift towards positive bias) is similar for both sets of samples as long as the leakage current level remains low.

This analysis can be extended by studying the particular features of the C-V curves after the stress pulses. Figures 9(a) and 9(b) show a comparative analysis between sets A ($Al_2O_3/AlON$) and B (Al_2O_3) of consecutive C-V curves after CVS in the low voltage regime ($V_G - V_{FB} = +2.1$ V) with a leakage current in the range of pA. In both cases (sets A and B), we observe a shift towards positive bias (i.e., accumulation of negative charge) of the upper part of the C-V curves with a similar difference between the onset point V_O with respect to V_{FB} in the C-V curves; $V_{FB} - V_O = 0.15$ V.

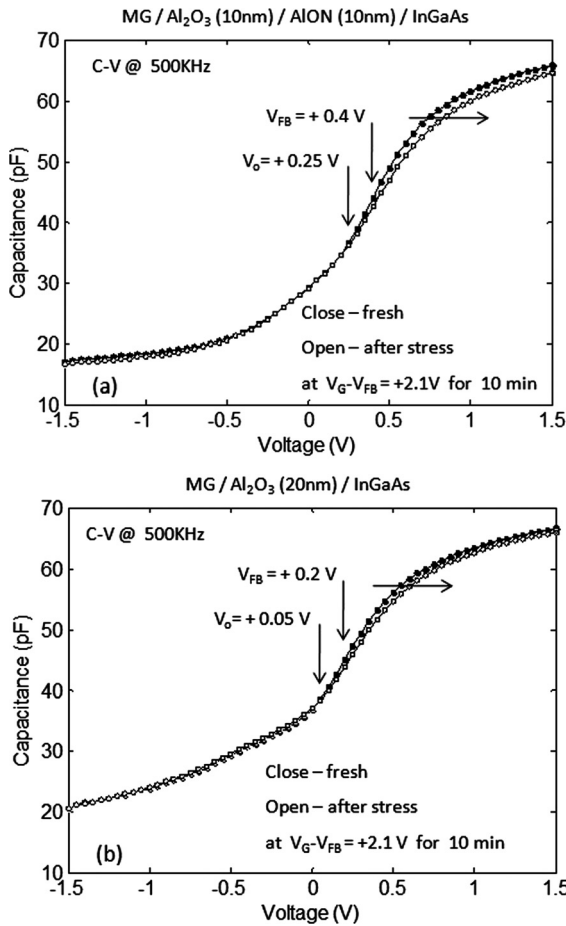


FIG. 9. Consecutive C-V curves at 500 KHz after CVS at $V_G - V_{FB} = +2.1$ V at room temperature with an accumulated stress time of 10 min. (a) for set A corresponding to MG/Al_2O_3 (10 nm)/ $AlON(10\text{ nm})/InGaAs$; (b) set B corresponding to MG/Al_2O_3 (20 nm)/ $InGaAs$. It is worth to note that the difference between the onset point V_O with respect to V_{FB} in the C-V curves is $V_{FB} - V_O = +0.15$ V.

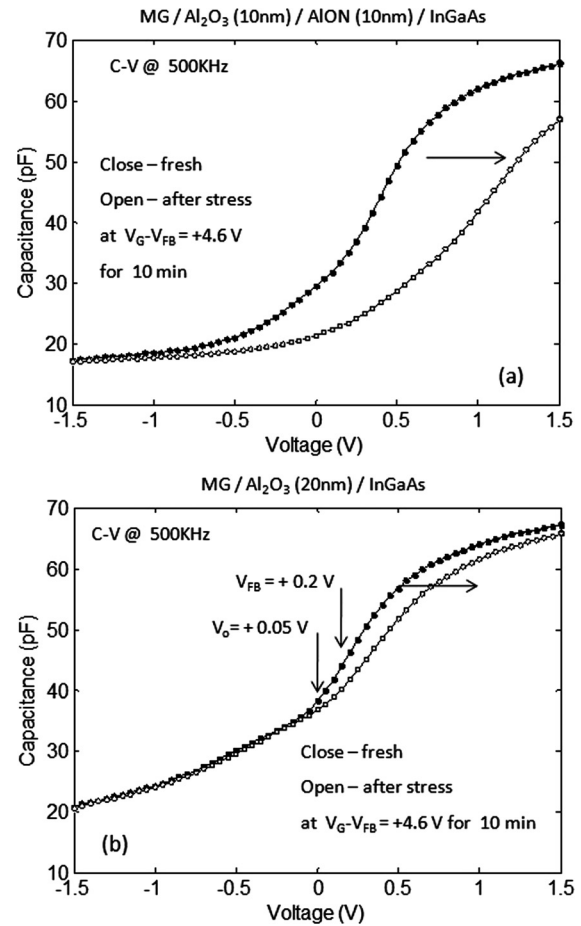


FIG. 10. Consecutive C-V curves at 500 KHz after CVS at $V_G - V_{FB} = +4.6$ V at room temperature with an accumulated stress time of 10 min. (a) for set A corresponding to MG/Al_2O_3 (10 nm)/ $AlON(10\text{ nm})/InGaAs$; (b) set B corresponding to MG/Al_2O_3 (20 nm)/ $InGaAs$. It is worth to note that only in this case the difference between the onset point V_O with respect to V_{FB} in the C-V curves is $V_{FB} - V_O = +0.15$ V.

Figures 10(a) and 10(b) show a similar comparative analysis between both sets, but in the high voltage regime ($V_G - V_{FB} = +4.6$ V). In this case, we observe large differences between the C-V curves, as expected from Figure 8. Figure 10(a) shows, for set A ($\text{Al}_2\text{O}_3/\text{AION}$), a translation of the C-V curve towards positive bias after the CVS, indicating accumulation of negative charge in the gate oxide, while Figure 10(b) shows, for set B (Al_2O_3), a different behavior. After the CVS pulse, we observe a shift towards positive bias only of the upper part of the C-V curve, showing similar features to those observed at low voltages (see Figure 9). It should be noted that even though the bias conditions in Figure 10 are similar for both sets of samples, the leakage current levels are not the same, showing a difference of more than two orders of magnitude (see Figure 3).

Based on these observations, we believe that the buildup of negative charge under positive bias could be caused by electron trapping. At low voltages, with very low leakage currents, the shift of V_{FB} reflects the carrier/defect energy alignment in the MOS stack as was suggested in our previous paper.³² The changes in the electrical characteristics are dominated by electron trapping into traps located in the oxide, at energy levels aligned with the upper part of the InGaAs gap. We believe that electron trapping is the main mechanism due to the absence of any modification of the C-V hysteresis and the conductance peak after the CVS.

Regarding the location of the traps, the similar features of the C-V curves for both sets (the equal difference between the onset point V_O with respect to V_{FB} in the C-V curves; $V_{FB} - V_O = 0.15$ V) indicate that the onset point for the distribution does not depend on the dielectric layer, in agreement with our previous paper.³² In this regime, as long as the leakage current remains low, we observe similar features of the C-V and of the dynamics of V_{FB} as function of the time under CVS pulses for both set of samples.

At high voltages, when the leakage currents are high, it is clear that the negative charge build up (i.e., C-V shift towards positive bias) is accompanied by generation of defects due to the higher leakage current levels, suggesting that electron trapping into defects generated by such higher injection current may also be responsible for the shift of V_{FB} towards positive bias.

IV. SUMMARY

In this paper, the influence of the addition of N to alumina-based gate oxide was studied by the comparison of the degradation characteristics of MOS stacks with $\text{Al}_2\text{O}_3/\text{AION}$ and Al_2O_3 as dielectric layers. It has been observed that the high-k/InGaAs stacks behave differently under positive and negative stress bias. Under negative stress bias, the degradation is dominated by the generation of positive charge in the gate oxide, and the accumulated charge is larger for MOS stacks with $\text{Al}_2\text{O}_3/\text{AION}$ as dielectric. The physical reason for such a difference lies in the origin of the generated charge that shifts the V_{FB} . It has been demonstrated that the main contribution to the overall degradation of the gate oxide occurs in the volume of the AION interlayer, resembling the situation of standard SiON/Si stacks,

where the addition of N to the SiO_2 gate oxide has a serious adverse effect on reliability.

Under positive stress bias, the degradation is dominated by buildup of negative charge due to electron trapping in pre-existing or stress-induced traps. For stress bias with low leakage currents, the changes of the electrical characteristics are dominated by electron-trapping into traps located in energy levels in the upper part of the semiconductor gap. For stress bias corresponding to higher leakage current levels, an additional component contributes to the degradation of the MOS stacks. In this regime, the electron trapping occurs in stress-induced traps, increasing thus the shift of V_{FB} towards positive bias.

The analysis of the electrical degradation is of utmost importance since InGaAs is the front runner candidate for n-type channels MOSFET. The results presented in this paper contribute to a better understanding of the limiting factors of the reliability of $\text{Al}_2\text{O}_3/\text{InGaAs}$ stacks. The overall results clearly show that the improvement of the high-k dielectric/InGaAs interface does not necessarily mean an increase of the reliability of the MOS stack. In the case of N addition to Al_2O_3 , the D_{it} improvement is followed by a compromise in the capacitor reliability.

ACKNOWLEDGMENTS

The authors gratefully acknowledge B. Kazer and J. Franco (IMEC) for inspiring discussions. Felix Palumbo is a permanent staff at CONICET, Argentina. The research leading to these results has been performed at the Technion–Israel Institute of Technology receiving funding from the European Union’s—Seventh Framework Program (FP7/2007-2013) under Grant Agreement No. 299094–MC–CONAT.

- ¹G. F. Jiao, W. Cao, Y. Xuan, D. M. Huang, P. D. Ye, and M.-F. Li, *IEEE Int. Electron Devices Meet.* **2011**, 27.1.1.
- ²S. Deora, G. Bersuker, W. Y. Loh, D. Veksler, K. Matthews, T. W. Kim, R. T. P. Lee, R. J. W. Hill, D.-H. Kim, W.-E. Wang, C. Hobbs, and P. D. Kirsch, *IEEE Trans. Device Mater. Reliab.* **13**(4), 507 (2013).
- ³S. Oktyabrsky and P. D. Ye, *Fundamentals of III-V Semiconductor MOSFETs* (Springer, New York, 2010).
- ⁴R. Chau, S. Datta, M. Doczy, B. Doyle, J. Jin, J. Kavalieros, A. Majumdar, M. Metz, and M. Radosavljevic, *IEEE Trans. Nanotechnol.* **4**, 153 (2005).
- ⁵R. Engel-Herbert, Y. Hwang, and S. Stemmer, *J. Appl. Phys.* **108**, 124101 (2010).
- ⁶E. O’Connor, B. Brennan, V. Djara, K. Cherkaoui, S. Monaghan, S. B. Newcomb, R. Contreras, M. Milojevic, G. Hughes, M. E. Pemble, R. M. Wallace, and P. K. Hurley, *J. Appl. Phys.* **109**, 024101 (2011).
- ⁷R. Engel-Herbert, Y. Hwang, J. Cagnon, and S. Stemmer, *Appl. Phys. Lett.* **95**, 062908 (2009).
- ⁸Y. Hwang, R. Engel-Herbert, N. G. Rudawski, and S. Stemmer, *J. Appl. Phys.* **108**, 034111 (2010).
- ⁹Y. Hwang, R. Engel-Herbert, and S. Stemmer, *Appl. Phys. Lett.* **98**, 052911 (2011).
- ¹⁰I. Krylov, A. Gavrilov, M. Eizenberg, and D. Ritter, *Appl. Phys. Lett.* **101**, 063504 (2012).
- ¹¹H. D. Trinh, E. Y. Chang, P. W. Wu, Y. Y. Wong, C. T. Chang, Y. F. Hsieh, C. C. Yu, H. Q. Nguyen, Y. C. Lin, K. L. Lin, and M. K. Hudai, *Appl. Phys. Lett.* **97**, 042903 (2010).
- ¹²E. O’Connor, S. Monaghan, K. Cherkaoui, I. M. Povey, and P. K. Hurley, *Appl. Phys. Lett.* **99**, 212901 (2011).
- ¹³T. D. Lin, Y. H. Chang, C. A. Lin, M. L. Huang, W. C. Lee, J. Kwo, and M. Hong, *Appl. Phys. Lett.* **100**, 172110 (2012).
- ¹⁴F. Palumbo and M. Eizenberg, *J. Appl. Phys.* **115**, 014106 (2014).
- ¹⁵N. Wrachien, A. Cester, Y. Q. Wu, P. D. Ye, E. Zanoni, and G. Meneghesso, *IEEE Electron Device Lett.* **32**(4), 488 (2011).

- ¹⁶J. H. Stathis and S. Zafar, *Microelectron. Reliab.* **46**(2), 270 (2006).
- ¹⁷V. D. Maheta, C. Olsen, K. Ahmed, and S. Mahapatra, *IEEE Trans. Electron Devices* **55**(7), 1630 (2008).
- ¹⁸S. Mahapatra, N. Goel, S. Desai, S. Gupta, B. Jose, S. Mukhopadhyay, K. Joshi, A. Jain, A. E. Isla, and M. A. Alam, *IEEE Trans. Electron Devices* **60**(3), 901 (2013).
- ¹⁹R. Winter, J. Ahn, P. C. McIntyre, and M. Eizenberg, *J. Vac. Sci. Technol., B* **31**, 030604 (2013).
- ²⁰L.-S. Wang, L. Liu, J.-P. Xu, S.-Y. Zhu, Y. Huang, and P.-T. Lai, *IEEE Trans. Electron Devices* **61**(3), 742 (2014).
- ²¹D. M. Fleetwood, *IEEE Trans. Nucl. Sci.* **39**, 269 (1992).
- ²²D. M. Fleetwood, M. R. Shaneyfelt, W. L. Warren, J. R. Schwank, T. L. Meisenheimer, and P. S. Winokur, *Microelectron. Reliab.* **35**, 403 (1995).
- ²³G. He, B. Deng, H. Chen, X. Chen, J. Lv, Y. Ma, and Z. Sun, *APL Mater.* **1**, 012104 (2013).
- ²⁴M. Choi, J. L. Lyons, A. Janotti, and C. G. Van de Walle, *Appl. Phys. Lett.* **102**, 142902 (2013).
- ²⁵E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology* (Wiley, New York, 2003).
- ²⁶R. H. French, *J. Am. Ceram. Soc.* **73**(3), 477 (1990).
- ²⁷S. Lombardo, J. H. Stathis, B. P. Linder, K. L. Pey, F. Palumbo, and C. H. Tung, *J. Appl. Phys.* **98**, 121301 (2005).
- ²⁸J. H. Stathis, *IBM J. Res. Dev.* **46**(2/3), 265 (2002).
- ²⁹J. Franco, A. Alian, B. Kaczer, D. Lin, T. Ivanov, A. Pourghaderi, K. Martens, Y. Mols, D. Zhou, N. Waldron, S. Sioncke, T. Kauerauf, N. Collaert, A. Thean, M. Heyns, and G. Groeseneken, *IEEE Int. Reliab. Phys. Symp. Proc.* **2014**, 6A.2.1.
- ³⁰J. Franco, B. Kaczer, P. J. Roussel, J. Mitard, S. Sioncke, L. Witters, H. Mertens, T. Grasser, and G. Groeseneken, *Int. Electron Devices Meet.* **2013**, 15.2.1.
- ³¹J. Lin, Y. Gomeniuk, S. Monaghan, I. M. Povey, K. Cherkaoui, E. O'Connor, M. Power, and P. K. Hurley, *J. Appl. Phys.* **114**, 144105 (2013).
- ³²F. Palumbo, R. Winter, I. Krylov, and M. Eizenberg, *Appl. Phys. Lett.* **104**, 252907 (2014).