Performance of annealed hybrid silicon heterojunctions: A numerical computer study

F. A. Rubinelli[a)]
Instituto de Tecnologia para la Industria Quimica (INTEC), Universidad Nacional del Litoral, Güemes 3450, 3000 Santa Fe, Argentina

L. F. Marsal and J. Pallarès
Department d' Enginyeria Electrónica, Universitat Rovira i Virgili, Avenida Països Catalans 26, 43007 Tarragona, Spain

(Received 12 May 2004; accepted 28 October 2004; published online 7 January 2005)

The performance of the standard hydrogenated amorphous silicon carbon–crystalline silicon solar cell is extensively compared with the performance of a hybrid structure subjected to a high-temperature annealing processing. Our analysis indicates that high-temperature-annealed heterojunctions show more robustness in the presence of energy offsets and defective amorphous-crystalline interfaces. Annealed hybrid cells are also less vulnerable to the negative impact of amorphous silicon carbon doped layers with poor electrical properties. Furthermore, annealed structures have the potential to generate higher efficiencies than conventional heterojunctions regardless of the wafer quality. The presence of boron at the amorphous-crystalline interface and in the wafer front region plays an important role in annealed hybrid structures that are made with low-quality wafers or where there is a highly defective amorphous-crystalline interface. In this scenario, a linear boron profile in the wafer front region is more appropriate, for which there is an optimum thickness. For low defect amorphous-crystalline interfaces and high-quality wafers, a boron exponential profile is more appropriate when boron creates additional defects in the front region of the wafer. The shape of the boron profile becomes less relevant when the boron does not add additional defects to the front region of high-quality wafers and when the amorphous-crystalline interface is low defect or defect-free. © *2005 American Institute of Physics*.
[DOI: 10.1063/1.1836006]

I. INTRODUCTION

Amorphous silicon/crystalline silicon heterojunction solar cells began to attract considerable attention once it had been demonstrated that high efficiencies (21%) can be achieved on Czochralski (Cz) silicon with a simple structure and a low-temperature process.[1] This practice has the potential to become a cost-effective alternative for present day crystalline silicon (*c*-Si) and poly-Si solar cell technology. The *p*-*n* junction is formed by plasma-enhanced chemical-vapor deposition (PECVD) at temperatures below 300 °C. The low-temperature process enables the use of cheaper lower-quality substrates. Back surface or passivating layers can also be added by deposition.

In general, amorphous-crystalline (*a*-*c*) silicon heterojunctions consist of a thin (<50 nm) highly doped amorphous silicon carbide window layer deposited on a crystalline silicon wafer. The window layer should have a high transparency to maximize the light absorption in *c*-Si and a high conductivity to minimize the series resistance losses. The band gap and the activation energy of the amorphous silicon layer can be easily tailored by PECVD deposition. This flexibility has led to many applications of hybrid heterojunctions as solar cells,[2] transistors,[3] x-ray detectors,[4] photoreceivers,[5] and light-emitting diodes.[6]

The main drawbacks of *a*-*c* heterojunctions are that (a) the defect density at the *a*-*c* interface can be high because of damage caused by polishing and by residual impurities remaining after the wafer has been cleaned and (b) offsets introduced by materials of different band gaps can impose serious limitations on photocarrier collection. An interesting way to overcome these negative features of heterojunctions is to anneal them at temperatures between 800 and 900 °C. At these high temperatures, the amorphous layer becomes a mixed-phase material that consists of submicron-size crystallites embedded in an amorphous matrix.[7,8] The presence of a fraction of microcrystalline phase in the amorphous matrix increases the electrical conductivity and decreases the optical band gap.[8] Under appropriate temperature and annealing conditions, impurity atoms from the deposited layer can diffuse into the substrate and move the *p*-*n* junction away from the metallurgical interface. Reference 9 discusses the effects that annealing can have on the electrical characteristics of *p*-type *a*-SiC on *n*-type crystalline silicon heterojunctions. This structure is called an annealed *a*-*c* heterojunction and it will be recognized in this paper as the *p*-*p*-*n* heterojunction by the presence of an "extra *p* layer" created in the first nanometers of the *c*-Si wafer by diffusion of boron from the *p*-*a*-SiC layer.

The aim of this paper is to explore the possible advantages of the *p*-*p*-*n* device over its counterpart, the single *a*-SiC/*c*-Si heterojunction. Using a detailed computer model-

[a)]Author to whom correspondence should be addressed; electronic mail: pancho@ceride.gov.ar

ing, we compare the efficiencies of both types of devices for different *a*-SiC band gaps, *a*-*c* offsets, diffused layer widths in the *c*-Si wafer, etc. First, and assuming that the electrical and optical parameters in the *c*-Si wafer are identical, we study the different scenarios in which the annealed *p*-*p*-*n* heterojunction performs better than the conventional *p*-*n* structure. We also discuss the real wafer status of both structures. Finally, we use computer simulations to explore how different boron profiles at the front region of the wafer affect the solar cell efficiency.

II. GENERAL INFORMATION

A. Modeling

Simulations were performed with the computer code D-AMPS, the AMPS' code (analysis of microelectronic and photonic devices developed at The Pennsylvania State University, USA[10]) plus some new developments. These new developments are the inclusion of amphoteric states,[11] the defect pool model,[12] and scattering at rough surfaces.[13]

We represent the density of states in *a*-SiC films with three different Gaussian distributions: D^-, D^0, and D^+. The peak energy of these Gaussians are located in the lower half of the band gap (D^-), close to the Fermi level of the intrinsic material (D^0), and in the upper half of the band gap (D^+), respectively. The ratio of charged-to-neutral defects was 4:1 and the correlation energy U was assumed to be equal to 0.2 eV. The peaks of the Gaussians were spaced 0.3 eV apart in energy and the density of states enclosed by each Gaussian is in agreement with the figures proposed by the defect pool model.[12] The separation between the nonoccupied D^+ peak and the double occupied D^- peak, usually known as Δ, was therefore equal to 0.4 eV and independent of the *a*-SiC band gap.

Neutral boundary conditions were adopted at the front and back contacts. The doping density, trap density, and cross sections in *c*-Si were selected to describe a high-quality *c*-Si wafer. In the annealed junction, the boron profile is represented by a function decaying exponentially from the *a*-*c* interface towards the *c*-Si bulk in agreement with experimental findings.[9] Finally, we will assume that back-surface field (BSF) is present at the back contact in order to gain insight into the full electrical potential of these structures.

Three different structures are compared in this paper: the single *p*-*a*-SiC/*n*-*c*-Si heterojunction that we will call device A or *p*-*n*; the double emitter *p*-*a*-SiC/PDL/*n*-*c*-Si heterojunction that we will call device B or *p*-*p*-*n* and where PDL stands for the region of the wafer where boron has diffused from the *p*-*a*-SiC layer by annealing; and finally, the *p*-*a*-SiC/*n*-*c*-Si structure or device C, which is the result of removing the PDL layer in device B. The first and the second solar cells (A and B) are real devices while the third solar cell (C) is included here only for purposes of comparison. This triple comparison allows us to analyze the separate impacts of lower offsets at the *a*-*c* interface and of the PDL layer on the solar cell efficiency. We pay particular attention to understanding the role played by the PDL layer in improving the solar cell efficiency.

TABLE I. Experimental parameters used in our simulations of *p*-*n* and *p*-*p*-*n* hybrid solar cells.

	Device A *p*-*a*-SiC/*n*-*c*-Si	Device B (annealed) *p*-*a*-SiC/*p*-*c*-Si/*n*-*c*-Si
a-SiC gap (eV)	1.9	1.4
a-SiC activation energy (eV)	0.4	0.05
a-SiC minority-carrier lifetime (s)	10^{-11}	10^{-11}
a-SiC thickness (nm)	50	50
Wafer minority-carrier lifetime (s)	10^{-3}	$2.5\times10_{-4}$
Wafer thickness (μm)	300	300
Wafer doping density (cm^{-3})	7×10^{15}	7×10^{15}
p-*c*-Si (PDL) layer-thickness (nm)	···	360
PDL layer-boron concentration at the *a*-*c* interface (cm^{-3})	···	5×10^{19}

B. Experimental knowledge

Table I lists the experimentally known electrical parameters used in our simulations. High-temperature annealing processing (800–900 °C) in hybrid structures gives rise to boron diffusion from the *p*-*a*-SiC layer into the wafer, which increases the emitter width. The resulting boron depth profile shows an exponential profile that reaches regions further from the *a*-*c* interface at higher temperatures.[9] The doping density in *a*-SiC is adjusted to match the experimental dark conductivity. The stoichiometry of this film is approximately $a\text{-}Si_{0.8}C_{0.2}$:H and the dark conductivity is around 32 $\Omega\ cm^{-1}$. The trap density and cross sections in *c*-Si are tailored to reproduce the wafer minority-carrier lifetime. Using the electrical and optical material parameters listed in Table I as input data in D-AMPS we checked our ability to fit available experimental dark *J*-*V*-*T* and light *J*-*V* curves in few *p*-*a*-SiC/*n*-*c*-Si (A) and *p*-*a*-SiC/*p*-*c*-Si/*n*-*c*-Si (B) samples. In annealed structures, the study of the transport mechanisms that control the dark current–voltage at different temperatures indicates that the diode is nearly ideal and has quite a low series resistance that will not limit the fill factor in solar cells.[9]

III. RESULTS AND DISCUSSION

In Sec. III A, we quantify the effect on the solar cell performance of several energy offset distributions, various defective layers at the amorphous-crystalline interface, and low and high activation energies at the *p*-*a*-SiC layer. In Sec. III B, we explore the dependence of the solar cell efficiency on the boron profile present in the *n*-*c*-Si wafer. We also study the possible deterioration of the device efficiency caused by boron atoms diffusing from the *p*-*c*-SiC layer into the PDL layer.

A. Basic features of hybrid solar cells

First, we will explore the advantages of the double-emitter configuration of structure B over the single-emitter configuration of devices A and C. Below we will discuss how annealing processing affects the difference in lifetimes between devices A and B (see Table I).

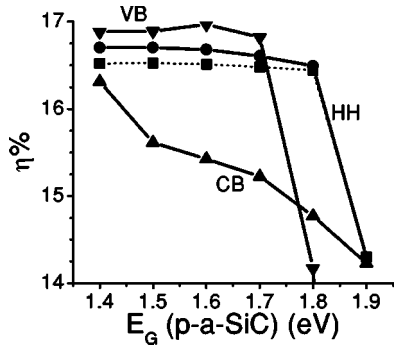

FIG. 1. Efficiency of the *p*-*n* hybrid solar cell with respect to the *p*-*a*-SiC band gap (devices A and C). The density of DB at the *a*-*c* interface is assumed to be 10^{11} cm^{-2}. CB, HH, and VB correspond to an offset that is entirely in the conduction band, half in the conduction band and half in the valence band, and entirely in the valence band, respectively.

1. Offsets

Rigorous modeling of *a*-SiC/*c*-Si heterojunctions requires special consideration to be given to the relative displacement of the conduction and valence bands at the *p*-*n* interface. Experimental work still has not unambiguously established the relative conduction- and valence-band displacement as the *p*-*a*-SiC band gap is widened or narrowed. When the band offset is entirely located at the conduction-band edge, the resulting potential barrier at the *a*-*c* interface mitigates electron back diffusion, thus reducing recombination losses in the *p*-*a*-SiC layer and undesired electron flows towards the front contact. The price to pay is that holes are pushed by a lower electric field to exit but there is no potential barrier that hinders collection. When the band offset is entirely located at the valence-band edge, the increased energy difference between Fermi levels in *a*-SiC and *c*-Si increases the electric-field intensity around the *a*-*c* interface and also reduces electron back diffusion. Holes drift with more intensity towards the front contact but they have to surmount a higher barrier at the *a*-*c* interface, which can increase recombination losses at the *a*-*c* defective layer. Hence, by changing the band alignments, we activate two competing effects and the final outcome has to be established in each particular case.

Figure 1 shows the impact of different offset alignments on the solar cell efficiency for different *p*-layer band gaps. The energy offset distribution nomenclature is as follows: CB stands for an offset entirely in the conduction band, HH stands for an offset that is half in the conduction band and half in the valence band, and VB stands for an offset entirely in the valence band. We cover the band-gap energy range going from high-temperature-annealed *a*-SiC (E_G=1.4 eV) (Ref. 7) to the standard material grown by PECVD (E_G =1.9 eV). For simplicity we have not included multiple step tunneling mechanisms in these simulations. Detailed discussions on the role played by tunneling currents at the *a*-*c* interface and their impact on the solar cell performance can be found in previous publications.[14] Tail slopes, the total dangling-bond density (DBD), and the acceptor doping density (N_A) were changed in accordance with the *a*-SiC band gap by reproducing the activation energies of 0.05 eV for E_G=1.4 eV and of 0.4 eV for E_G=1.9 eV. In Fig. 1 we have not included the PDL layer. Hence we are only looking at devices C and A for E_G=1.4 eV and E_G=1.9 eV, respectively.

TABLE II. *p*-*a*-SiC/*n*-*c*-Si built-in potentials for different *a*-SiC band gaps and band alignments; CB, HH, and VB correspond to an offset entirely in the conduction band, half in the conduction band and half in the valence band, and entirely in the valence band, respectively.

Offsets/gap (eV)	CB (eV)	HH (eV)	VV (eV)	E_A (*p*-layer) (eV)
1.4	0.84	0.98	1.12	0.05
1.5	0.77	0.96	1.15	0.12
1.6	0.7	0.94	1.18	0.19
1.7	0.63	0.92	1.21	0.26
1.8	0.56	0.9	1.24	0.33
1.9	0.49	0.88	1.27	0.40

When we assumed that offsets were equally split between the conduction and the valence band we adopted two different approaches. First, we moved the activation energy in the *p*-aSiC layer between 0.05 eV (E_G=1.4 eV) and 0.4 eV (E_G=1.9 eV) by adjusting the acceptor doping density. The activation energy varied linearly from 0.05 to 0.4 eV in conjunction with the band gap. This assumption of a linear variation varied the built-in potential (V_{bi}) with respect to the *a*-SiC band gap for any band alignment. Secondly, we assumed that the built-in potential V_{bi} was kept constant for different *a*-SiC band gaps. For the first scenario, Table II shows the offsets and activation energy adopted for each individual *p*-*a*-SiC band gap. Nomenclature is as in Fig. 1.

Figure 1 shows that for high *p*-*a*-SiC band gaps the transport of holes at the *a*-*c* interface is entirely blocked when the offset is completely in the valence band. For high *a*-SiC band gaps the performance of the (*p*)*a*-SiC/(*n*)*c*-Si heterojunction can become very sensitive to band alignment, something that cannot be controlled experimentally.

In our previous simulations different *p*-*a*-SiC band gaps (and therefore different offsets at the *a*-*c* interface) had given rise to different electric-field profiles inside the depletion region. In order to quantify the impact of different offsets on the solar cell performance without masking our results with the changes made to the electric-field profile in Fig. 1, we also show (dotted lines) the heterojunction efficiency for different *a*-SiC but constant built-in potential V_{bi} (shown only for HH alignments). For different band gaps the acceptor doping density in the *p* layer is adjusted so that the built-in potential V_{bi} is equal to 0.88 eV and E_G(*p*-*a*-SiC)=1.9 eV. As was observed when the electric field was allowed to vary with the *p*-*a*-SiC band gap, high band gaps make free-carrier transport more difficult and has a negative impact on the solar cell efficiency. The solid and the dotted lines (HH alignment) clearly show the separate impacts on the solar cell performance of lower offsets and higher electric fields. Figure 1 shows that the heterojunction is less sensitive to offsets at the *a*-*c* interface for lower offsets and for more intense electric fields in the depletion region (higher values of V_{bi}).

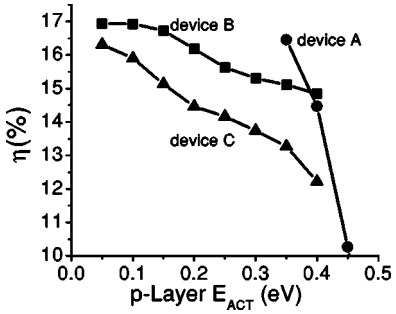

FIG. 2. Efficiency of hybrid solar cells with respect to the *p*-layer activation energy. The density of defect states at the *a*-*c* interface is equal to 10^{11} cm^{-2}.

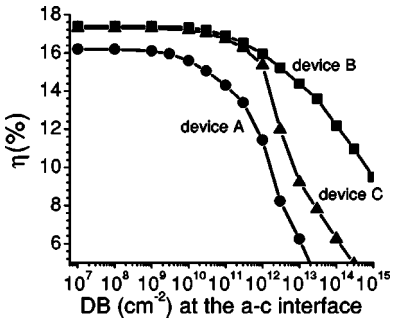

FIG. 3. Efficiency of hybrid solar cells with respect to the surface density of defects at the *a*-*c* interface. The defective *a*-*c* interface layer is assumed to be 10 nm thick and the boron density at the *a*-*c* interface is 5×10^{13} cm−2 in device B.

2. Activation energy at the (*p*)-*a*-SiC *layer*

Another benefit of the annealed *p*-*p*-*n* structure is the robustness introduced by the PDL layer in devices with a poor-quality *a*-SiC layer. Highly defective and/or noneffi-ciently doped (N_A) *p*-*a*-SiC layers reduce the solar cell efficiency in *p*-*p*-*n* structures to a lesser extent. The single *p*-*a*-SiC/*n*-*c*-Si heterojunction, on the other hand, is quite sensitive to these adverse characteristics of the amorphous layer.

Figure 2 compares the efficiency of the three structures for different *a*-SiC activation energies (E_{act}). In a single *a*-*c* heterojunction it is well known that the built-in potential V_{bi} is very sensitive to the activation energy of the amorphous layer. Figure 2 clearly shows the dramatic decrease in the efficiency of device A for higher *p*-*a*-SiC activation energies. As soon as the doping concentration is below the dangling bond density (DBD) the efficiency of the *p*-*n* solar cell collapses. In the annealed heterojunction, on the other hand, the efficiency is still acceptable for low N_A/DBD ratios (or, in other words, for high activation energies). In these simulations, we have assumed that the doping profile in the *p*-*c*-Si (PDL) layer is not changed when the doping density (or the activation energy) in the amorphous layer is varied. It is interesting to note that the efficiency of the annealed *p*-*p*-*c* structure (device B) also decreases at high values of E_{act} (*p*-*a*-SiC). In order to reach charge neutrality, the bands in the amorphous layer near the *a*-*c* interface are forced to bend downwards when E_{act} (*p*-*a*-SiC) is poor, which creates a higher barrier for holes flowing towards the *a*-*c* interface. This barrier hinders hole transport and favors recombination losses at the *a*-*c* interface in the PDL layer and the depletion region of the *n*-*c*-Si wafer. However, the recombination losses increase most in the amorphous layer because a higher barrier for holes at the *a*-*c* interface also means a lower barrier for electron back diffusion at the *a*-*c* interface.

The solar cell efficiency cannot be improved by using wafers with higher doping levels. Higher doping concentrations increase the built-in potential but also deteriorate the electrical properties of the wafer. Thinner *p*-*a*-SiC layers help to improve J_{SC} and consequently the efficiency because they reduce losses in the front region, mainly at blue wavelengths. Our code predicts a relative increase of almost 11% in the efficiency when we use a 10-nm-thick *p*-*a*-SiC layer instead of a 50-nm-thick layer. For the parameters used in our analysis, at 4-nm the electric field in the *p*-*c*-Si layer is shielded from the *a*-*c* interface. Hence, the *p*-*a*-SiC layer could be as thin as 8 nm so that the front contact is kept electrostatically isolated from the *p*-*c*-Si layer. Hence, thinner *p*-*a*-SiC layers are not recommended because any undesired band bending effect at the front contact could seriously harm the electrical field inside the PDL layer.

3. Defective layer at the amorphous-crystalline interface

Figure 3 illustrates the sensitivity of the different hybrid structures to the presence of a defective interface layer at the *a*-*c* interface. This defective layer is assumed to be 10 nm thick and to have the *c*-Si band gap.[15] We can see that the efficiency of the *p*-*n* structure (device A) initiates its decline for a surface defect density higher than just 10^9 cm^{-2} and its performance already shows a significant deterioration for a surface defect density of 3×10^{11} cm^{-2}. On the other hand, the annealed *p*-*p*-*n* structure (device B) is much more robust in the presence of such defective layers. A surface defect density of 10^{11} cm^{-2} does not harm its performance, which remains at around 17%. Furthermore, the efficiency is still well above 14% even for *a*-*c* interfaces as defective as 10^{13} DB/cm^2. The theoretical *p*-*n* device C shows greater sensitivity to the presence of an *a*-*c* defective layer than structure B for interface defective layers of more than 10^{12} DB/cm^2.

First, we will discuss our results for very low defect densities at the *a*-*c* interface. In this scenario, the recombination loss and the shielding effect on the electric field of the depletion region introduced by the *a*-*c* interface are negligible. Similar performances of devices B and C indicate that the PDL layer is not responsible for the fact that the efficiencies in device B are higher than those in device A. Table III lists the performances predicted by D-AMPS for the three

TABLE III. Predicted performances for structures without a defective layer at the *a*-*c* interface.

	Device A	Device B	Device C
J_{SC} (mA/cm^2)	28.20	29.17	29.18
V_{oc} (V)	0.784	0.765	0.753
FF	0.733	0.779	0.787
Efficiency (%)	16.20	17.40	17.30

structures when the presence of the *a*-*c* defective layer can be neglected.

Recombination losses are higher in device A than in devices B and C. In short circuit conditions, losses come mainly from recombination in the *p*-*a*-SiC layer (highest loss in structure A) and from electron back diffusion at the front contact (highest loss in structures B and C). Recombination losses in the wafer become dominant near V_{oc} and they control its value. In devices A and B, losses at the front contact and in the *p* layer do not significantly increase with voltage. The scenario is different in device C where recombination losses in the *p* layer rise considerably for forward voltages near V_{oc} due to the absence of the PDL layer. The higher back diffusion of electrons to the *p* layer is responsible for the lower values of V_{oc} predicted by our code for device C.

In device A the lower effective built-in potential (the activation energy is 0.4 eV instead of 0.05 eV) and the accumulation of free holes near the *a*-*c* interface give rise to a thinner depletion region in *c*-Si and to a less intense electric field in the wafer bulk. The weaker electric field in device A allows higher concentrations of free electrons and holes and more recombination, which leads to a poorer fill factor (FF). However, structure A shows a higher V_{oc} than devices B and C. Visual inspection of light *J*-*V* curves indicates that the *J*-*V* characteristic of structure A has a tail for forward voltages when the forward voltage approaches V_{oc}. This phenomenon is connected to the trapping and detrapping processes of holes at the *p* layer. The huge piling up of free holes at the *a*-*c* interface on the *c*-Si side restricts the trapped carrier distribution in the *p*-*a*-SiC layer by the charge neutrality condition. Holes are released from gap states to the valence band inside the *p* layer and preferentially near the *a*-*c* interface, which magnifies the net negative charge in this region. This scenario is connected to the creation of a light-induced dipole that introduces a voltage drop around the *a*-*c* interface, the sign of which is opposite to that of the applied force. When the forward voltage increases, the thickness of the depletion region in the wafer decreases, which allows more electrons to recombine with free holes accumulated near the *a*-*c* interface. The reduction of the free hole concentration at the *a*-*c* interface induces the trapping of back diffusing free holes inside the *p* layer, which subsequently reinforces the electric field in the depletion region and the wafer. The strengthening of the electric field increases the solar cell V_{oc} because a higher voltage is needed to achieve a total recombination loss equal to the photocurrent. This scenario also leads to a significant deterioration in FF.

The effective built-in potentials of devices B and C are higher because of the low activation energy of the annealed *a*-SiC layer. Higher built-in potentials lead to devices with better FF and J_{SC}. Better J_{SC} and FF are connected to a lower electron back diffusion in the *p*-*a*-SiC layer and at the front contact. A more intense electric field in the depletion region makes it easier to push electrons towards the wafer bulk.

Let us now discuss devices with a defective *a*-*c* interface layer. Table IV shows the performance predicted by D-AMPS for the three structures studied in this paper when they have an *a*-*c* defective layer with a surface density of 10^{13} cm^{-2}.

TABLE IV. Predicted performances for structures with an *a*-*c* defective layer with 10^{13} DB/cm^{-2}.

	Device A	Device B	Device C
J_{SC} (mA/cm^2)	28.05	27.66	29.09
V_{oc} (V)	0.458	0.630	0.467
FF	0.486	0.825	0.678
Efficiency (%)	6.24	14.39	9.23

We observe in our simulations that at short circuit conditions the main loss mechanisms are electron back diffusion at the front contact in device A and recombination in the *p* layer in device C, similar to what we found for high-quality interfaces. In device B, recombination losses at the interface defective layer are comparable to the electron back diffusion loss at the front contact and of the same order. In any case, the presence of a highly defective interface does not harm J_{SC} much. When a forward voltage is applied, recombination losses at the interface defective layer quickly increase at higher voltages in devices A and C. Table IV shows that FF is quite poor and V_{oc} is lower in these devices. On the other hand, the PDL layer in device B prevents electron back diffusion of photogenerated electrons from the wafer towards the interface. This result clearly shows the important role played by the *p*-*c*-Si (PDL) layer in achieving good V_{oc} and FF in hybrid structures with highly defective *a*-*c* interfaces and low *a*-SiC band gaps (1.4 eV). Device C still performs better than device A because of its higher effective built-in potential, which prevents some of the photogenerated electrons of the wafer from reaching the defective interface where they can recombine.

The three figures already shown indicate that the annealed structure is more robust in the presence of offsets and defective layers at the *a*-*c* interface than the single *p*-*n* hybrid heterojunction (A). In addition, Fig. 3 shows that for highly defective *a*-*c* interfaces the robustness of the *p*-*p*-*n* structure comes mainly from the PDL layer and not from the lower offsets at the *a*-*c* interface. The PDL layer allows the annealed heterojunction not only to sustain an acceptable built-in potential for a *p*-amorphous layer with poor electrical properties (Fig. 2) but also to host quite defective layers at the *a*-*c* interface while maintaining a quite reasonable efficiency. High *p*-SiC activation energies can considerably deteriorate the depletion region electric field in single *p*-*n* hybrid cells, which can significantly enhance the recombination of photogenerated carriers at the defective layer, in the depletion region and in the wafer. On the other hand, the annealed structure is more stable at low values of N_A or high densities of DB in the *p*-*a*-SiC layer because the PDL layer is able to sustain a reasonable intensity of the electric field inside the depletion region even in these adverse scenarios.

B. Boron diffusion into the wafer: Impact on the solar cell efficiency

In this section, we will study the dependence of the solar cell performance on the boron doping profile in the PDL layer or wafer front region and the possible negative effects of boron diffusion in the wafer.

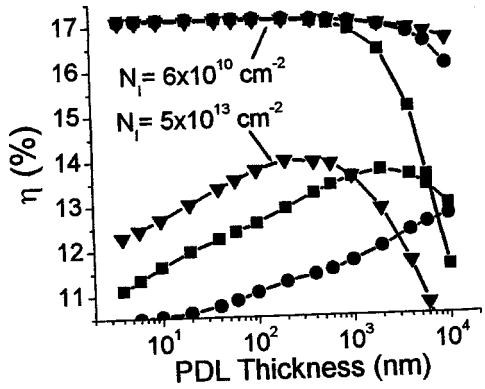

FIG. 4. Efficiency of the annealed *p-p-n* solar cell with respect to the PDL thickness for different boron profiles: (▼) linear distribution, (■) exponential distribution with F_W=6%, and (●) exponential distribution with F_W =0.5%. The surface density of defects at the *a-c* interface is assumed to be moderate (6×10^{10} cm^{-2}) and very high (5×10^{13} cm^{-2}).

1. Boron profile in the diffused (*p*)-*c*-Si (PDL) layer

It is interesting to explore how the efficiency of the annealed *p-p-n* structure depends on the boron doping profile in the PDL layer. In our simulations, the boron profile is represented by the following equation:

$$N_A(0)e^{(-x/X_d)}, \tag{1}$$

where $N_A(0)$ is the boron concentration at the *a-c* interface (5×10^{19} cm^{-3}) and x is the position with respect to the *a-c* interface ($x=0$). The parameter X_d (nanometer) is given by the expression $X_d=C_W W_{PC}$, where W_{PC} (nanometer) is the PDL layer thickness estimated to be 360 nm from our secondary-ion-mass spectroscopy (SIMS) profiles.[9] C_W (nondimensional) reflects how steep the boron exponential profile is. In order to reproduce the experimental boron profile. The most appropriate value for the parameter C_W was found to be 0.06.

The various exponential boron distributions are given by the figure $F_W=C_W\times100\%$. In the particular case of the experimental boron profile, F_W=6% and we can identify this distribution as the 6% exponential. Figure 4 shows the dependence of the solar cell efficiency on W_{PC} for two different boron exponential profiles (F_W=0.5% and F_W=6%) and for a linear boron profile. In this figure, we include results for devices that have a moderate and quite a high density of defects at the *a-c* interface. In the first case, we assume the presence of a surface defect density of only 6×10^{10} cm^{-2}. We observe that different boron concentration profiles do not give rise to significant differences in the solar cell performance for PDL layers thinner than 1000 nm. Although it cannot be clearly seen in Fig. 4, efficiency is maximum at a given optimum PDL thickness ($OPDL_W$): 17.127% at 10 nm in the linear profile, 17.122 at 60 nm in the 6% exponential, and 17.094 at 200 nm in the 0.5% exponential. PDL layers thinner than $OPDL_W$ enhance the FF but deteriorate the open circuit voltage (V_{oc}). The reverse is true for PDL layers thicker than $OPDL_W$. The current J_{SC} is quite a weak function of the PDL thickness. We find that for very thin PDL layers, recombination losses inside the PDL layer are negligible in comparison to losses at the *a-c* defective layer (and lower than losses at the *p* layer and front contact) making the solar cell efficiency almost insensitive to the boron profile.

A *p-n* junction located near the *a-c* interface efficiently extracts photogenerated holes and drifts electrons towards the wafer where they diffuse until they reach the back contact. In thick PDL layers, the linear distribution tends to build the *p-n* junction closer to the right edge of the PDL layer while steep exponential distributions tend to build the same *p-n* junction closer to the left edge of the PDL layer. As a result of this, the linear distribution gives rise to a *p-n* junction located further from the *a-c* interface and to an extremely thick effective *p* layer in the wafer. Because of its low electric field, this region does not efficiently push electrons towards the wafer and it gives rise to a high population of free holes, which significantly increases the recombination losses at the PDL layer. This scenario leads to high recombination losses and poor efficiencies. On the other hand, very steep exponential distributions efficiently expel minority carriers far from the defective *a-c* interface and holes towards the front contact. Thick PDL with a linear distribution gives rise to better V_{oc} than thin PDL layers with exponential distributions but they introduce a severe deterioration of J_{sc}. For instances comparing cells with a linear (L) and with a 0.5% exponential ($0.5E$) profile for a 1000-nm-thick PDL layer we obtain the following figures: V_{oc} (V)=0.724 (L) and 0.709 ($0.5E$), FF=0.778 (L) and 0.803 ($0.5E$), and J_{sc} (mA/cm^2) =20.52 (L) and 29.14 ($0.5E$). On the contrary, our simulations indicate that for highly defective *a-c* interfaces (see Fig. 4) linear boron or nonsteep exponential profiles are more appropriate. In general, a highly defective *a-c* layer significantly reduces V_{oc}. For a surface defect density of 5×10^{13} cm^{-2} and assuming a 200-nm-thick PDL layer, we have V_{oc} (V)=0.636 (L) and 0.513 ($0.5E$), FF=0.825 (L) and 0.805 ($0.5E$), and J_{sc} (mA/cm^2)=26.61 (L) and 27.29 ($0.5E$). In these devices V_{oc} is mostly determined by recombination losses in these highly defective *a-c* interfaces and, to a much lesser extent, by recombination losses in the PDL layer where the electric field has been weakened or partially shielded by the defective *a-c* interface. The linear boron profile prevents better electron back diffusion towards the *a-c* interface where they can easily recombine.

The detrimental effect of defective layers at the *a-c* interface in *p-p-n* solar cells is more pronounced when the concentration of boron is lower at the *a-c* interface $N_A(0)$. Figure 5 illustrates this point and shows the dependence of the solar cell efficiency on $N_A(0)$ for different *a-c* interface qualities. The concentration of $N_A(0)$ also determines the boron profile inside the PDL layer. A higher density of defects at the *a-c* interface and/or lower values of $N_A(0)$ tend to reduce V_{oc}. The weaker electric field at the PDL layer prevents in lesser extent back diffusion of electrons toward the *a-c* interface and increases the recombination losses at the interface and inside the PDL layer.

2. Boron profiles in low-quality wafers

In our simulations, we adopted a wafer minority-carrier lifetime of 2.5×10^{-4} s (see Table I). Annealed hybrid cells were also fabricated with wafers of lower quality and a minority-carrier lifetime of 4×10^{-6} s. It is interesting to un-

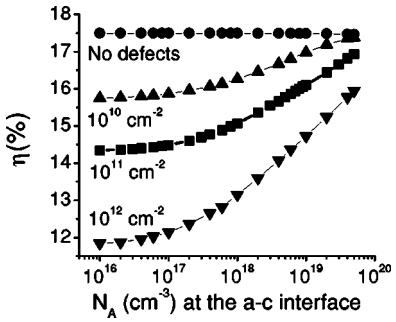

FIG. 5. Efficiency of the annealed *p-p-n* solar cell with respect to the boron concentration at the *a-c* interface. Curves are plotted for a defect-free *a-c* interface and for three different qualities of defective *a-c* interfaces. Results are shown for a 6% exponential boron distribution in the PDL layer.

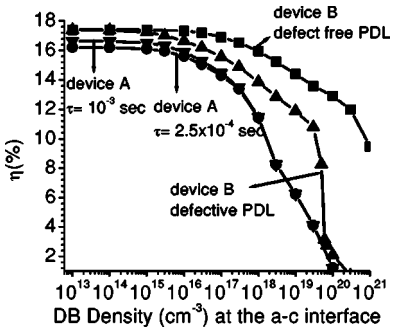

FIG. 7. Hybrid solar cell efficiency with respect to the surface density of defects at the *a-c* interface. The defective *a-c* interface layer is assumed to be 10 nm thick and the boron density at the *a-c* interface is 5×10^{13} cm^{-2} in device B.

dertake a similar study with D-AMPS in hybrid devices made with these poor-quality wafers. Figure 6 illustrates the dependence of the efficiency on the PDL thickness for different boron profiles. Lower minority-carrier lifetimes make the collection of photocarriers more sensitive to the PDL electric -field distribution. When the PDL layer is too thick, the exponential doping profile spreads the electric -field over a large region of the wafer, weakening its intensity and enhancing the recombination losses. On the other hand, when the PDL layer is too thin, the boron profile distributes the electric fields over a very localized region near the *a-c* interface and the free-carrier drift is not very efficient. Hence, the electric-field profile is optimum for intermediate thicknesses of the PDL layer.

Figure 6 also shows how the efficiency varies for different boron profiles. It shows our results for three values of F_w in exponential doping distributions ($F_w=0.5\%$, $F_w=6\%$, and $F_w=5\%$) and in a linear doping profile. Interestingly, the performance is best for more gradual exponential boron profiles and the linear distribution turns out to be the optimum choice. In this case, thin PDL layers enhance J_{sc} and deteriorate V_{oc}, and thick *p-c*-Si layers produce the opposite effect. FF results in a weak function of the PDL thickness.

Under short circuit conditions, annealed solar cells with exponential doping profiles block electron back diffusion into the *p-a*-SiC more efficiently than those with linear doping profiles by reducing recombination losses. Recombination losses near the *a-c* interface in the diffused *p-c*-Si layers

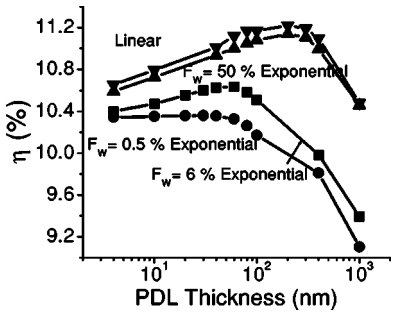

FIG. 6. Efficiency of the annealed *p-p-n* solar cell with respect to the p-*c*-Si thickness for different boron profiles: (▼) linear distribution, (▲) exponential distribution with $F_W=50\%$, (■) exponential distribution with $F_W=6\%$, and (●) exponential distribution with $F_W=0.5\%$. The minority-carrier lifetime in the wafer is 4×10^{-6} s.

are also lower with the exponential profile but the opposite effect is observed in the PDL layer near the *n-c*-Si wafer and in the wafer. When the PDL layer is thicker, the exponential distribution helps to keep J_{sc} near the current generated by the solar cell without the PDL layer (maximum J_{sc}). We observe that the linear boron distribution leads instead to better V_{oc} and FF. The exponential distribution gives rises to V_{oc} values in the range $0.517-0.53$ *V* while for the linear distribution V_{oc} values are in the range $0.53-0.582$ V for PDL layer thicknesses between 4 and 1000 nm. These trends are similar to the ones found in devices made with high-quality wafers. Independently of the boron distribution, the PDL layer tends to reduce J_{sc} and to enhance V_{oc} and FF.

3. Undesired effects: Wafer damage in high-quality wafers

One important issue is the possible damage that boron diffusion can cause to the wafer. In the simulations described above we have made an important assumption: boron entering the *n*-type wafer does not create any additional defects. Figure 7 compares the efficiencies of the annealed *p-p-n* cell for two different scenarios: boron does and does not (Fig. 3) increase the density of defects inside the PDL layer. In our simulations, we not only assume that the boron concentration decays exponentially ($F_w=6\%$) according to Eq. (1) but also that the mobilities, defect cross sections, and densities of dangling bonds follow a similar dependence. The mobilities at the *a-c* defective layer are adopted from tabulated values available for highly boron-doped *c*-Si [$N_A(0)=5\times10^{19}$ cm^{-3}]. Cross sections are assumed to be two orders higher at the *a-c* interface than in the wafer bulk in order to reduce the minority-carrier lifetime by the same amount. The dangling-bond density at the *a-c* interface varies between 10^{13} and 10^{21} cm^{-3}. The PDL layer where mobilities, cross sections, and dangling-bond densities exponentially graded will be called "damaged" PDL in order to make a distinction with respect to regular PDL layers where only boron is assumed to follow an exponential or linear curve.

Our simulations indicate that the grading (lowering) of the free-carrier mobilities in the PDL layer has no impact on the solar cell efficiency. On the other hand, the grading of cross sections and defect densities seriously deteriorates the solar cell performance. Figure 7 indicates that the annealed

TABLE V. Predicted performances for annealed *p-p-n* (B) structures with damaged and nondamaged PDL layers and defective layers at the *a-c* interface of 10^{11} and 10^{13} DB/cm^2.

	Damaged PDL	Defect-free PDL
$N_{a\text{-}c}$ (cm^{-2})	10^{11}	10^{11}
J_{SC} (mA/cm^2)	26.87	29.13
V_{oc} (V)	0.547	0.728
FF	0.808	0.797
Efficiency (%)	11.84	16.91
$N_{a\text{-}c}$ (cm^{-2})	10^{13}	10^{13}
J_{SC} (mA/cm^2)	29.02	27.66
V_{oc} (V)	0.655	0.630
FF	0.819	0.825
Efficiency (%)	11.57	14.39

p-p-n structure (device B) still performs better than the *p-n* structure (device A) even when boron damages the PDL layer. As expected, there is a noticeable drop in the efficiency when the density of defects is higher than $N_A(0)=5\times10^{19}$ cm^{-3}. For dangling-bond densities at the *a-c* interface higher than 5×10^{19} cm^{-3}, the annealed *p-p-n* has no advantages over the conventional *p-n* structure. The damaged PDL layer has a negative impact on all the solar cell parameters but particularly on V_{oc}. Table V compares the solar cell parameters of both B structures for a density of defects at the *a-c* interface of 10^{11} and 10^{13} cm^2. Comparing B structures with damaged and with defect-free PDL layers, we see that additional recombination losses in the defective PDL layer are responsible for the lower V_{oc}

Figure 7 shows that the efficiency of device A (the nonannealed *p-n* junction) improves when a real minority-carrier lifetime of 10^{-3} s is adopted in the wafer (see Table I). This does not change the conclusions drawn above; i.e., the *p-p-n* annealed structure still performs significantly better than the conventional *p-n* heterojunction, although the annealing processes slightly reduce the wafer minority lifetime.

Finally, Figure 8 illustrates the dependence of the *p-p-n* structure (device B) on the PDL thickness for a 6% exponential distribution assuming that the density of defects, defect cross sections, and boron concentration show an exponential distribution inside the PDL layer. For purposes of comparison we include the same curve for a device B that has a defect-free PDL layer. We can see that our predictions in annealed solar cells with damaged PDL layers are different. We observe that there is no optimum PDL thickness for a linear boron profile and that exponential rather than linear boron profiles give rise to higher efficiencies. This result differs from our previous findings for thin PDL layers in *p-p-n* devices with high- and low-quality wafers (see Figs. 4 and 6, respectively). On the other hand, our results in Fig. 8 show some similarities with the ones in Fig. 4 for thick PDL layers. We also see that for devices with thick PDL layers the linear boron profile in damaged PDL layers is more detrimental to the solar cell performance than the exponential profiles, especially for thick PDL layers. We have to keep in mind that in these simulations not only is the boron concentration set to vary linearly with position but also the defect distribution. Hence, by choosing the linear boron profile, we include more defects in the PDL layer than with any exponential distribution. The linear boron distribution significantly magnifies the recombination losses in the PDL region, damaging J_{sc} and V_{oc}. At the same time the linear profile strengthens the electric field in the depletion region and slightly improves the FF. Table VI compares the output parameters of solar cells with a linear and with a 0.5% exponential boron distribution for a 1000-nm-thick PDL region.

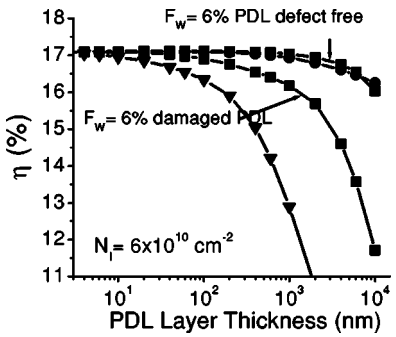

FIG. 8. Efficiency of the annealed *p-p-n* solar cell with respect to the PDL thickness for different boron profiles: (▼) linear distribution, (■) exponential distribution with $F_W=6\%$, and (●) exponential distribution with $F_W=0.5\%$. The surface density of defects at the *a-c* interface is assumed to be 6×10^{10} cm^{-2}. The density of dangling bonds, cross sections, and mobilities are graded inside the PDL layer. For the sake of comparison, we also include the exponential distribution corresponding to $F_W=6\%$ for a defect-free PDL.

TABLE VI. Predicted performances of annealed *p-p-n* (device B) structures with a damaged 1000-nm-thick PDL layer and a defective layer at the *a-c* interface with a surface density of defects of 6×10^{10} DB/cm^2. The linear and the 0.5% exponential boron distributions are compared.

$N_{a\text{-}c}$ (cm^{-2})$=6\times10^{10}$ $W=100$ nm	Linear profile	0.5% exponential
J_{SC} (mA/cm^2)	24.08	29.20
V_{oc} (V)	0.653	0.726
FF	0.820	0.799
Efficiency (%)	12.89	16.93

Figures 4 and 8 indicate that the efficiency of annealed *p-p-n* devices is highest at a particular PDL thickness for the exponential boron profiles. However, our results indicate that the higher efficiency of annealed *p-p-n* structures made with high-quality wafers and which have a low density of defects at the *a-c* interface comes mainly from the lower *p*-layer activation energy and from the lower offsets at the *a-c* interface. The PDL layer plays an important role in annealed *p-p-n* solar cells with highly defective *a-c* interfaces.

IV. CONCLUSIONS

Using numerical computer simulations, we investigate the advantages of a high-temperature-annealed hybrid *p-p-n* amorphous-crystalline silicon solar cell over the conventional *p-n* amorphous-crystalline silicon solar cell. High-temperature-annealed heterojunctions are more robust to the presence of band offsets and defective states at the amorphous-crystalline (*a-c*) interface. Lower offsets facili-

tate the flow of free carriers, and defective layers with a higher surface density of dangling bonds can be tolerated in the annealed structure. Double-emitter *p-p-n* structures give rise to efficiencies that are higher than those of conventional cells because of their lower *p*-layer activation energy and higher built-in potential. The presence of boron at the *a-c* interface and in the front region of the wafer plays a significant role in *p-p-n* structures with a highly defective *a-c* interface and/or a low-quality wafer. In this scenario a linear boron profile is the most appropriate distribution in the diffused *p* layer. For low defective or defect-free *a-c* interfaces and high-quality wafers, a boron exponential profile is more appropriate in annealed structures if boron creates additional defects in the front region of the wafer, the most likely scenario in our solar cells. The boron profile shape is irrelevant if boron does not add additional defects to the front region of high-quality wafers. Thin amorphous layers are recommended to maximize the short circuit current (8 nm). Annealed *p-p-n* solar cells are less sensitive to highly defective or inefficiently doped amorphous layers. For highly doped amorphous layers, the differences between the efficiencies of *p-p-n* and *p-n* structures are smaller and band alignments can define the best performing cell. Back-surface fields and high minority-carrier lifetimes in wafers are beneficial for both structures in similar proportions.

ACKNOWLEDGMENTS

We are very grateful for the financial support of the Agencia Nacional de Promoción Científica y Tecnológica (Argentina), PICT 11-12523 and of the Comisión Interministerial de Ciencia y Tecnologia (CICYT), Spain, program TIC 02-04184-C02.

[1]T. Sawada, N. Terada, S. Tauge, T. Buba, T. Takahama, E. Wakisaka, S. Tsuda, and S. Nakano, *Proceedings of IEEE in World Conference in Photovoltaic Energy Conversion*, Hawaii, 1994 (IEEE, New York, 1994), p. 1219.
[2]M. Tanaka, M. Taguchi, T. Matsuyama, T. Sawada, S. Tsuda, S. Nakano, H. Hanafusa, and Y. Kuwano, Jpn. J. Appl. Phys., Part 1 **31**, 3518 (1992).
[3]K. Sasaki, M. M. Rahman, and S. Furukawa, IEEE Trans. Device Letters 6, 311 (1985).
[4]M. Yabe, N. Satoi, and Y. Seki, Proceedings of the Fourth Sensor Symposium, edited by S. Kataoka, Tsukuba, Japan, 1984 p. 105.
[5]D. Caputo, G. de Cesare, F. Irrera, and F. Palma, IEEE Trans. Electron Devices **43**, 1351 (1996).
[6]Y. A. Chen, C. F. Chiou, W. C. Tsay, L. H. Laih, J. H. Hong, and C. Y. Chang, IEEE Trans. Electron Devices **44**, 1360 (1997).
[7]A. Orpella, J. Puigdollers, D. Bardés, R. Alcubilla, L. F. Marsal, and J. Pallarés, Solid-State Electron. **44**, 1543 (2000).
[8]F. Demichelis, C. F. Pirri, and E. Tresso, Philos. Mag. B **66**, 135 (1992).
[9]L. F. Marsal, I. Martin, J. Pallares, A. Orpella, and R. Alcubilla, J. Appl. Phys. **94**, 2622 (2003).
[10]J. McElheny, J. K. Arch, H. S. Lin, and S. J. Fonash, J. Appl. Phys. **64**, 1254 (1988).
[11]H. Okamoto, H. Kida, and Y. Hamakawa, Philos. Mag. B **49**, 231 (1984).
[12]J. Powel and S. C. Deane, Phys. Rev. B **53**, 10121 (1996).
[13]A. Rubinelli, J. D. Ouwens, and R. Schropp, Proceedings of the 13th European Photovoltaic Solar Energy Conference and Exibition, Nice, France 1995, p. 195.
[14]M. W. M. van Cleef *et al.*, J. Non-Cryst. Solids **227–230**, 1291 (1998).
[15]A. Asano, T. Ichimura, Y. Uchida, and H. Sakai, J. Appl. Phys. **63**, 2346 (1988).