# The data acquisition system of the Latin American Giant Observatory (LAGO)

M. Sofo Haro*, L.H. Arnaldi, For the LAGO Collaboration[1]

Laboratorio Detección de Partículas y Radiación, Centro Atómico Bariloche, Av. Bustillo 9500, S. C. de Bariloche, Río Negro, Argentina

## ARTICLE INFO

## ABSTRACT

LAGO is an extended cosmic ray observatory composed of water-Cherenkov detectors (WCD) placed throughout Latin America. It is dedicated to the study of various issues related to astrophysics, space weather and atmospheric physics at the regional scale. In this paper we present the design and implementation of the front-end electronics and the data acquisition system for readout of the WCDs of LAGO. The system consists of preamplifiers and a digital board sending data to a computer via an USB interface. The analog signals are acquired from three independent channels at a maximum rate of $\sim 1.2 \times 10^5$ pulses per second and a sampling rate of 40 MHz. To avoid false trigger due to baseline fluctuations, we present in this work a baseline correction algorithm that makes it possible to use WCDs to study variations of the environmental radiation. A data logging software has been designed to format the received data. It also enables an easy access to the data for an off-line analysis, together with the operational conditions and environmental information. The system is currently used at different sites of LAGO.

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* Corresponding author.
    E-mail addresses: miguelsofoharo@cab.cnea.gov.ar (M. Sofo Haro), arnaldi@cab.cnea.gov.ar (L.H. Arnaldi).
    [1] W. Alvarez[m], C. Alvarez[i], C. Araujo[r], O. Areso[g], H. Arnaldi[b], H. Asorey[b], M. Audelo[e], H. Barros[t], X. Bertou[b], M. Bonnett[r], R. Calderon[m], M. Calderon[d], A. Campos-Fauth[u], A. Carramiñana[h], E. Carrasco[h], E. Carrera[s], D. Cazar[s], E. Cifuentes[m], D. Cogollo[v], R. Conde[a], J. Cotzomi[a], S. Dasso[g,x,y], A. De Castro[n], J. De La Torre[r], R. De León[m], A. Estupiñan[m], A. Galindo[h], L. Garcia[m], M. Gómez Berisso[b], M. González[b], W. Guevara[c,z], A.M. Gulisano[f,g], H. Hernández[k], A. Jaimes[m], J. López[j], C. Mantilla[d], R. Martín[f], A. Martinez-Mendez[n], O. Martínez[a], E. Martins[v], J.J. Masías-Meza[y], R. Mayo-García[w], T. Melo[v], J. Mendoza[s], P. Miranda[o], E. Montes[v], E. Morales[r], I. Morales[m], E. Moreno[a], C. Murrugarra[t], C. Nina[o], L. A. Núñez[n], A. Núñez-Castiñeyra[k], L. Otiniano[c], J. Peña-Rodríguez[n], J. Perenguez[j], H. Pérez[m], Y. Perez[k], G. Perez[q], S. Pinilla-Velandia[t], E. Ponce[a], R. Quishpe[s], F. Quispe[c], K. Reyes[l], H. Rivera[o], J. Rodriguez[r], M. Rodríguez-Pascual[w], M. Romero[r], A.J. Rubio-Montero[w], H. Salazar[a], J. Salinas[o], C. Sarmiento-Cano[n], I. Sidelnik[b], M. Sofo Haro[b], M. Suárez-Durán[n], M. Subieta[o], J. Tello[t], R. Ticona[t], I. Torres[h], L. Torres-Niño[n], J. Truyenque[c], M. Valencia-Otero[n], S. Vargas[n], N. Vásquez[d], L. Villasenor[p], M. Zamalloa[r], L. Zavala[e]

[a] Benemérita Universidad Autónoma de Puebla, Mexico
[b] Centro Atómico Bariloche/Instituto Balseiro (CNEA/CONICET/UnCuyo), Argentina
[c] Comisión Nacional de Investigación y Desarrollo Aeroespacial, Peru
[d] Escuela Politécnica Nacional, Ecuador
[e] Escuela Superior Politécnica de Chimborazo, Ecuador
[f] Instituto Antártico Argentina, Dirección Nacional del Antártico, Argentina
[g] Instituto de Astronomía y Física del Espacio, IAFE (UBA-CONICET), Argentina
[h] Instituto Nacional de Astrofísica, Óptica y Electrónica, Mexico
[i] Universidad Autónoma de Chiapas, UNACH, Mexico
[j] Universidad Central de Venezuela, Venezuela
[k] Universidad de Los Andes, ULA, Venezuela
[l] Universidad de Nariño, Colombia
[m] Universidad de San Carlos, Guatemala
[n] Universidad Industrial de Santander, Colombia
[o] Universidad Mayor de San Andrés, Bolivia
[p] Universidad Michoacana de San Nicolás de Hidalgo, Mexico
[q] Universidad Politécnica de Pachuca, Mexico
[r] Universidad San Antonio Abad del Cusco, Peru
[s] Universidad San Francisco de Quito, Ecuador
[t] Universidad Simón Bolivar, Venezuela
[u] Universidade Estadual de Campinas, Brazil
[v] Universidade Federal de Campina Grande, Brazil
[w] Centro de Investigaciones Energéticas Medioambientales y Tecnológicas, Spain
[x] Departamento de Ciencias de la Atmósfera y los Océanos, Facultad de Ciencias Exactas y Naturales, Universidad de Buenos Aires, Argentina
[y] Departamento de Física, Facultad de Ciencias Exactas y Naturales, Universidad de Buenos Aires, Argentina
[z] Instituto Geofísico del Perú (IGP), Peru

# 1. Introduction

Cosmic particles of various types reach the Earth. They rain down constantly, some of them with energies much higher than can be generated in any man-made experiment. Cosmic rays contribute to natural background radiation and produce some of the most interesting and still deeply unknown phenomena in particle and astroparticle physics. In order to understand these physical phenomena and others directly related with them, it is necessary to study the cosmic ray flux and composition in detail.

Given the maturity of current electronics design, we can find high performance systems at low costs. Nowadays, it is possible to find systems with response times in the order of nanoseconds and even faster. The high-energy physics community has benefited deeply from these improvements, and many experiments are producing, acquiring and analyzing data at rates and costs unreachable a decade ago. The Latin American Giant Observatory (LAGO) [1] is one of them. It is an international project of astroparticle physics that involves institutions from 10 countries (Argentina, Bolivia, Brazil, Colombia, Ecuador, Guatemala, Mexico, Peru, Spain and Venezuela). LAGO operates a network of water-Cherenkov detectors (WCD) widely spread over Latin America. The project objectives include: the operation of Cherenkov detectors at high altitude searching for the high-energy component of gamma-ray bursts, the study of the space weather through the solar modulation of galactic cosmic rays, and the precise measurement of the flux of background radiation at ground level.

In this context, a fundamental requirement is to have a high-speed data acquisition (DAQ) system, in order to register the fast signals produced within the detector volume. These fast signals are a consequence of the passage, through the water volume of the detector, of the secondary particles coming from the interaction of cosmic rays in the atmosphere.

In this paper we present a system that is primarily designed for the LAGO Project, but which is also easily adaptable to other experiments. The design of the hardware is a derivation of that used in the Pierre Auger Observatory, optimized to be cost effective for LAGO [2,3]. It is a powerful electronic platform that simplifies the process of acquiring the high rates of cosmic-ray events or signals with similar characteristics. Besides its primary use as an acquisition system for astroparticle experiments, it is also well suited as a teaching tool, helping students to incorporate concepts related to the acquisition, processing and analysis of large amounts of data in real time.

# 2. Description of the data acquisition system

The LAGO Project uses water tanks as particle detectors. A typical WCD of LAGO is a tank filled with purified water, having a volume lying in the range between 1 m$^3$ and 40 m$^3$. The detector is sensitive to the Cherenkov radiation produced by the charged particles passing through the water volume. The WCD is also sensitive to high-energy photons, which through pairs creation emit secondary electrons and positrons that also produce Cherenkov light. The detector has an internal bag containing the water, made by a highly diffusive and reflective fabric of commercial Tyvek[2] 1073D or equivalent [4]. The diffusion of Cherenkov photons in this inner coating reduces the signal dependence on the trajectory of secondary particles within the detector, since photons are spread evenly. A photomultiplier tube (PMT) overlooks the water volume and collects the Cherenkov photons. Hamamatsu R5912 8-in. PMTs are used. The PMT base is equipped with an (active or passive)
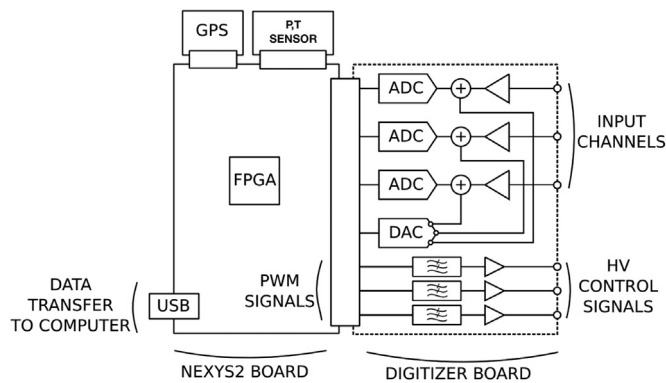


**Fig. 1.** Block diagram of the acquisition system. The main system components are shown: the three channel digitizer card, the Nexys-II board and the peripherals (GPS and the pressure and temperature sensor).

voltage divider, a high-voltage power supply and a preamplifier for conditioning the amplitudes of the output pulses [5]. The high-voltage covers the range from 0 to −2000 V with respect to ground and can be controlled by a low voltage in the range of 0 to +5 V. Our DAQ provides the voltages required for the high-voltage supply and the other components in the PMT base.

The shape of the pulses coming from the detector depends on the water purity, the reflectivity of the diffusing material and the geometry of the tank. It is the result of the convolution between the response of the PMT to individual photons and the time distribution of the photons reaching the PMT, after successive reflections on the inner coating and propagation through the water. Typically, a WCD detector delivers pulses with a sharp rise time (∼10 ns) and a decay time (∼70 ns) dominated by the attenuation length of the Cherenkov photons in the water.

Fig. 1 summarizes our data acquisition system, it is composed of a digitizer card, a commercial Nexys-II[3] board and the external sensors as peripherals. The electronic card digitizes pulses from three independent channels simultaneously, at a sampling rate of 40 MHz. Each channel has an anti-aliasing filter and a baseline stabilizer circuit. The digitizer card is connected, through a Hirose FX2 high-speed connector, to the Nexys-II board.

We have implemented a simple triggering algorithm for the acquisition of the pulses: all the pulses with an amplitude above a required threshold are stored locally, and are then transferred to a PC.

Working in this configuration, the maximum acquisition rate is of the order of $1.2 \times 10^5$ pulses per second. Additionally, the system can be operated in a mode where only the maximum amplitude and charge of each pulse is stored (i.e., the area under the curve), reaching acquisition rates of up to $2 \times 10^6$ pulses per second.

The acquisition system can be controlled via a standard USB port connected to a PC or a single board computer (SBC). The operating parameters, such as the trigger level, the high voltage at each channel and the GPS time format, can be programmed by the user at runtime. The data is transferred in real time to the PC for storage and offline analysis. In addition to the acquisition of the pulses from the three channels, further information related to the underlying environmental conditions, such as the pressure and temperature, is recorded every second.

The FPGA present on the Nexys-II board is responsible for the acquisition and pre-processing of the data, the setting of the trigger thresholds and the adjustment of the voltages, as well as the control and communication with the peripherals (the GPS and the pressure and temperature sensor). The three control signals for

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[2] Tyvek is a trademark of Dupont.

[3] http://www.digilentinc.com/Products/Detail.cfm?Prod=NEXYS2.
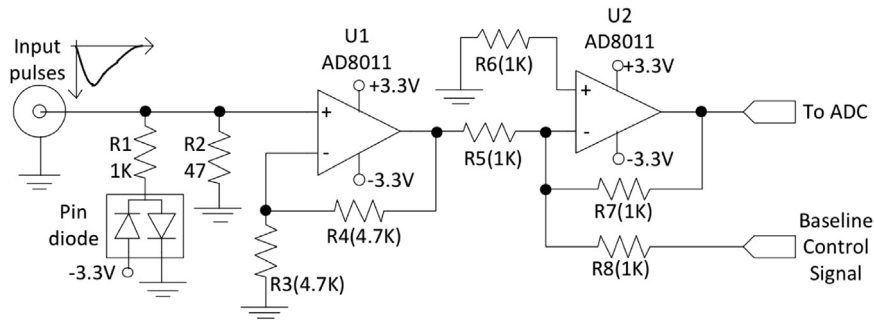
**Fig. 2.** Schematic diagram of one acquisition channel. It is composed of a voltage amplifier, acting also as anti-aliasing filter, and a baseline stabilization stage before the pulses reach the ADC chip. The stabilization stage can be controlled by the FPGA.
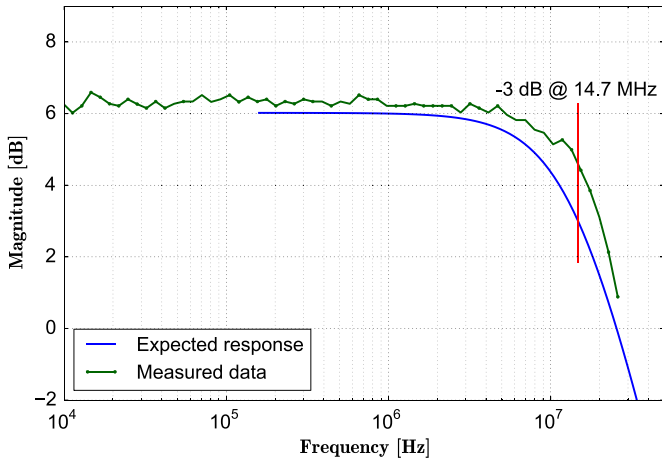


**Fig. 3.** Closed-loop gain of the anti-aliasing filter. A comparison between the expected and the measured response is shown. The graph shows a good agreement, within the 1.0 dB level. The $-3$ dB point is found at 14.7 MHz.

the high-voltage source are generated independently, using a pulse width modulation (PWM) technique.

## 2.1. The digitizer card

The DAQ card is powered with 12 V DC and offers the possibility to distribute its input voltage to the bases of the PMT so that the whole setup can be operated with a single main power supply.

We use currently the version 2.0 of the DAQ card, it is a two-layer electronic card, which has three independent acquisition channels. Each channel consists of three stages: a voltage amplifier, implemented with a current feedback amplifier (CFA) in a non-inverting configuration, acting also as anti-aliasing filter, an analog adder intended for the baseline stabilization and the ADC chip to digitize the analog pulses of the detector. The input has a matching resistor of 50 $\Omega$ to avoid reflections and two diodes for the CFA input protection. In Fig. 2 we present a schematic diagram of the first two stages of one acquisition channel.

The CFA topology of operational amplifiers allows for a wide bandwidth, absence of slew rate limitation, and above all, essentially the absence of a gain-bandwidth product limit. This occurs because the bandwidth of the current feedback topology, in a first order analysis, is independent of gain and only depends on the value of the feedback resistor [6]. The bandwidth of the first stage shown in Fig. 2 depends only on $R_4$, instead of the voltage closed-loop gain $1 + R_4/R_3$, as normally occurs in the voltage feedback amplifiers (VFA). Therefore, $R_4$ can be used to select the bandwidth and $R_3$ to select the gain. The ability to control the bandwidth independently is an important advantage of the CFA over conventional operational amplifiers for this

application. The theoretical cutoff frequency of the designed anti-aliasing filter is 14.7 MHz, as shown in Fig. 3.

The bandwidth can be calculated with the relation $f_{CL} = (R_c/R_4)f_{OL}$, where $f_{CL}$ represents the closed-loop cutoff frequency and $f_{OL} = (2\pi R_c C_c)^{-1}$ is the open-loop cutoff frequency, determined by the CFA internal parameters $R_c$ and $C_c$.

The electronic front-end can manage negative pulses with amplitudes up to $-3.5$ V. The analog-to-digital conversion is performed by a 10-bit ADC. We use an AD9203 chip from Analog Devices. In order to accommodate the high dynamic range of the output pulses coming from the detector, the reference voltage of the chip can be changed by means of an external jumper, depending on the saturation level of the input. In the typical configuration, the 10-bit resolution gives a minimum detectable voltage level of 976 μV.

Due to the nature of the experiment, which is the measurement of the rate of particles at ground level with great accuracy, the stabilization of the electronic response against environmental effects is crucial. Since the trigger system compares the instantaneous voltage at each channel with a reference voltage (i.e., the settled trigger threshold), any change in the level of the baseline could bias the measurements. These baseline changes, caused by temperature variations, can be significant at low thresholds, since the flux of secondary particles varies with the particle energy as a power law. Therefore, to avoid this and also the low level electronic noise, the front-end maintains the baseline in a stable value of 50 ADC bins ($\sim$49 mV) by adding an offset voltage in the second stage of each input channel. The pulse polarity is also inverted at the second stage to match the expected input for the ADC chip.

The baseline offset voltage is generated by the FPGA and is applied through a 12-bit digital-to-analog converter (DAC). This voltage excursion is then added to the input signal of each channel independently to achieve an automatic baseline control. The FPGA updates the offset at a constant rate of 5 kHz (every 2 ms). The impact of the baseline correction is shown in Fig. 4, where averages over 1 s and 15 min of the baseline are compared to the evolution of temperature over several days. The correlation of the baseline with temperature and the behavior of one channel when no baseline correction is added are clearly visible, even for this particular experimental setup in which the digitizer card was operated within a laboratory room with small changes in the air temperature, while the WCD was outside the building.

There are three circuits that complete the electronic front-end, each of which can control independently a high-voltage source to power a PMT. Each circuit provides a user-programmable voltage in the range of 0 to $+5$ V. When coupled to a PMT base, this voltage drives an output voltage in the range of 0 to $-2000$ V.

This setup allows us to independently control up to three WCD in the same place, thereby reducing costs. Furthermore, this also allows one to perform coincidence studies between detectors. If more
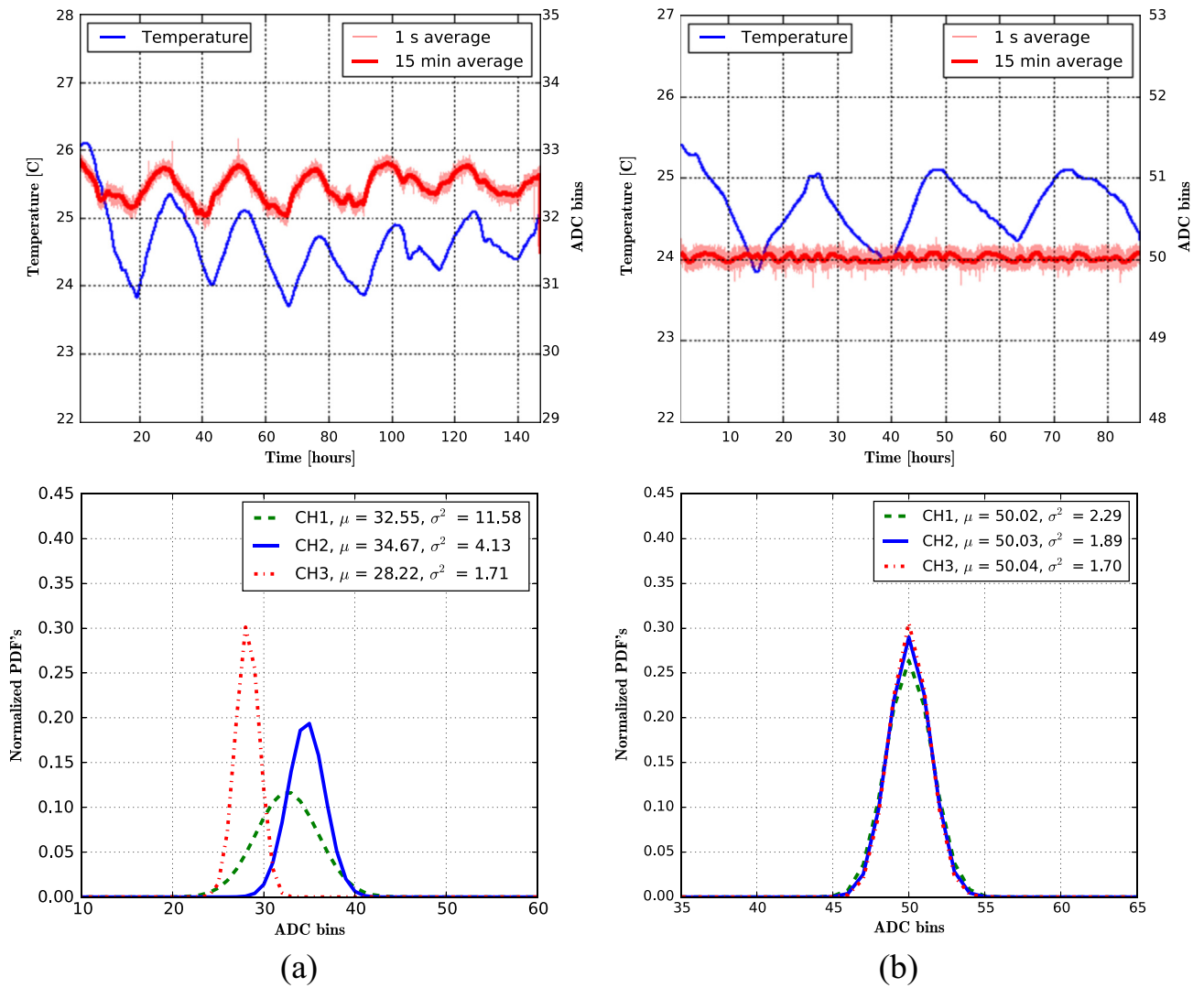
**Fig. 4.** Baseline without (a) and with (b) the baseline offset algorithm described in the text. In the upper panels the baseline evolution as a function of time is shown. The correlation with temperature is clearly visible when no correction is applied (left), even for short time periods. In the lower panels, the histograms of the three baselines are shown. The electronic boards were within a laboratory room, while the WCD was outside the building in this experimental setup.
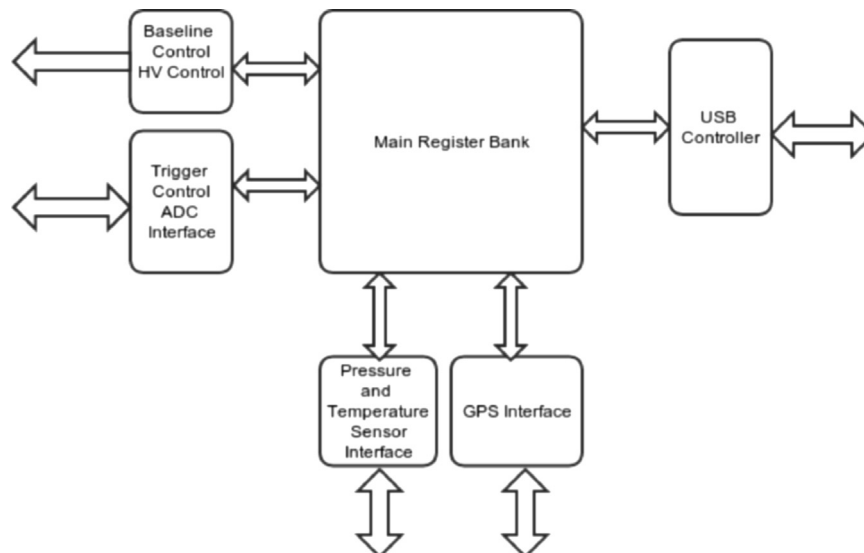


**Fig. 5.** Higher hierarchy blocks of the FPGA firmware. Essentially, it is a large register bank, accessible for the attached peripherals.
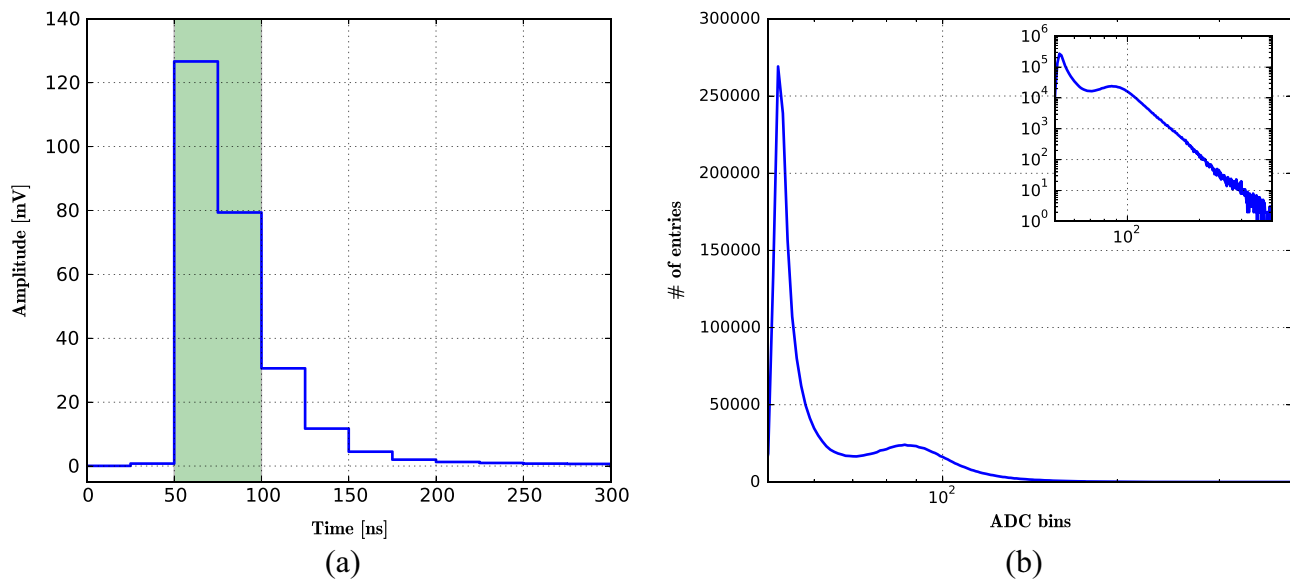
**Fig. 6.** (a) Average pulse of a typical 1.8 m$^3$ WCD working with a central 8-in. PMT. The high-voltage source is set at 1.5 kV. (b) Charge histogram of the pulses registered during one hour of data acquisition. Two peaks are clearly visible: the first is an artifact of the triggering system, as what is plotted here is the histogram of the total integrated area of the pulses, while the trigger occurs in amplitude. The second maximum is associated with the passage of vertical and central muons through the water volume. Inset shows the same histogram in log scale. This histogram is used for the calibration of the WCD.

detectors are required, multiple electronic cards can be synchronized by using a single GPS signal, the one-pulse-per-second (1PPS) signal.

### 2.2. The FPGA firmware

Given the high level of integration required and the desired flexibility for the system, we had to implement part of the data acquisition system in an FPGA. The managing and pre-processing of the data is done in the Nexys-II electronic board, as described above. The firmware of the FPGA is a mixture of blocks implemented in the standard VHDL programming language [7]. The firmware consists of a large bank of registers which peripherals can access for reading and writing. Fig. 5 illustrates the implementation of the firmware as a block diagram.

There are several specific hierarchical blocks in charge of the different tasks at FPGA level. One of these blocks can manage the corresponding high-voltage source of the PMT, generating a slow ramp of voltage to increment and/or decrements the voltage to the PMT. This voltage ramp is done to protect the PMTs because rapid voltage changes can destroy it. Another block implements the baseline correction algorithm, as described in Section 2.1. The firmware also implements various standard communication protocols (SPI, I2C and UART) to manage the attached peripherals.

The FPGA generates the 40 MHz clock signal for the fast ADC, allowing a completely synchronous design. The whole system is controlled by a state machine implemented in the FPGA.

#### 2.2.1. The trigger sub-system

The trigger sub-system, a block of code implemented in the FPGA, is responsible for deciding which pulses can be acquired. At every clock pulse the trigger algorithm compares the digitized input signal, $V_i$, with the absolute trigger threshold, $V_{thr}$, set by the user in ADC bins before the start of the data acquisition. If $V_i > V_{thr}$, this input value is stored into an internal memory, the trigger condition is fulfilled and acquisition of the pulse starts. The two previous values, $V_{i-1}$ and $V_{i-2}$, are then recovered from the internal memory to provide a good definition of the rise time of the pulse. The first three temporal bins are therefore acquired only when the trigger condition is fulfilled. After this first step, a programmable number of extra temporal bins, typically 9–17, are acquired to get the complete pulse. In the basic

configuration, 9 additional temporal bins are stored, making a total of 12 bins (i.e., 300 ns at 40 MHz) for an individual pulse.

As longer acquisition windows imply larger amount of data to be stored and transferred (an important issue in some remote locations of the LAGO Project), we have conducted an analysis of the typical duration of the pulses coming from different detectors. We have compared the responses of different WCDs to determine the average pulse for them. For the typical geometries and bias voltages used in the WCDs of LAGO, a pulse length of 12 bins ensures no clipping and a manageable size of the acquired data.

The trigger algorithm is applied independently on the three channels. If the trigger condition is fulfilled in at least one of them, the signal is acquired on the three channels at the same time, allowing an offline search for time coincidences on up to three different detectors with a single electronic system.

Additionally, there are two internal counters. One of them, a 30-bit counter that increments every time the triggering condition is fulfilled in at least one channel, assigns consecutive numbers to each acquired pulse. This counter allows the identification of missing pulses, due to buffering overflow with the highest rates of acquisition. The second one is in charge of counting the number of rising edges of the clock in the current second. If a GPS is present, the counter monitors the stability of the clock signal generated by the FPGA. If no GPS is connected, the counter is used as an internal clock signal. This counter also assigns a time stamp to every pulse recorded. The acquired pulses are thus labeled with three numbers: the pulse count, the time stamp, and a 3-bit mask identifying the channels fulfilling the trigger conditions.

There is another working mode, the sub-trigger mode, with an algorithm similar to the normal trigger mode, but with different data recorded. If the input signal level is above the user-defined sub-trigger threshold, the signal maximum (i.e., the pulse peak) and the integral of the pulse (i.e., the pulse charge), instead of the entire pulse, are transferred. This working mode gives extra flexibility to the system, allowing to get higher data rates.

The data flow is done through a standard USB port. An FX2LP chip from Cypress, present on the Nexys-II board, manages the data flow between the acquisition system and the PC or SBC. In order to have an open source system, the commercial Digilent™

USB driver was replaced by the FPGALink libraries,[4] an open source implementation specifically designed for the FX2LP chip.

### 2.3. The PC software

The final step of the acquisition system is a computer program running on a PC or a SBC, acting as a link between the end-user and the electronic system. It is written in ANSI C++ language, using open source libraries. The whole code is licensed under BSD-2[5] license and is available at the LAGO public repository, on github[6] for downloading.

The entire process of data acquisition is managed by this software, allowing direct access to peripherals of the electronic front-end. It is possible to check the status of the GPS or the pressure and temperature sensor directly from the command line. Through this software we can access all the FPGA registers. We can check the status of these internal registers or configure the thresholds for the channels.

The data logging software was designed to obtain data from the FPGA and create the files to save them. To ease the handling and transfer of data from remote sites, each file corresponds to one hour of acquisition. The data is saved in a hierarchical arrangement of ASCII files, containing the acquired pulses of each channel and their corresponding labels (the pulse counter, the trigger time stamp and channel mask).

In order to cross-check the data from different detectors located in different places, we have created a repository [8] for storing the data of all the WCDs in LAGO. Different levels of metadata are stored for offline analysis and to organize the data repository. Three main levels of metadata are used: the first level, the file header, includes the complete information of the registers, the trigger levels and sub-trigger thresholds, the PMT high-voltages and the internal constants of calibration from the temperature and pressure sensor. The second level of metadata is saved every second and gives information about the internal clock frequency, GPS time and localization, local temperature and atmospheric pressure. The third level is stored as the file footer, with information about the last hour of acquisition: trigger rates per channel, averages of atmospheric conditions and the status of the acquisition card. An additional file, containing only the first and the third level of metadata, is produced to ease the data uploading procedure into the repository. After one hour of data taking, a new file is created, while the current file is closed and compressed.

### 2.4. Example analysis

A typical analysis of data produced by the acquisition system can be seen in Fig. 6. An average pulse can be reconstructed from the multiple pulses recorded. This average pulse gives direct information regarding the propagation of Cherenkov photons within the detector and can be used as a tracer for the water purity and the internal wall reflectivity. Building the charge histogram of all recorded pulses allows one to determine the position of the vertical equivalent muon (VEM), the average energy deposited by a through-going central muon, appearing usually as a well identified peak in the charge histogram. This calibration point is crucial to the operation of WCD in many experiments, such as the Pierre Auger Observatory [9–11]. Other possible analyses include (but are not limited to) the study of the muon lifetime by looking at the histogram of the time difference between successive pulses [12], the study of the flux of particles in single detectors at millisecond levels in search of transient events, or looking for coincidences at the level of tens of nanoseconds between nearby detectors, in order to detect extended air showers of cosmic rays with energies of TeV and above.

### 3. Conclusions

We have presented a highly configurable data acquisition system of low cost, based on off-the-shelf components. The acquisition system was designed from scratch, taking into account the key features of the physical processes involved, in order to provide a flexible and yet powerful platform to digitize and acquire data from different types of detectors of particles and radiation.

The data acquisition system is managed through simple open-source software which monitors the acquisition parameters and the general status of the system. The software can record all the pulses observed in the detector and send them to a dedicated PC for an offline analysis.

Although this acquisition system was designed as the main data acquisition platform of the LAGO Project, it can also be used, with minor changes, in similar experiments where nanosecond resolution and high-speed data acquisition are required.

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[6] https://github.com/lagoproject/acqua.